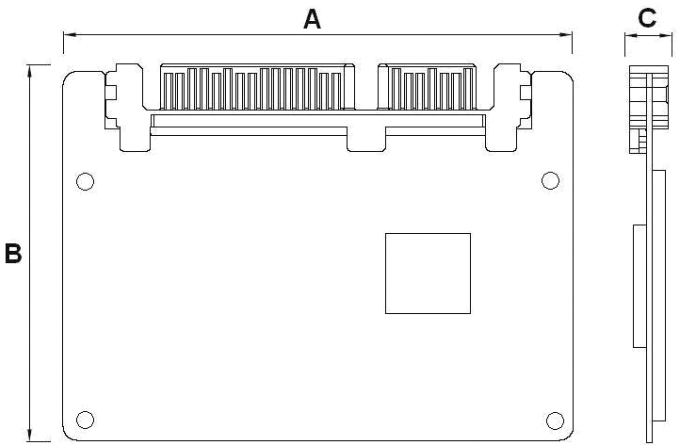
TS4GSSD25H-M
TS8GSSD25H-M
TS16GSSD25H-M
TS32GSSD25H-M
TS64GSSD25H-M

2.5” Half-Slim Solid State Disk

Description

Due to smaller size, huge capacity, high speed, and low power consumption, Transcend’s 2.5” Half-Slim Solid State Disk is perfect replacement storage device for mobile devices, such as mobile tablet, Netbook and CULV (Consumer Ultra Low Voltage) Netbook.

Placement



Features

- RoHS compliant
- Fully compatible with devices and OS that support the SATA 3.0Gb/s standard
- Non-volatile Flash Memory for outstanding data retention
- Advanced Global Wear-Leveling and Block management for reliability
- Built-in ECC (Error Correction Code) functionality
- Support Security Command
- Support HW purge function (optional)
- Compliant with JEDEC MO-297
- Shock resistance

Dimensions

Side	Millimeters	Inches
A	54.00 ± 0.40	2.160 ± 0.016
B	39.00 ± 0.20	1.560 ± 0.008
C	4.00 ± 0.15	0.160 ± 0.004

TS4GSSD25H-M
TS8GSSD25H-M
TS16GSSD25H-M
TS32GSSD25H-M
TS64GSSD25H-M

Transcend®

2.5” Half-Slim
Solid State Disk

Specifications

Physical Specification		
Form Factor		2.5-inch Half-Slim
Storage Capacities		4 GB to 64 GB
Dimensions (mm)	**Length**	54.00 ± 0.40
	Width	39.00 ± 0.20
	Height	4.00 ± 0.15
Input Voltage		5V ± 5%
Weight		10 g
Connector		SATA 7+15 pins combo connector

Environmental Specifications		
Operating Temperature		0 ℃ to 70 ℃
Storage Temperature		- 40 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Power Requirements			
Input Voltage		5V ± 5%	
Mode		**Max. (mA)**	**Max. (W)**
Power Consumption	**Write**$_{(peak)}$	341.4	1.7
	Read$_{(peak)}$	293.7	1.5
	Idle$_{(peak)}$	131.1	0.7

Performance		
Model P/N	**Sequential Read** (Max.)	**Sequential Write** (Max.)
TS4GSSD25H-M	35MB/s	12MB/s
TS8GSSD25H-M	55 MB/s	18 MB/s
TS16GSSD25H-M	100 MB/s	20 MB/s
TS32GSSD25H-M	100 MB/s	40 MB/s
TS64GSSD25H-M	100 MB/s	38 MB/s

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS4GSSD25H-M	7,732,368	7,671	16	63
TS8GSSD25H-M	15,621,984	15,498	16	63
TS16GSSD25H-M	31,277,056	16,383	16	63
TS32GSSD25H-M	62,586,880	16,383	16	63
TS64GSSD25H-M	125,206,528	16,383	16	63

Reliability	
Data Reliability	Supports BCH ECC 8/15 bit per 512-byte and 16/30 bit per 1 KB
Data Retention	10 years
MTBF	1,500,000 hours

Regulations	
Compliance	CE, FCC and BSMI

Reliability

Global Wear Leveling – Advanced algorithm to enhance the Wear-Leveling Efficiency

There are 3 main processes in global wear leveling approaches:

(1) Record the block erase count and save in the wear-leveling table.

(2) Find the static-block and save it in wear-leveling pointer.

(3) Check the erase count when the block popped from spare pool. If the block erase count is bigger than WEARCNT, then swapped the static-block and over-count-block. After actual test, global wear leveling successfully even the erase count of every block; hence, it can extend the life expectancy of Flash product.

ECC algorithm

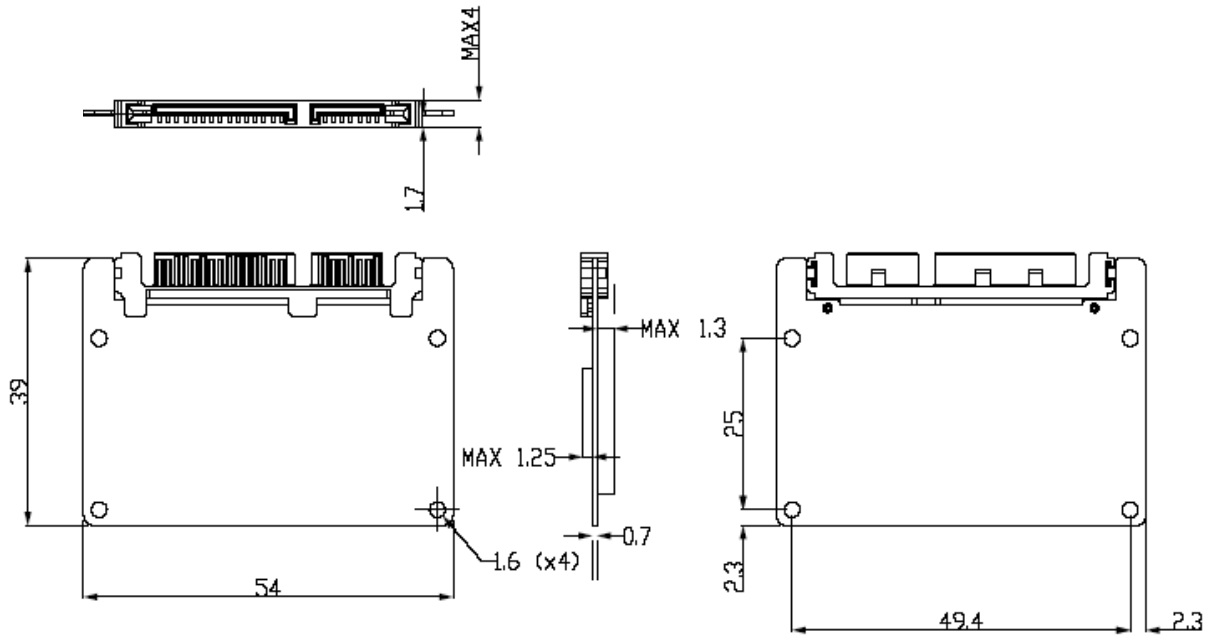
The controller uses BCH8/BCH15 ECC algorithm per 512 bytes and BCH16/BCH30 ECC algorithm per 1 KB according to structure of flash. BCH8/BCH15 can correct up to 8 or 15 random error bits within 512 data bytes. BCH16/BCH30 can correct up to 16 or 30 random error bits within 1KB data.

Bad-block management

When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as bad block to prevent the used of this block and caused data lost later on.

Package Dimensions

Below figure illustrates the Transcend 2.5” Half-Slim Solid State Disk. All dimensions are in mm.

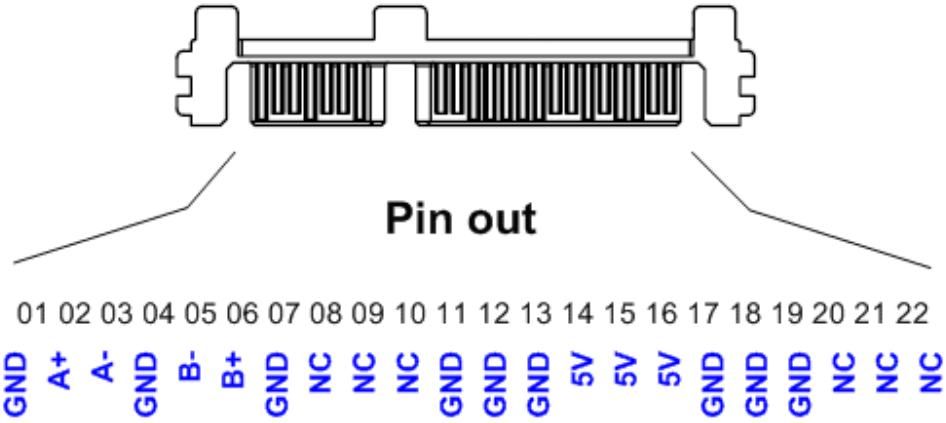


※ **Compliant with JEDEC MO-297**

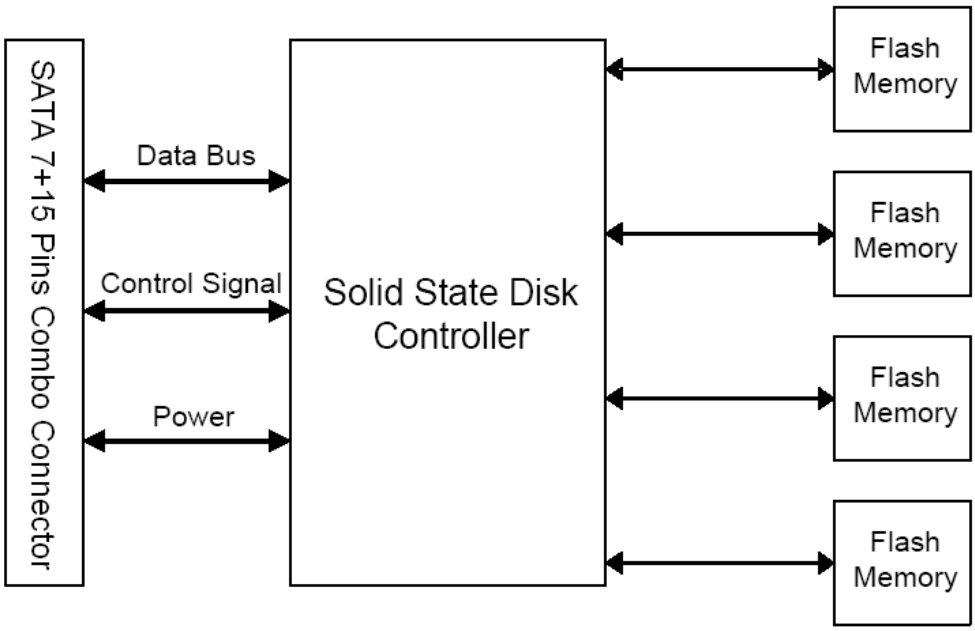
Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	GND	02	A+
03	A-	04	GND
05	B-	06	B+
07	GND	08	NC
09	NC	10	NC
11	GND	12	GND
13	GND	14	5V
15	5V	16	5V
17	GND	18	GND
19	GND	20	NC
21	NC	22	NC

Pin Layout



Block Diagram



SATA Interface

Out of bank signaling

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 $ALIGN_P$ primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having a duration of 160 UI_{OOB}. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 4 and Table 2.

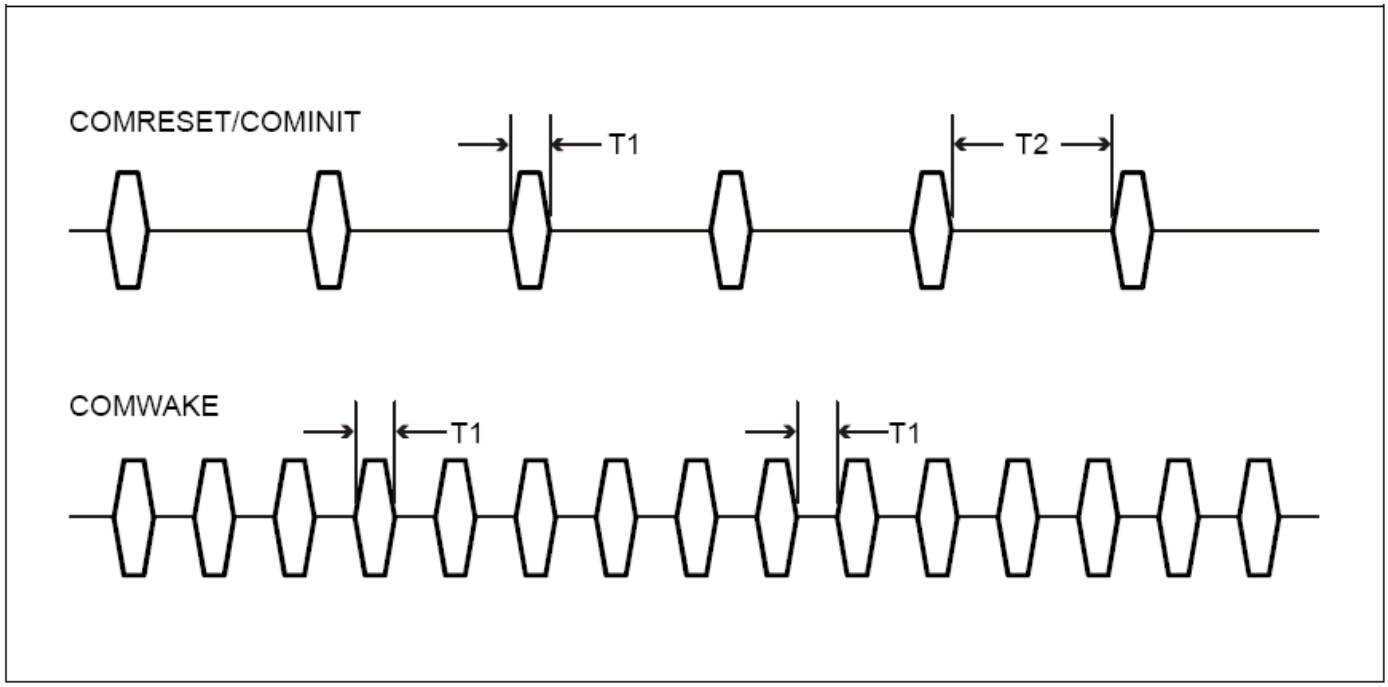


Figure 4: OOB signals

Time	Value
T1	160 UI_{oob} (106.7 ns nominal)
T2	480 UI_{oob} (320 ns nominal)

Table 2: OOB signal times

COMRESET

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing. The COMRESET signal shall be:

1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or

2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or

3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looks for four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer shall initiate the Reset sequence shown in Figure 5 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.

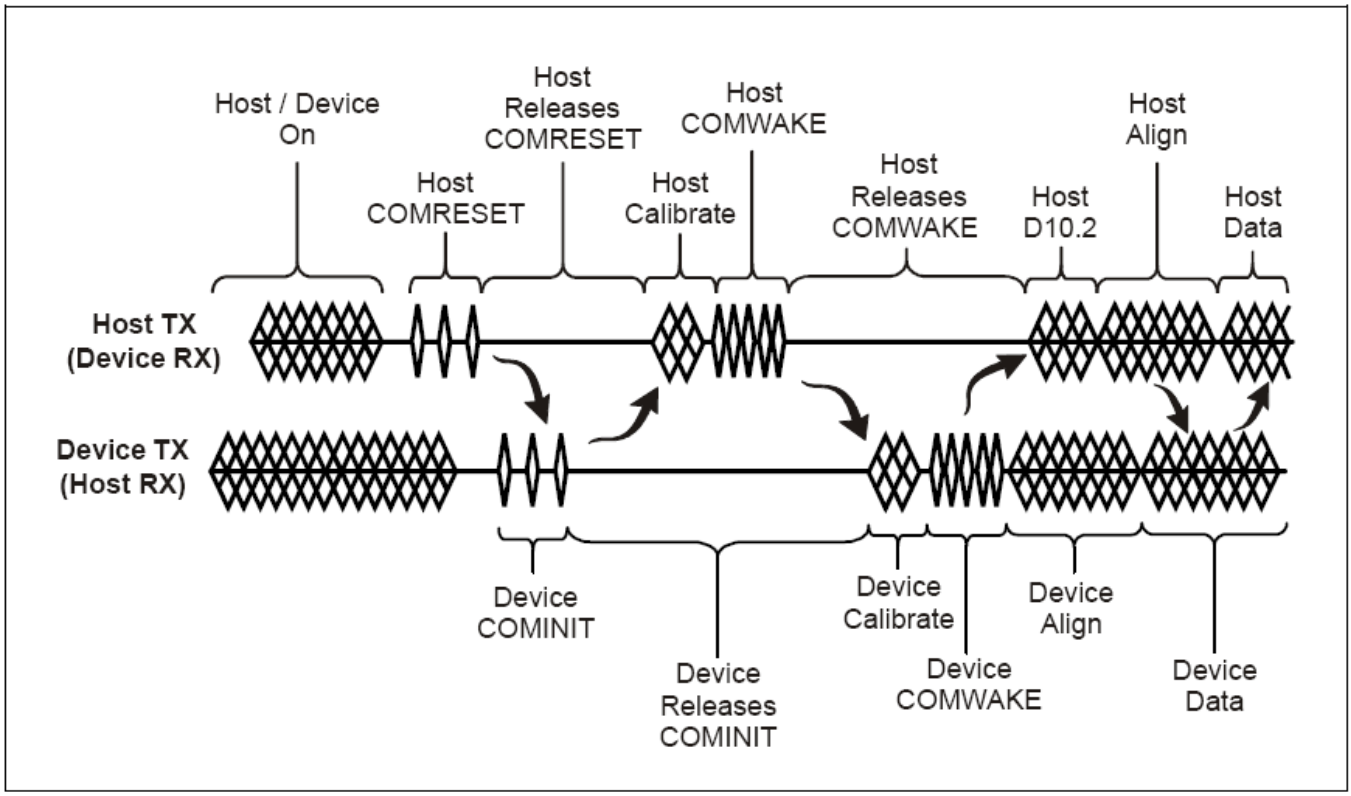


Figure 5: comreset sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the host causes the host to issue COMRESET
3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
4. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
5. Host calibrates and issues a COMWAKE.
6. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.
7. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
8. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
9. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

COMINIT

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 6, below.

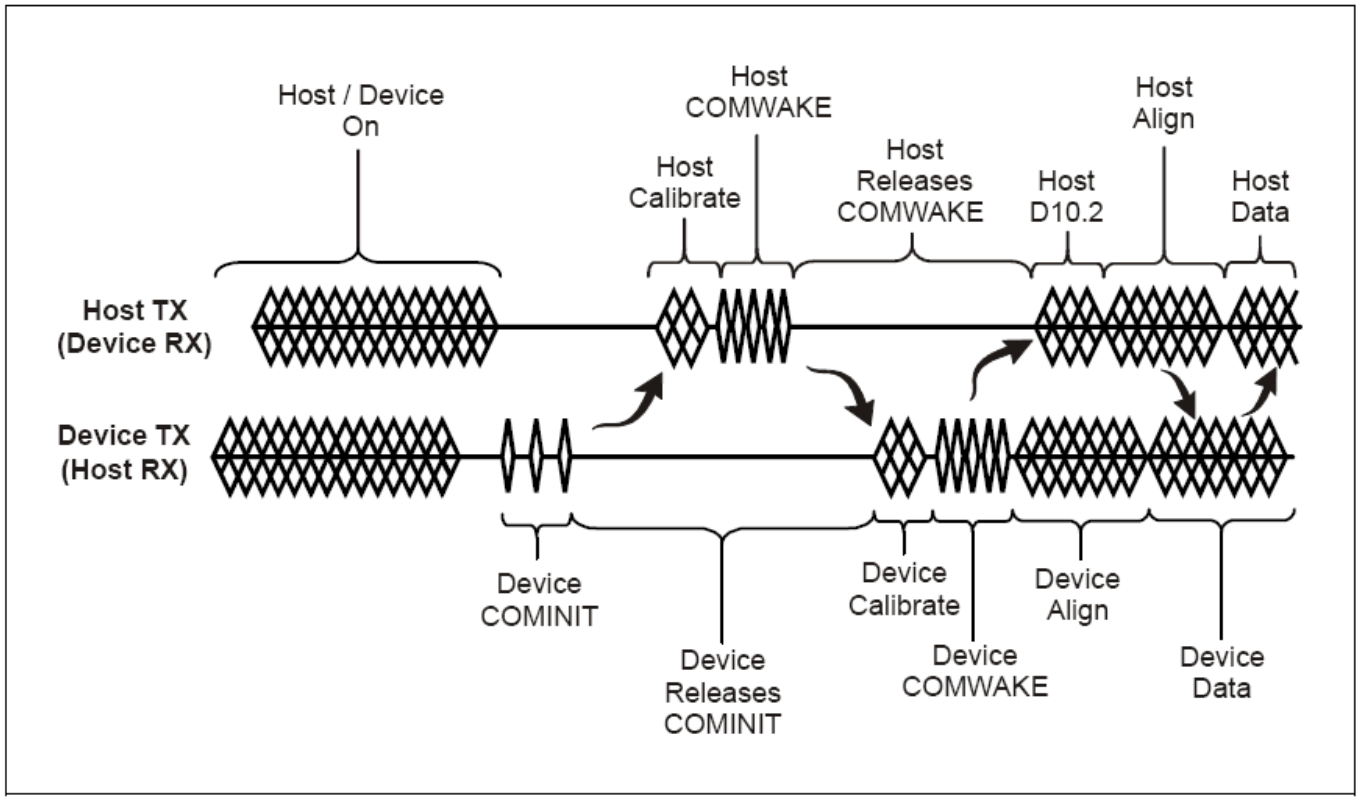


Figure 6: cominit sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

5. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer. 6. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

6. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

Power on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative.

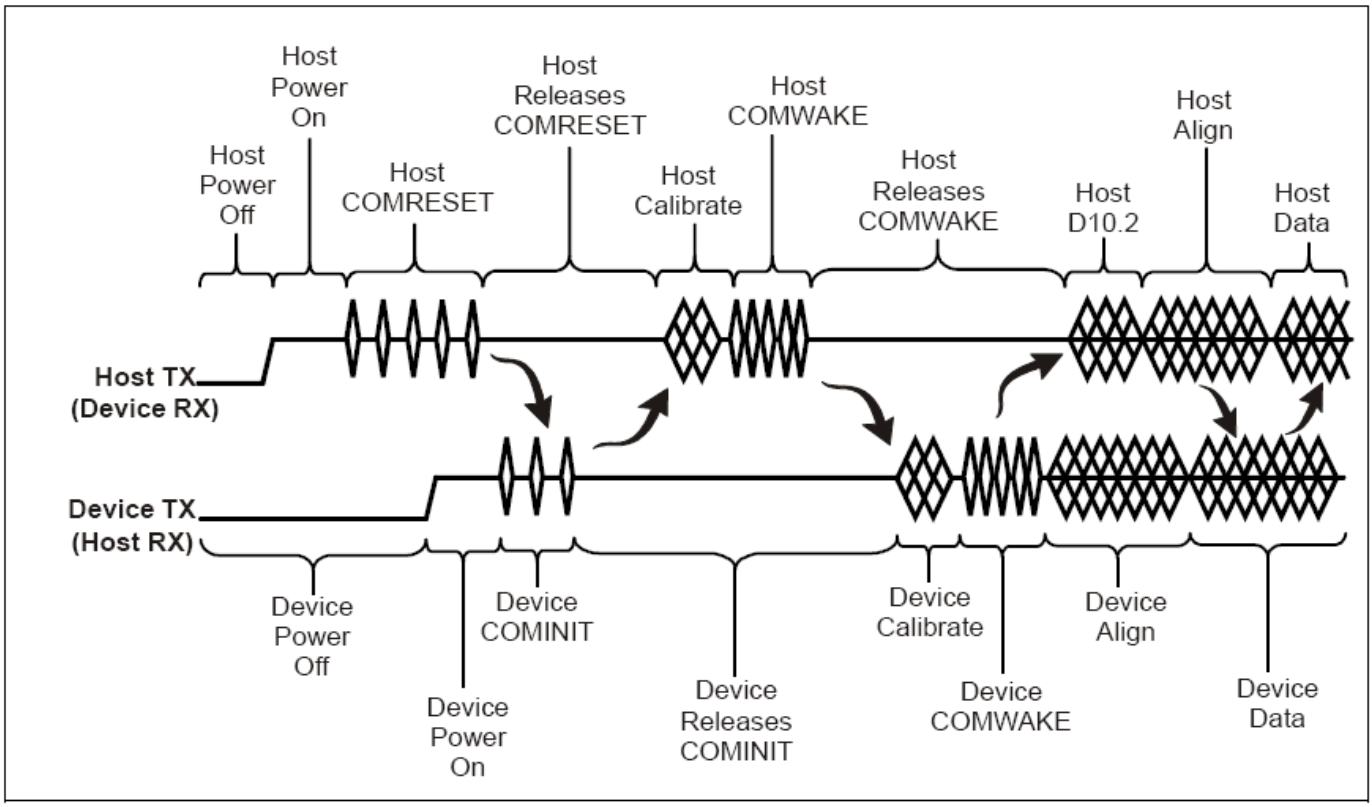


Figure 7: power on sequence

Description:

1. Host/device power-off - Host and device power-off.
2. Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).
3. Host issues COMRESET
4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
5. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
6. Host calibrates and issues a COMWAKE.
7. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After $ALIGN_P$ primitives have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of $ALIGN_P$ primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending $ALIGN_P$ primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.
8. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first $ALIGN_P$. This insures interoperability with multi-generational and synchronous designs. If no $ALIGN_P$ is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
9. Device locks – the device locks to the ALIGN sequence and, when ready, sends the $SYNC_P$ primitive indicating it is ready to start normal operation.
10. Upon receipt of three back-to-back non-$ALIGN_P$ primitives, the communication link is established and normal operation may begin.

ATA command register

This table with the following paragraphs summarizes the ATA command set.

Command Table

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
READ DMA	C8h	DMA
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data

SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-In
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) EXt	24h	PIO data-In
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-In
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write DMA FUA Ext	3Dh	DMA
Write Multiple Ext	39h	PIO data-out
Write Multiple FUA Ext	CEh	PIO data-out
Write Sector(s) Ext	34h	PIO data-out

ATA Command Specifications

CHECK POWER MODE (E5h)

The host can use this command to determine the current power management mode.

EXECUTE DIAGNOSTICS (90h)

This command performs the internal diagnostic tests implemented by the drive.

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

FLUSH CACHE EXT (EAh)

48-bit feature set mandatory command. This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

■ Identify Device Information Default Value

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0000h	2	Obsolete
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer. Supports MDMA Mode 0,1,and 2
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h

Word Address	Default Value	Total Bytes	Data Field Type Information
66	0078h	2	Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-75	0000h	14	Reserved
76	0006h	2	Serial ATA capacities · Support Serial ATA Gen1 · Support Serial ATA Gen2
77-79	000h	6	Reserved
80	0080h	2	Minor version number (ATAPI-7)
81	0000h	2	Minor version number
82-84	742Bh	2	Command sets supported 0
83	550Ch	2	Command sets supported 1
84	4002h	2	Command sets supported 2
85-87	XXXXh	6	Features/command sets enabled
88	007Fh	2	Ultra DMA Mode Supported and Selected
89	0001h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	FFFEh	2	Master Password Revision Code
93-127	0000h	70	Reserved
128	0001h	2	Security status
129-159	0000h	64	Vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	0000h	2	Reserved
165-175	0000h	22	Reserved
176-255	0000h	140	Reserved

- **Word 0: General Configuration**

  Devices that conform to this standard shall clear bit 15 to zero.

  If bit 7 is set to one, the device is a removable media device.

  Bit 6 is obsolete.

If bit 2 is set to one it indicates that the content of the IDENTIFY DEVICE data is incomplete. This will occur if the device supports the Power-up in Standby feature set and required data is contained on the device media. In this case the content of at least word 0 and word 2 shall be valid.

- **Word 1: Default Number of Cylinders**
  This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.
- **Word 3: Default Number of Heads**
  This field contains the number of translated heads in the default translation mode.
- **Word 6: Default Number of Sectors per Track**
  This field contains the number of sectors per track in the default translation mode.
- **Words 7-8: Number of Sectors per Card**
  This field contains the number of sectors per SSD Storage Device. This double word value is also the first invalid address in LBA translation mode.
- **Words 10-19: Serial Number**
  This field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (words (19:10)) and Model number (words (46:27)) shall be unique for a given manufacturer.
- **Word 22: ECC Count**
  This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h.
- **Words 23-26: Firmware Revision**
  This field contains the revision of the firmware for this product.
- **Words 27-46: Model Number**
  This field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (words (19:10)) and Model number (words (46:27)) shall be unique for a given manufacturer
- **Word 47: Read/Write Multiple Sector Count**
  Bits (7:0) of this word define the maximum number of sectors per block that the device supports for READ/WRITE MULTIPLE commands. If the serial interface is implemented, this field shall be set to 16 or less.
- **Word 49: Capabilities**
  Bit 13: Standby Timer
  If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command
  If bit 13 is set to 0 then the Standby timer operation is defined by the vendor.
  Bit 11: IORDY Supported
  If bit 11 is set to 1 then this SSD Storage Device supports IORDY operation.
  If bit 11 is set to 0 then this SSD Storage Device may support IORDY operation.
  Bit 10: IORDY may be disabled
  Bit 10 shall be set to 0, indicating that IORDY may not be disabled.
  Bit 9: LBA supported
  Bit 9 shall be set to 1, indicating that this SSD Storage Device supports LBA mode addressing. CF devices shall support LBA addressing.
  Bit 8: DMA Supported If bit 8 is set to 1 then Read DMA and Write DMA commands are supported. Bit 8 shall

be set to 0. Read/Write DMA commands are not currently permitted on CF cards.

- **Word51: PIO Data Transfer Cycle Timing Mode**
  The PIO transfer timing for each SSD Storage Device falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

- **Word53: Translation Parameters Valid**
  Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any SSD Storage Device that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

- **Word54-56Current Number of Cylinders, Heads, Sectors/Track**
  These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

- **Word57-58: Current Capacity**
  This field contains the product of the current cylinders times heads times sectors.

- **Word 59: Multiple Sector Setting**
  If bit 8 is set to one, bits (7:0) reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. This field may default to the preferred value for the device.

- **Word60-61: Total Sectors Addressable in LBA Mode**
  This field contains the total number of user addressable sectors for the SSD Storage Device in LBA mode only.

- **Word 63: Multiword DMA transfer**
  Word 63 identifies the Multiword DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is enabled, then no Multiword DMA mode shall be enabled. If a Multiword DMA mode is enabled then no Ultra DMA mode shall be enabled.

- **Word 64: Advanced PIO transfer modes supported**
  Bits (7:0) of word 64 of the IDENTIFY DEVICE data is defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting.

  Of these bits, bits (7:2) are Reserved for future PIO modes. Bit 0, if set to one, indicates that the device supports PIO mode 3. All devices except CFA and PCMCIA devices shall support PIO mode 3 and shall set bit 0 to one. Bit 1, if set to one, indicates that the device supports PIO mode 4. If the serial interface is implemented, bits (1:0) shall be set to one.

- **Word 65: Minimum Multiword DMA transfer cycle time**
  Word 65 of the parameter information of the IDENTIFY DEVICE command data is defined as the minimum Multiword DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the device supports when performing Multiword DMA transfers on a per word basis. If the serial interface is implemented, this value shall be set to indicate 120 ns.

  If this field is supported, bit 1 of word 53 shall be set to one. Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in words (70:64) other than this field and the device does not support this field, the device shall return a value of zero in this field.

- **Word 66: Recommended Multiword DMA transfer cycle time**

  Word 66 of the parameter information of the IDENTIFY DEVICE command data is defined as the device recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. If the serial interface is implemented, this value shall be set to indicate 120 ns.

  If this field is supported, bit 1 of word 53 shall be set to one. Any device that supports Multiword DMA mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

  If bit 1 of word 53 is set to one because a device supports a field in words (70:64) other than this field and the device does not support this field, the device shall return a value of zero in this field.

- **Word 67: Minimum PIO transfer cycle time without flow control**

  Word 67 of the parameter information of the IDENTIFY DEVICE command data is defined as the minimum PIO transfer without IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If the serial interface is implemented, this value shall be set to indicate 120 ns.

  If this field is supported, Bit 1 of word 53 shall be set to one. Any device that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

  If bit 1 of word 53 is set to one because a device supports a field in words (70:64) other than this field and the device does not support this field, the device shall return a value of zero in this field.

- **Word 68: Minimum PIO transfer cycle time with IORDY**

  Word 68 of the parameter information of the IDENTIFY DEVICE command data is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. If the serial interface is implemented, this value shall be set to indicate 120 ns.

  If this field is supported, Bit 1 of word 53 shall be set to one.

  All devices except CFA and PCMCIA devices shall support PIO mode 3 and shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the device. The maximum value reported in this field shall be 180 to indicate support for PIO mode 3 or above.

  If bit 1 of word 53 is set to one because a device supports a field in words (70:64) other than this field and the device does not support this field, the device shall return a value of zero in this field.

- **Words 82-84: Features/command sets supported**

  Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by SSD Storage Device prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values

in these words should not be depended on by host implementers.

Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.
If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.
Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.
Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.
If bit 5 of word 82 is set to one, write cache is supported.
If bit 6 of word 82 is set to one, look-ahead is supported.
Bit 7 of word 82 shall be set to zero; release interrupt is not supported.
Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.
Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.
Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.
Bit 11 of word 82 is obsolete.
Bit 12 of word 82 shall be set to one; the SSD Storage Device supports the Write Buffer command.
Bit 13 of word 82 shall be set to one; the SSD Storage Device supports the Read Buffer command.
Bit 14 of word 82 shall be set to one; the SSD Storage Device supports the NOP command.
Bit 15 of word 82 is obsolete.

Bit 0 of word 83 shall be set to zero; the SSD Storage Device does not support the Download Microcode command.
Bit 1 of word 83 shall be set to zero; the SSD Storage Device does not support the Read DMA Queued and Write DMA Queued commands.
Bit 2 of word 83 shall be set to one; the SSD Storage Device supports the CFA feature set.
If bit 3 of word 83 is set to one, the SSD Storage Device supports the Advanced Power Management feature set.
Bit 4 of word 83 shall be set to zero; the SSD Storage Device does not support the Removable Media Status feature set.

- **Words 85-87: Features/command sets enabled**

  Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by SSD Storage Device prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

  Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.
  If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command.
  Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
  Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
  Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
  If bit 5 of word 85 is set to one, write cache is enabled.
  If bit 6 of word 85 is set to one, look-ahead is enabled.
  Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
  Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.
  Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
  Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
  Bit 11 of word 85 is obsolete.
  Bit 12 of word 85 shall be set to one; the SSD Storage Device supports the Write Buffer command.
  Bit 13 of word 85 shall be set to one; the SSD Storage Device supports the Read Buffer command.

Bit 14 of word 85 shall be set to one; the SSD Storage Device supports the NOP command.
Bit 15 of word 85 is obsolete.

Bit 0 of word 86 shall be set to zero; the SSD Storage Device does not support the Download Microcode command.
Bit 1 of word 86 shall be set to zero; the SSD Storage Device does not support the Read DMA Queued and Write DMA Queued commands.
If bit 2 of word 86 shall be set to one, the SSD Storage Device supports the CFA feature set.
If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
Bit 4 of word 86 shall be set to zero; the SSD Storage Device does not support the Removable Media Status feature set.

- **Word 88: Ultra DMA Modes Supported and Selected**

  Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported.

  Bits 15-13: Reserved
  Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
  Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
  Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
  Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
  Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
  Bits 7-5: Reserved
  Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.
  Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.
  Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.
  Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
  Bit 0: 1 = Ultra DMA mode 0 is supported

- **Word 89: Time required for Security erase unit completion**

  Word 89 specifies the time required for the Security Erase Unit command to complete. This command shall be supported on SSD Storage Device that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

- **Word 90: Time required for Enhanced security erase unit completion**

  Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.
  This command shall be supported on SSD Storage Device that support security.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

- **Word 91: Advanced power management level value**

  Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

- **Word 128: Security Status**
  Bit 8: Security Level
  If set to 1, indicates that security mode is enabled and the security level is maximum.
  If set to 0 and security mode is enabled, indicates that the security level is high.
  Bit 5: Enhanced security erase unit feature supported
  If set to 1, indicates that the Enhanced security erase unit feature set is supported.
  Bit 4: Expire
  If set to 1, indicates that the security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset.
  Bit 3: Freeze
  If set to 1, indicates that the security is Frozen.
  Bit 2: Lock
  If set to 1, indicates that the security is locked.
  Bit 1: Enable/Disable
  If set to 1, indicates that the security is enabled.
  If set to 0, indicates that the security is disabled.
  Bit 0: Capability
  If set to 1, indicates that SSD Storage Device supports security mode feature set.
  If set to 0, indicates that SSD Storage Device does not support security mode feature set.

- **Word 160: Power Requirement Description**
  This word is required for SSD Storage Device that support power mode 1.

  Bit 15: VLD
  If set to 1, indicates that this word contains a valid power requirement description.
  If set to 0, indicates that this word does not contain a power requirement description.
  Bit 14: RSV
  This bit is reserved and shall be 0.
  Bit 13: -XP
  If set to 1, indicates that the SSD Storage Device does not have Power Level 1 commands.
  If set to 0, indicates that the SSD Storage Device has Power Level 1 commands
  Bit 12: -XE
  If set to 1, indicates that Power Level 1 commands are disabled.
  If set to 0, indicates that Power Level 1 commands are enabled.
  Bit 0-11: Maximum current
  This field contains the SSD Storage Device maximum current in mA.

- **Word 162: Key Management Schemes Supported**
  Bit 0: CPRM support
  If set to 1, the device supports CPRM Scheme (Content Protection for Recordable Media)
  If set to 0, the device does not support CPRM.
  Bits 1-15 are reserved for future additional Key Management schemes.

- **Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings**
  This word describes the capabilities and current settings for CFA defined advanced timing modes using the True IDE interface.
  Notice! The use of True IDE PIO Modes 5 and above or of Multiword DMA Modes 3 and above impose significant restrictions on the implementation of the host:
  Additional Requirements for CF Advanced Timing Modes.
  There are four separate fields defined that describe support and selection of Advanced PIO timing modes and Advanced Multiword DMA timing modes. The older modes are reported in words 63 and 64.
  Word 63: Multiword DMA transfer and 6.2.1.6.19: Word 64: Advanced PIO transfer modes supported.

Bits 2-0: Advanced True IDE PIO Mode Support Indicates the maximum True IDE PIO mode supported by the card.

Value	Maximum PIO mode timing selected
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 5-3: Advanced True IDE Multiword DMA Mode Support Indicates the maximum True IDE Multiword DMA mode supported by the card.

Value	Maximum Multiword DMA timing mode supported
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 8-6: Advanced True IDE PIO Mode Selected Indicates the current True IDE PIO mode selected on the card.

Value	Current PIO timing mode selected
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

Bits 11-9: Advanced True IDE Multiword DMA Mode Selected Indicates the current True IDE Multiword DMA Mode Selected on the card.

Value	Current Multiword DMA timing mode selected
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

Bits 15-12 are reserved.

- **Word 164: CF Advanced PCMCIA I/O and Memory Timing Modes Capabilities and Settings**

  This word describes the capabilities and current settings for CFA defined advanced timing modes using the Memory and PCMCIA I/O interface.

Notice! The use of PCMCIA I/O or Memory modes that are 100ns or faster impose significant restrictions on the implementation of the host:
Additional Requirements for CF Advanced Timing Modes.

Bits 2-0: Maximum Advanced PCMCIA I/O Mode Support Indicates the maximum I/O timing mode supported by the card.

Value	Maximum PCMCIA IO timing mode Supported
0	255ns Cycle PCMCIA I/O Mode
1	120ns Cycle PCMCIA I/O Mode
2	100ns Cycle PCMCIA I/O Mode

3	80ns Cycle PCMCIA I/O Mode
4-7	Reserved

Bits 5-3: Maximum Memory timing mode supported
Indicates the Maximum Memory timing mode supported by the card.
Bits 15-6: Reserved.

Value	Maximum Memory timing mode Supported
0	250ns Cycle Memory Mode
1	120ns Cycle Memory Mode
2	100ns Cycle Memory Mode
3	80ns Cycle Memory Mode
4-7	Reserved

IDLE (E3h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h)

This command causes the device to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data.

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ DMA EXT (25h)

48-bit feature set mandatory command. Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 65536 sectors.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ MULTIPLE EXT (29h)

48-bit feature set mandatory command. This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h/21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ SECTOR(S) EXT (24h)

48-bit feature set mandatory command. This command reads 1 to 65536 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of zero requests 65536 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

READ VERIFY SECTOR(S) EXT (42h)

48-bit feature set mandatory command. This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock

result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security set Password data content

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Security level	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY UNLOCK (F2h)

This command disable LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

Security Unlock information

Word	Content		
0	Control word		
	Bit 0 Bits 1-15	Identifier Reserved	0=compare user password 1=compare master password
1-16	Password (32 bytes)		
17-255	Reserved		

SEEK (7xh)

This command is effectively a NOP command to the device although it does perform a range check.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

Features register Value and settable operating mode

Value	Function
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register.
55h	Disable read look-ahead feature
82h	Disable write cache
AAh	Enable read look-ahead feature

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

SLEEP (E6h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

SMART Function Set (B0h)

Performs different processing required for predicting device failures, according to the subcommand specified in the Features register. If the Features register contains an unsupported value, the Aborted Command error is returned. If the SMART function is disabled, any subcommand other than SMART ENABLE OPERATIONS results in the Aborted Command error.

SMART Feature Register Values			
D0h	Read Data	D5h	Read Log
D1h	Read Attribute Threshold	D6h	Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

1. If reserved size is below the Threshold, the status can be read from Cylinder register by Return Status command (DAh).

● **SMART Data Structure**

BYTE	F / V	Decription
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)

373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-397	F	Number of initial invalid block (396=MSB, 397=LSB)
398-399	V	Number of run time bad block (398=MSB, 399=LSB)
400-406	V	'SMI2242'
407-415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418-419	V	Number of child pair
420	F	Reserved
421-423	V	Average erase count
424-425	V	Number of child pair
426-428	V	Maximum erase count
429-431	V	Minimum erase count
432-445	F	Reserved
446-510	X	Vendor specific
511	V	Data structure checksum

F=the content of the byte is fixed and does not change.

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X=the content of the byte is vendor specific and may be fixed or variable.

R=the content of the byte is reserved and shall be zero.

* 4 Byte value : [MSB] [2] [1] [LSB]

STANDBY (E2h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device's buffer.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE DMA EXT (35h)

48-bit feature set mandatory command. Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE DMA FUA EXT (3Dh)

48-bit feature set mandatory command. This command provides the same function as the WRITE DMA EXT command except that regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE MULTIPLE EXT (39h)

48-bit feature set mandatory command. This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE MULTIPLE FUA EXT (CEh)

48-bit feature set mandatory command. This command provides the same functionality as the WRITE MULTIPLE EXT command except that regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported.

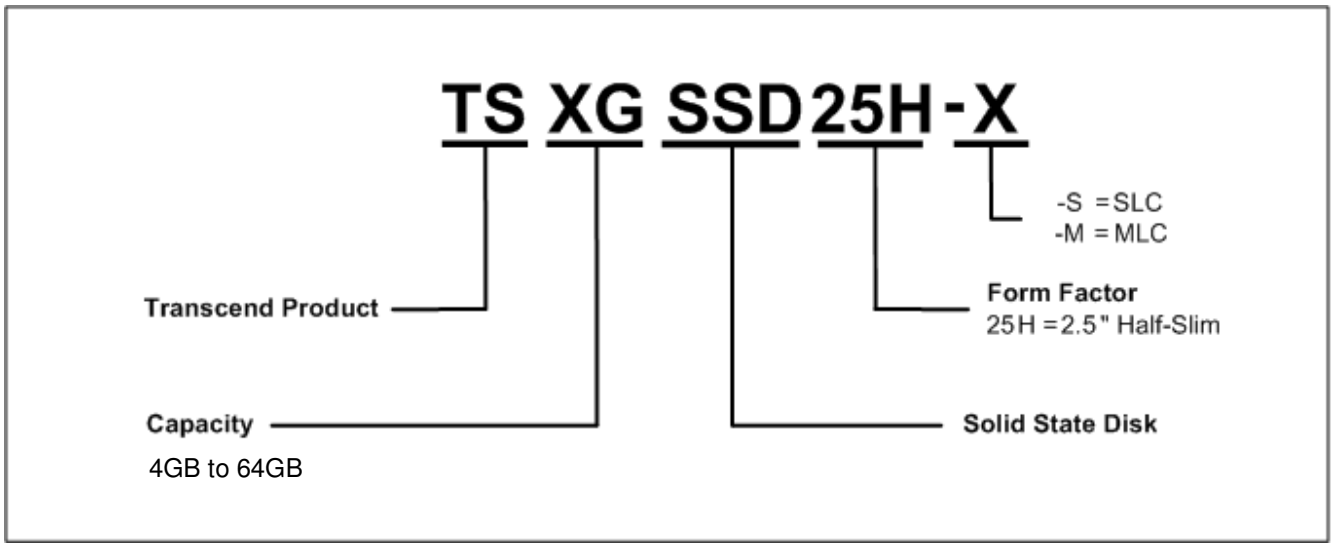
WRITE SECTOR(S) (30h/31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify “00h” to write 256 sectors.

WRITE SECTOR(S) EXT (34h)

48-bit feature set mandatory command. Write data to a specified number of sectors (1 to 65536, as specified with the Sector Count register) from the specified address. Specify “00h” to write 65536 sectors.

Ordering Information



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TAIWAN
No.70, XingZhong Rd., NeiHu Dist., Taipei, Taiwan, R.O.C
TEL +886-2-2792-8000
Fax +886-2-2793-2222
E-mail: sales@transcend.com.tw
www.transcend.com.tw

USA
Los Angeles:
E-mail: sales@transcendusa.com
Maryland:
E-mail: sales_md@transcendusa.com
www.transcendusa.com
CHINA
E-mail: sales@transcendchina.com
www.transcendchina.com
GERMANY
E-mail: vertrieb@transcend.de
www.transcend.de
HONG KONG
E-mail: sales@transcend.com.hk
www.transcendchina.com
JAPAN
E-mail: sales@transcend.co.jp
www.transcend.jp
THE NETHERLANDS
E-mail: sales@transcend.nl
www.transcend.nl
United Kingdom
E-mail: sales@transcend-uk.com
www.transcend-uk.com
KOREA
E-mail: sales@transcend.co.kr
www.transcend.co.kr