Dynamic Branch Predictor Using Machine Learning

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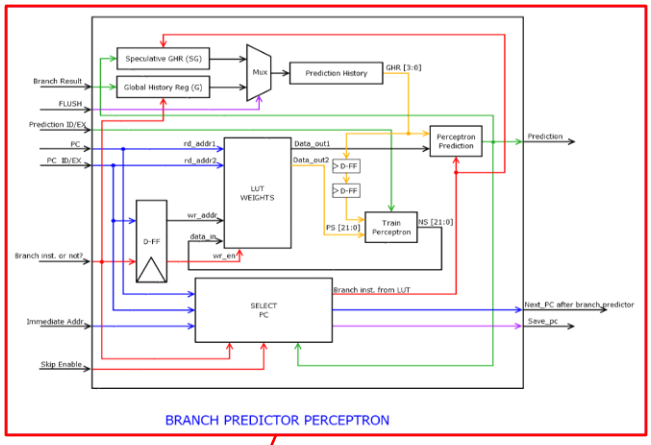
Modern CPU architectures utilize pipeline processing by staging every command to be handled in several steps such that the clock frequency can be boosted up, which will shorten the overall execution times of programs.

A branch predictor is required to maximize the successful prediction rate, thus accelerating the program execution.

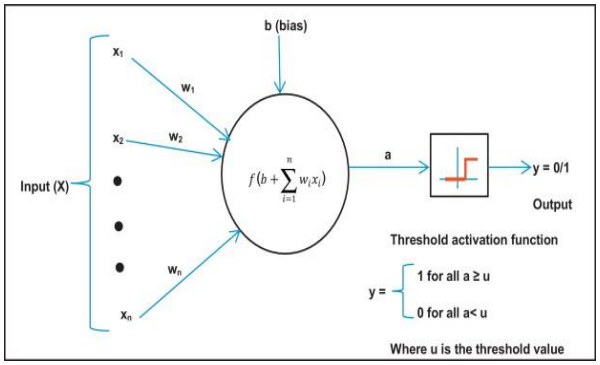
The project includes a pipelined RISC CPU (MIPS Architecture) with 2 versions of a branch prediction units:

- One using machine learning (perceptron)
- And one using state machine

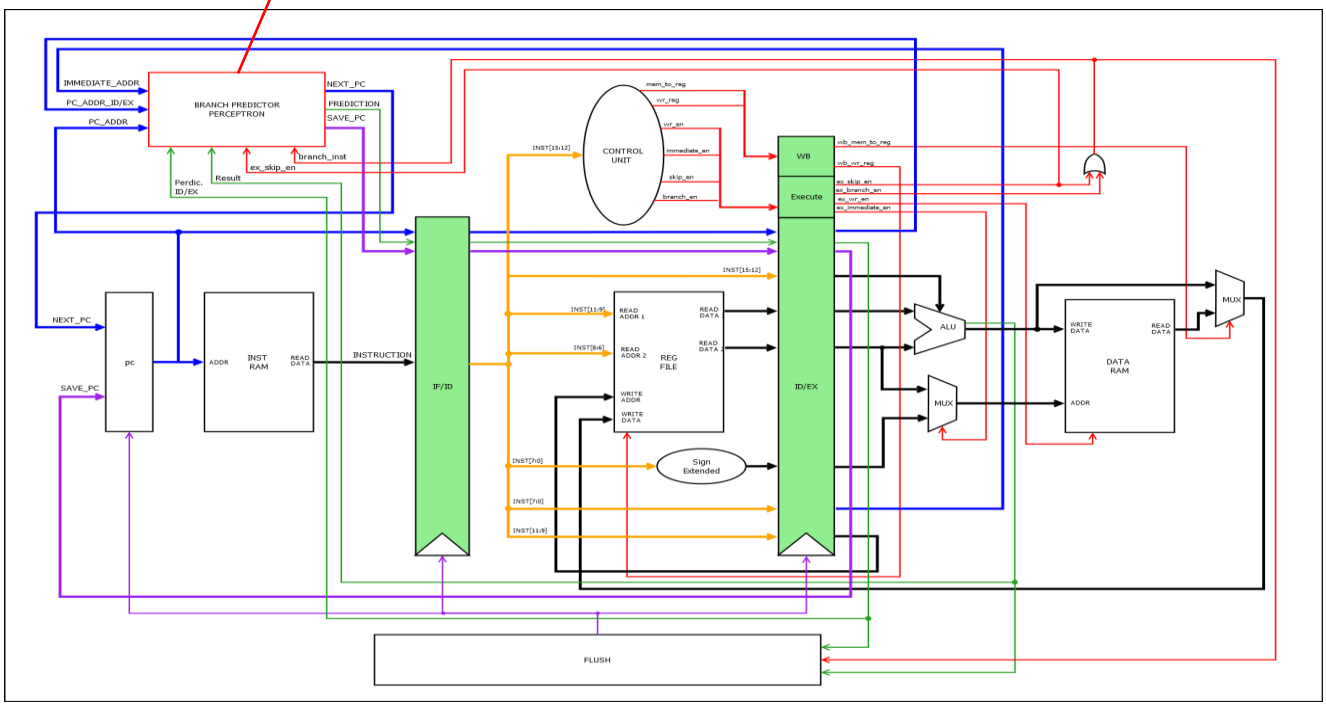
Sorting programs (as benchmarks) were running compare the solutions in terms of performance

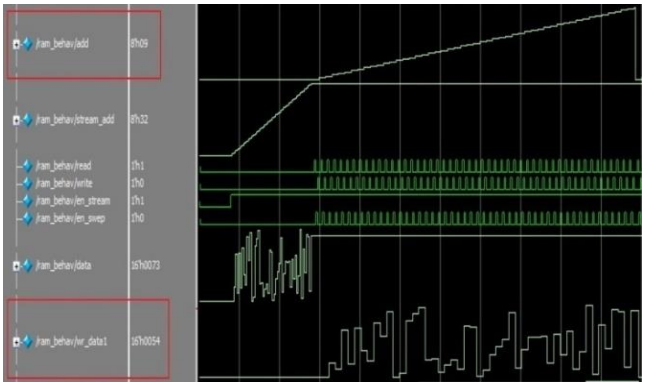


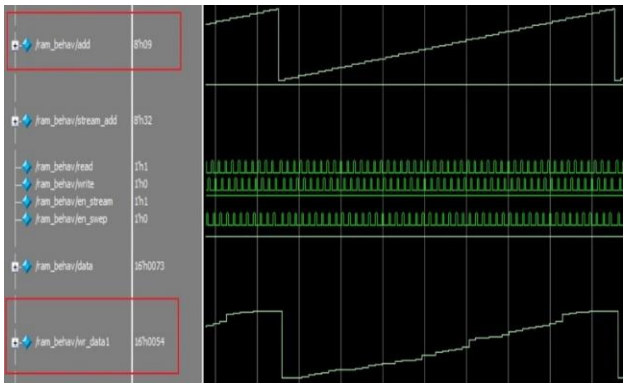
BRANCH PREDICTOR PERCEPTRON



The Perceptron Model







The Sorting – At the beginning (left) and at the end (Right)