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On the convex formulation of area for slicing floorplans

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ABSTRACT

In this paper, it is shown that the area optimization problem of a compact slicing floorplan may be formulated as a convex optimization problem when the areas of the analog components are modeled with continuous convex functions of the width (height). It is proved that the area of a compact slicing floorplan is a convex function of its width (height). The convexity is shown for the cases with and without dead (empty) space. This feature can be exploited to efficiently optimize the dimensions of layout components with multiple variants, without enumerating all possible combinations. Layout of a voltage-doubler circuit is used to quantitatively verify the proof.

1. Introduction

Reducing iterations between different design levels has been suggested by the International Technology Roadmap for Semiconductors as a major contribution towards the reduction of design cost. Towards this end, the integration of physical and electrical synthesis in one single step has been proposed, yielding the so-called layout-aware circuit synthesis approaches, such as [1]. Most successful analog circuit synthesis approaches are based on the formulation of the sizing problem as an optimization problem, commonly solved by iterative processes that imply hundreds or thousands of circuit performance evaluations. It becomes obvious that integration of physical synthesis into such circuit synthesis process is only practical if the circuit layout can be instanced very fast.

A key step of the physical synthesis process, and essential to determine layout area, is the layout floorplanning, i.e., the determination of properties and spatial relationships of a set of blocks. Lots of approaches have been reported along the three past decades for floorplanning of many (usually digital) cells in a chip [1–10].

Automatic floorplanning of analog circuits is less complex than its digital counterpart in terms of the number of blocks involved. However the complexity comes from analog constraints such as symmetry or proximity. Most reported approaches have focused on area minimization meeting some analog constraints [11,12]. However, an essential aspect in area minimization of a given analog floorplan is the variant selection problem, i.e., the determination of the specific implementation of each block among a set of possible realizations.

This paper deals with slicing floorplans. A floorplan is called slicing [2], if it is possible to recursively split it into rectangular slices by means of successive horizontal and vertical cuts. The resulting slices may be represented by a binary tree.

Area optimization on slicing analog floorplans using shape functions [3] (i.e., piece-wise linear functions built by instancing a device generator for discrete parameter values) accounting for every variant realization of component blocks was done in [1]. Enhanced shape functions were used in [4] for non-slicing floorplans. In both, shape functions were constructed by enumerating all possible solutions, therefore, a costly process if the number of variants is high. This optimization problem could be more efficiently solved if it could be formulated as a convex optimization problem. A function $f(x)$ is called convex, if it satisfies the condition:

$$f(\theta \cdot x+(1-\theta)\cdot y) \le \theta \cdot f(x)+(1-\theta)\cdot f(y) \quad (1)$$

where $\forall x, y \in \mathbf{dom} f$ and for all $\forall \theta \in \mathbf{R} : 0 \le \theta \le 1$. For continuous functions, a non-negative second derivative also indicates convexity:

$$\frac{d^2}{dx^2}[f(x)] \ge 0 \quad (2)$$

where $x \in \mathbf{dom} f$ and $f(x)$ is a twice differentiable function.

A relevant property of convex functions is that they have a single minimum, thus, if a minimum is found, it is the global minimum. Therefore, very efficient optimization algorithms can be applied and there is no risk to get stuck at local minima.

There is a one-to-many mapping from an analog device to its layout, i.e., a device may be represented by different layouts, commonly known as variants, by changing its geometrical

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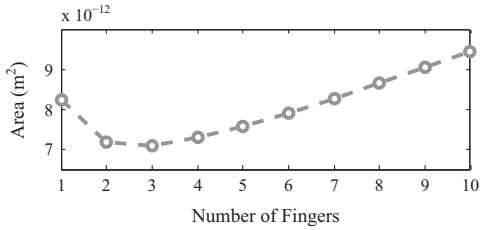

Fig. 1. The area of a transistor changes as the number of fingers *m*changes. Each data point corresponds to a different *m* value for a transistor in the UMC 0.13 μm technology with $W=5$ μm and $L=0.5$ μm.

parameters. For example, by changing the number of fingers of a transistor, different layouts may be obtained. For illustration's sake, Fig. 1 shows the area of a single transistor for different number of fingers, hence, different variants. In previous approaches to analogous problems, the transformation $\theta \leftrightarrow e^{\theta}$ was used and it was shown that after this transformation the problem of area optimization for a fixed floorplan is convex [5–7] and the transformed problem may be efficiently solved with a geometric programming solver. In these works, the area of each block was assumed to be constant for all possible variants. However, this is not the case for analog layouts as illustrated in Fig. 1. Also, these works did not consider the analog constraints. Note that symmetric placement constrains cannot be formulated in a geometric program.

A related work [8] demonstrates that the minimum area floorplanning problem is not convex and its optimal solution cannot be obtained by solving its Lagrangian dual problem. However, this is only the case if the heights of the blocks are not constrained by their widths.

We define a layout as *compact* if for a given width (height), it is not possible to obtain a shorter (thinner) layout by changing the geometrical parameters. For instance, the layout of Fig. 2a is not compact for the defined width *w*, if there exists a shorter layout, as in Fig. 2b. If the layout of Fig. 2b is the shortest possible layout, we call it a compact layout for the given width *w*. The concept of compactness is visualized in Fig. 2c, where the area of a layout and the area of a compact layout are represented by the filled region and the dark solid line, respectively.

In this paper, the width and height of a combination are denoted by *w* and *h*, respectively. The symbol ψ is used to denote the area of a combination. The area of a *h*orizontal combination, as in Fig. 3, is denoted by ψ_{H} whereas the area of a *v*ertical combination, as in Fig. 4, is denoted by ψ_{V}. Depending on the context a second index is used to denote *e*qual ($\psi_{\mathrm{H_E}}$ or $\psi_{\mathrm{V_E}}$), ma*x*imum ($\psi_{\mathrm{H_X}}$ or $\psi_{\mathrm{V_X}}$) and mi*n*imum ($\psi_{\mathrm{H_N}}$ or $\psi_{\mathrm{V_N}}$).

In this work we prove that the total area of a compact slicing floorplan is a convex function of its width (alternatively height). It is also shown that the convexity is satisfied, without applying any transformation and without any assumption on constant area. The proof makes only two assumptions on the component blocks:

- The area of a block is a convex function of its width (height), which is the case for analog devices such as resistors, capacitors and, transistors [9].
- Height $h(w)$ (alt. width $w(h)$) is a non-increasing function of the width w (alt. height h). In other words, the wider the variant is, the shorter the height is. This is also the case for analog devices [9]. Formally stating:

$$\frac{d}{dw}[h(w)] \le 0 \tag{3}$$

From this point, the width *w* is accepted as the free parameter and the height $h(w)$ is used as a continuous function of the width.

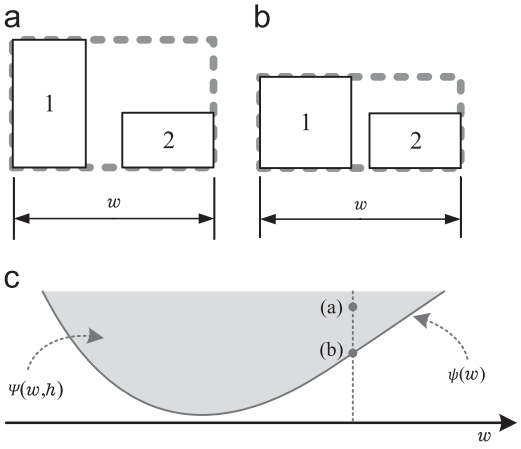

Fig. 2. Layout (a) is not compact, if it is possible to obtain a shorter layout as in (b) for a given width *w*. Points representing the areas of (a) and (b) are shown in (c). Filled region in (c) represents the area of any layout $\Psi(w,h)$ and the dark solid line represents the area of a compact layout $\psi(w)$.

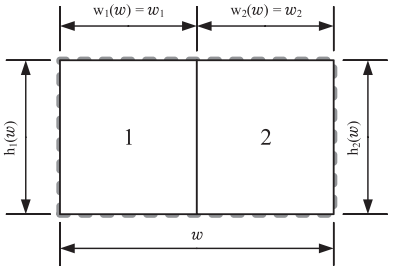

Fig. 3. Horizontal combination without dead space: heights of the blocks are equal, this configuration is denoted by $\mathrm{H_E}$ (*h*orizontal-*e*qual-height).

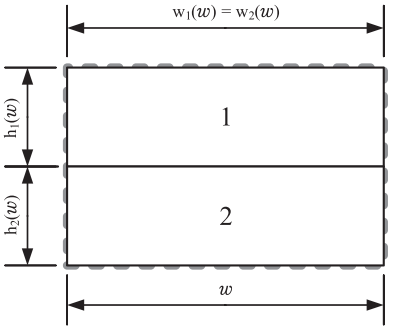

Fig. 4. Vertical combination without dead space: widths of the blocks are equal, this configuration is denoted by $\mathrm{V_E}$ (*v*ertical-*e*qual-width).

By observing a few instances of a device generator and also using the models in [9], height of a device may be easily formulated as a continuous function of its width. All the results may be obtained, without loss of generalization, if the height *h* is considered as the free parameter and the width $w(h)$ is used as a function of the height. Throughout the paper, if not explicitly stated, the dimensions of the blocks are assumed to be independent.

Our proof demonstrates that the area of a compact layout with two blocks is convex and can be extended to any compact slicing floorplan. Layouts without and with dead space are considered in Sections 2 and 3, respectively. In Section 4, our proof is generalized to any compact slicing floorplan. The proof is experimentally verified in Section 5. The conclusion is given in Section 6.

2. Convexity of slicing floorplans without dead space

In this section, we will consider the horizontal (Fig. 3) or vertical (Fig. 4) combination of two blocks without dead space.

Theorem 1. *If the area of the i-th block in Fig. 3, given as*

$$h_i(w_i)\cdot w_i \tag{4}$$

is a convex function of w_i and the height of the block $h_i(w_i)$ is a non-increasing function of w_i, then

$$\frac{d^2}{dw_i^2}[h_i(w_i)] \geq -\frac{2}{w_i}\cdot\frac{d}{dw_i}[h_i(w_i)] \tag{5}$$

is satisfied and $h_i(w_i)$ is a convex function of w_i.

Proof. Due to the fact that the area of the i-th block, given in (4), is convex in w_i, its second derivative is non-negative. Twice differentiating the expression in (4) and imposing that it is non-negative yields

$$\frac{d^2}{dw_i^2}[h_i(w_i)]\cdot w_i + 2\cdot\frac{d}{dw_i}[h_i(w_i)] \geq 0 \tag{6}$$

and rearranging the terms, Eq. (5) is obtained. As $h_i(w_i)$ is a non-increasing function of w_i, its first derivative is a non-positive number:

$$\frac{d}{dw_i}[h_i(w_i)] \leq 0 \tag{7}$$

Using the fact that the width of the i-th block w_i is a non-negative number and (7), the following expression is obtained from (5)

$$\frac{d^2}{dw_i^2}[h_i(w_i)] \geq 0 \tag{8}$$

Therefore, the height of the i-th block $h_i(w_i)$ is a convex function of its width w_i. □

Theorem 2. *Consider the horizontal combination, denoted by H_E, given in Fig. 3. If the area of each block in Fig. 3 is a convex function of its width w_i, and its height $h_i(w_i)$ is a non-increasing function of its width w_i, then the total area of the combination is a convex function of the width w.*

Proof. The area of the layout in Fig. 3 may be written as

$$\psi_{H_E}(w) = h_1(w_1(w))\cdot w = h_2(w_2(w))\cdot w \tag{9}$$

generically:

$$\psi_{H_E}(w) = h_i(w_i(w))\cdot w \tag{10}$$

The second derivative of (10) with respect to w is defined as Δ:

$$\psi''_{H_E}(w) = \Delta \tag{11}$$

$$= \frac{d^2}{dw_i^2}[h_i(w_i)]\cdot (w_i')^2\cdot w + \frac{d}{dw_i}[h_i(w_i)]\cdot (w_i''\cdot w + w_i') + \frac{d}{dw_i}[h_i(w_i)]\cdot w_i'$$

where the prime symbol (′) indicates the first derivative with respect to w. Replacing the term

$$\frac{d^2}{dw_i^2}[h_i(w_i)] \tag{12}$$

with a smaller quantity given by (5):

$$-\frac{2}{w_i}\cdot\frac{d}{dw_i}[h_i(w_i)] \tag{13}$$

δ_i is obtained, that must necessarily be smaller than Δ:

$$\Delta \geq \delta_i = -\frac{d}{dw_i}[h_i(w_i)]\cdot\zeta_i \tag{14}$$

where ζ_i is defined as

$$\zeta_i = \left(2\cdot w_i'\cdot\left(\frac{w_i'\cdot w}{w_i} - 1\right) - w_i''\cdot w\right) \tag{15}$$

Summing ζ_1 and ζ_2 and using

$$w_1 + w_2 = w \tag{16}$$

$$w_1' + w_2' = 1 \tag{17}$$

$$w_1'' + w_2'' = 0 \tag{18}$$

the following expression is obtained:

$$\zeta_1 + \zeta_2 = 2\cdot\frac{(w_1'\cdot w_2 - w_1\cdot w_2')^2}{w_1\cdot w_2} \geq 0 \tag{19}$$

This expression must be non-negative because w_1 and w_2 are non-negative. Thus, at least one of the functions, ζ_1 or ζ_2, must be non-negative. It is also known from (7) that the first derivative of the height of the i-th block with respect to its width is non-positive. Using this fact in (14), it is concluded that either δ_1 or δ_2 must be non-negative. Again from (14), Δ is non-negative which is defined in (11) as the second derivative of the area ψ_{H_E}.

In conclusion, ψ''_{H_E} is always positive, thus the total area is a convex function of the width w. □

Theorem 3. *Consider the vertical combination, denoted by V_E, given in Fig. 4. If the area of each block is a convex function of its width, then the total area of the layout is convex.*

Proof. The total area of the layout may be formulated as

$$\psi_{V_E}(w) = h_1(w)\cdot w + h_2(w)\cdot w \tag{20}$$

It is known that the area of each block in Fig. 4 is a convex function of its width. But it is also known that the width of each block is the width of the layout. Thus, the products in (20) are convex in w. It is also known that a positive weighted sum of convex functions is also a convex function. Thus, the expression in (20) is a convex function of w. □

3. Convexity of slicing floorplans with dead space

When the i-th block in Fig. 3 reaches its dimensional limits:

$$w_{i_{min}} \leq w_i \leq w_{i_{max}} \tag{21}$$

some dead space is going to emerge. The possible cases are shown in Fig. 5, where the layouts are considered to be compact for a given width w.

Theorem 4. *For the layouts given in Fig. 5, the total area is a convex function of the width w.*

Proof. For the cases in Fig. 5a and in Fig. 5b, the height of the layout reaches its minimum value $h_{1_{min}}$ and does not decrease if w increases. Formally, the area ψ_{H_N} is

$$\psi_{H_N}(w) = \psi_{H_{N1}}(w) = \psi_{H_{N2}}(w) = h_{1_{min}}\cdot w \tag{22}$$

This expression is a linear function of w, thus the area is a convex function of w. For the case in Fig. 5c, the area is

$$\overline{\psi}_{H_{X1}}(w_2) = h_2(w_2)\cdot w_{1_{min}} + h_2(w_2)\cdot w_2 \tag{23}$$

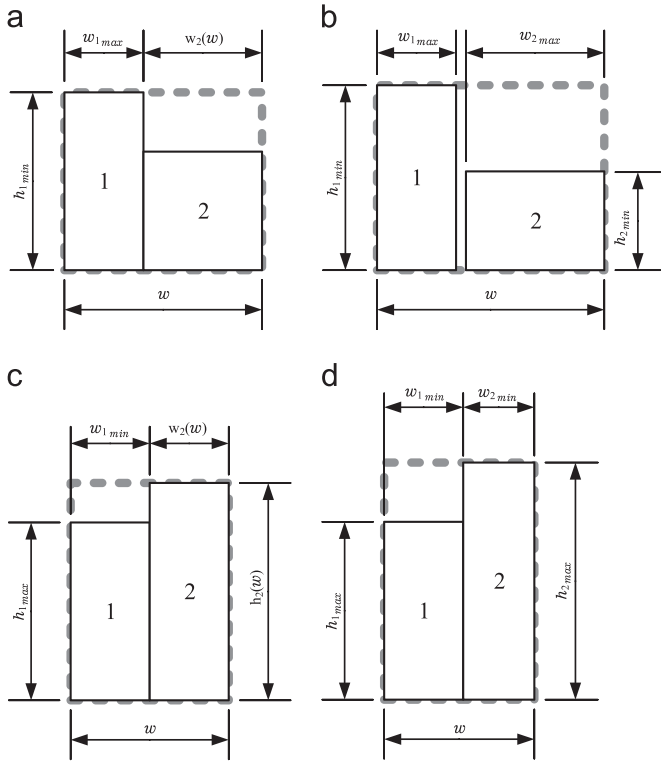

Fig. 5. Horizontal combination with dead space. (a) One of the blocks reaches its minimum height, this combination is denoted by H_{N1} (*h*orizontal-mi*n*imum-height-1). (b) Both blocks reach their minimum height, denoted by H_{N2} (*h*orizontal-mi*n*imum-height-2). (c) One of the blocks reaches its maximum height, this combination is denoted by H_{X1} (*h*orizontal-ma*x*imum-height-1). (d) Both blocks reach their maximum height, denoted by H_{X2} (*h*orizontal-maximum-height-2).

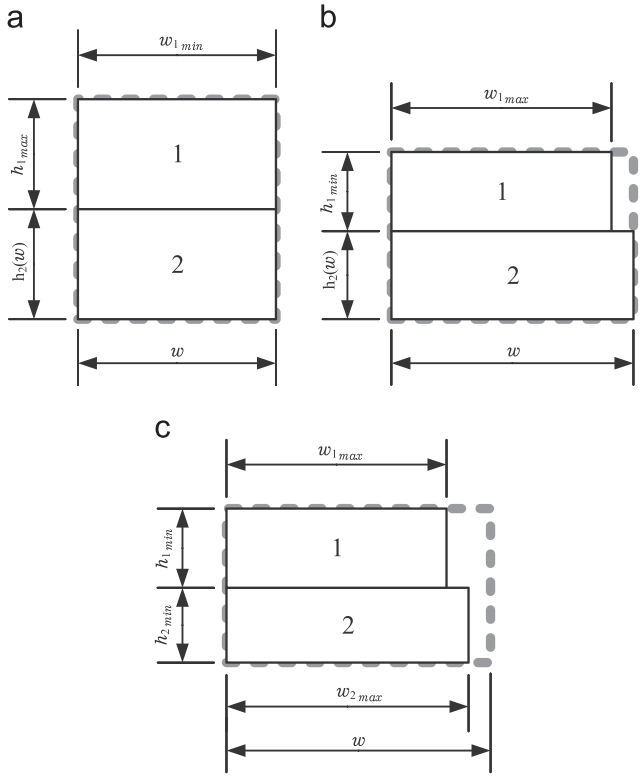

Fig. 6. Vertical combination. (a) One of the blocks reaches its minimum width. In this case there is no dead space. This combination is denoted by V_{N1} (vertical-mi*n*imum-width-1). (b) One of the blocks reaches its maximum width, denoted by V_{X1} (vertical-ma*x*imum-width-1). (c) Both blocks reach their maximum width, denoted by V_{X2} (*v*ertical-maximum-width-2).

where $\overline{\psi}_{H_{X1}}$ is a function of w_2. Noting that the term $h_2(w_2)$ is known to be convex from Theorem 1 and $w_{1_{min}}$ is a positive constant, the first and the second products in the sum are convex functions of w_2. Thus, $\overline{\psi}_{H_{X1}}$ is a convex function of w_2. The area of the combination given in Fig. 5c:

$$\psi_{H_{X1}}(w) = \overline{\psi}_{H_{X1}}(w - w_{1_{min}}) \tag{24}$$

is a shifted version of $\overline{\psi}_{H_{X1}}$, and if one is convex, the other one is also convex. Finally, the case in Fig. 5d is the limit case: w is not allowed to have values smaller than $w_{1_{min}} + w_{2_{min}}$, and the area of the combination is a constant:

$$\psi_{H_{X2}} = \psi_{H_{X1}}(w_{1_{min}} + w_{2_{min}}) \quad \square \tag{25}$$

Vertical combinations, other than the one in Fig. 4, are generalized in Fig. 6, where each one is compact for a given w.

Theorem 5. *For the layouts given in Fig. 6, the total area is a convex function of the width w.*

Proof. In Fig. 6a, the narrowest possible case is given. In this case there is no dead space and convexity is already stated in Theorem 3:

$$\psi_{V_{N1}} = \psi_{V_E}(w_{1_{min}}) \tag{26}$$

For the case of Fig. 6b, the total area is

$$\psi_{V_{X1}}(w) = h_{1_{min}} \cdot w + h_2(w) \cdot w \tag{27}$$

where the expression is a sum of two convex functions of w. The first product in the sum is a linear function of w and the second term is convex by the initial assumptions listed in Section 1. Considering the case of Fig. 6c, the area may be formulated as

$$\psi_{V_{X2}}(w) = (h_{1_{min}} + h_{2_{min}}) \cdot w \tag{28}$$

where this expression is linear, thus, a convex function of w. $\square$

4. Convexity of any slicing floorplan

In Sections 2 and 3, the convexity of different cases has been analyzed. The following theorem proves the convexity when all those cases are considered together.

Theorem 6. *The area of the horizontal combination may be formulated as*

$$\psi_H(w) = \max(\tilde{\psi}_{H_{X1}}, \tilde{\psi}_{H_E}, \tilde{\psi}_{H_{N1}}) \tag{29}$$

and, similarly, the area of the vertical combination may be formulated as

$$\psi_V(w) = \max(\tilde{\psi}_{V_E}, \tilde{\psi}_{V_{X1}}, \tilde{\psi}_{V_{X2}}) \tag{30}$$

where $\tilde{\psi}$ is a function of the width w and is obtained through extending $\psi(w)$, which is defined in the range $[w_{min}, w_{max}]$, linearly in the ranges $(0, w_{min})$ and (w_{max}, ∞) such that for each of the points w_{min} and w_{max} the first derivative of $\tilde{\psi}(w)$ both from left and right is the same.

The area of both the horizontal combination $\psi_H(w)$ and the vertical combination $\psi_V(w)$ are convex functions of the width w.

Proof. If $\psi(w)$ is constructed by linearly extending the convex function $\tilde{\psi}(w)$ as described in the theorem, then the function $\psi(w)$ is also going to be convex. And if the area of the horizontal and vertical combinations may be formulated as given in (29) and (30), respectively, both the areas of the horizontal and the vertical compositions are convex in w, as the maximum of several convex

functions is also convex. The following discussion shows that the area of horizontal and vertical combinations may be represented by the formulations given in (29) and (30), respectively.

Considering the illustration given in Fig. 7a and the definitions given in (3), (9), (22) and (24) the following conclusions may be derived:

$$\frac{d}{dw}\psi_{H_{X1}}\Big|_{w=w_I} \le \frac{d}{dw}\psi_{H_E}\Big|_{w=w_I} \tag{31}$$

$$\frac{d}{dw}\psi_{H_E}\Big|_{w=w_{II}} \le \frac{d}{dw}\psi_{H_{N1}}\Big|_{w=w_{II}} \tag{32}$$

Similarly, considering the illustration given in Fig. 7b and the definitions given in (3), (20), (27) and (28) the following conclusions may be derived:

$$\frac{d}{dw}\psi_{V_E}\Big|_{w=w_I} \le \frac{d}{dw}\psi_{V_{X1}}\Big|_{w=w_I} \tag{33}$$

$$\frac{d}{dw}\psi_{V_{X1}}\Big|_{w=w_{II}} \le \frac{d}{dw}\psi_{V_{X2}}\Big|_{w=w_{II}} \tag{34}$$

Thus, the *max*function in (29) and (30) selects the correct functions for each region as indicted in Fig. 7. This proves that the horizontal and the vertical combinations may be formulated with (29) and (30), respectively. □

The convexity of horizontal and vertical combinations has been proven. Following theorem generalizes the proof to any slicing floorplan, composed of horizontal and vertical combinations.

Theorem 7. *The area of a compact slicing floorplan is a convex function of its width w.*

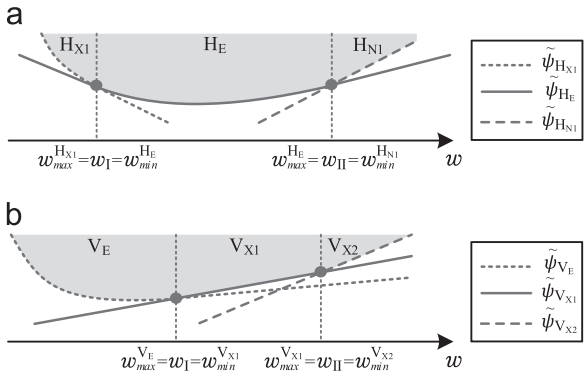

Fig. 7. The area as a function of the width w may be obtained by taking the maximum of the extended functions. (a) For a horizontal combination, the area ψ_H is the maximum of the functions: $\tilde{\psi}_{H_{X1}}, \tilde{\psi}_{H_E}, \tilde{\psi}_{H_{N1}}$. (b) For a vertical combination, the area ψ_V is the maximum of the functions: $\tilde{\psi}_{V_E}, \tilde{\psi}_{V_{X1}}, \tilde{\psi}_{V_{X2}}$.

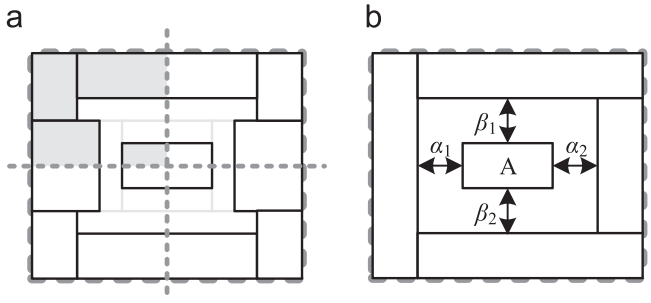

Fig. 8. (a) A combination composed of symmetric blocks. (b) Proximity constraints between the block A and its neighbors are shown.

Proof. As defined in Section 1, a compact layout has the shortest possible height for a given width w. Thus, the height $h(w)$ of any layout combination is a non-increasing function of the width w, as stated in (3). In Theorem 6, the area of horizontal and vertical combinations, ψ_{H_E} and ψ_{V_E}, are proven to be convex in w. Thus, any combination satisfies the conditions listed in Section 1. It is concluded that a horizontal or a vertical combination also satisfies the mentioned conditions. Due to the hierarchy of slicing floorplans, area of any compact slicing floorplan is convex in w. □

Because of the fact that dimensions of symmetric blocks depend on each other, this case is not covered in Theorem 7. Symmetric placement and proximity constraints are covered in the following theorem.

Theorem 8. *The area of a compact slicing floorplan with symmetry constraint, in a combination composed of symmetric blocks, and with proximity constraint, between a block and its neighbors, is a convex function of its width w.*

Proof. A symmetric slicing floorplan is shown in Fig. 8a, where the symmetry axes are indicated by the dashed lines. If a horizontal or (and) a vertical axis passes through a block, it cuts the area of this block into two (four) equal sub-blocks. The area of each sub-block, as a function of its width, may be obtained by scaling the area of the original block, convex by the assumption listed in Section 1, with a positive constant. Thus, the area of the sub-block is convex in its width and satisfy the listed conditions. As a result, the symmetry axes partition the layout into four quarters and each is composed of blocks and sub-blocks satisfying the conditions in Section 1. In Fig. 8a, the blocks and sub-blocks in the upper-left quarter are indicated with gray regions. Theorem 7 states that the area of a quarter is convex in its width and its height is a non-increasing functions of its width. The function for the total area may be obtained by scaling the function for the area of a quarter. Thus, the total area of the layout, dashed rectangle in Fig. 8a, is convex in its width. If the width (height) of a quarter increases, the width (height) of the layout also increases. It may be concluded that the height of the layout is a non-increasing function of its width as stated in (3). In conclusion, a combination composed of symmetric blocks may be considered as a super block in a compact layout and Theorem 7 states the convexity.

A layout with proximity constraints is shown in Fig. 8b, where the block A is constrained. Let us replace the block A with a larger block $\tilde{A}$ which satisfies the following:

$$w = w_A + \alpha \tag{35}$$

$$h(w) = h_A(w_A) + \beta \tag{36}$$

where α and β are defined as

$$\alpha = \alpha_1 + \alpha_2 \tag{37}$$

$$\beta = \beta_1 + \beta_2 \tag{38}$$

The area of the larger block is

$$\begin{aligned}\psi(w) = {} & (w-\alpha)\cdot h_A(w-\alpha) \\ & + (w-\alpha)\cdot\beta \\ & + \alpha\cdot h_A(w-\alpha) \\ & + \alpha\cdot\beta\end{aligned} \tag{39}$$

The first product in the sum resembles (24) and is convex in w. The second product in (39) is a linear term and it also convex in w. The third product is the scaled and shifted version of $h_A(w_A)$, proven to be convex in Theorem 1, thus third product is also convex. As a result, area of the larger block $\tilde{A}$ is convex in w. If the width (height) of the block A increases, the width (height) of the block $\tilde{A}$ also increases. Thus, the block $\tilde{A}$ satisfies the conditions listed in Section 1 and Theorem 7 states the convexity of the layout where

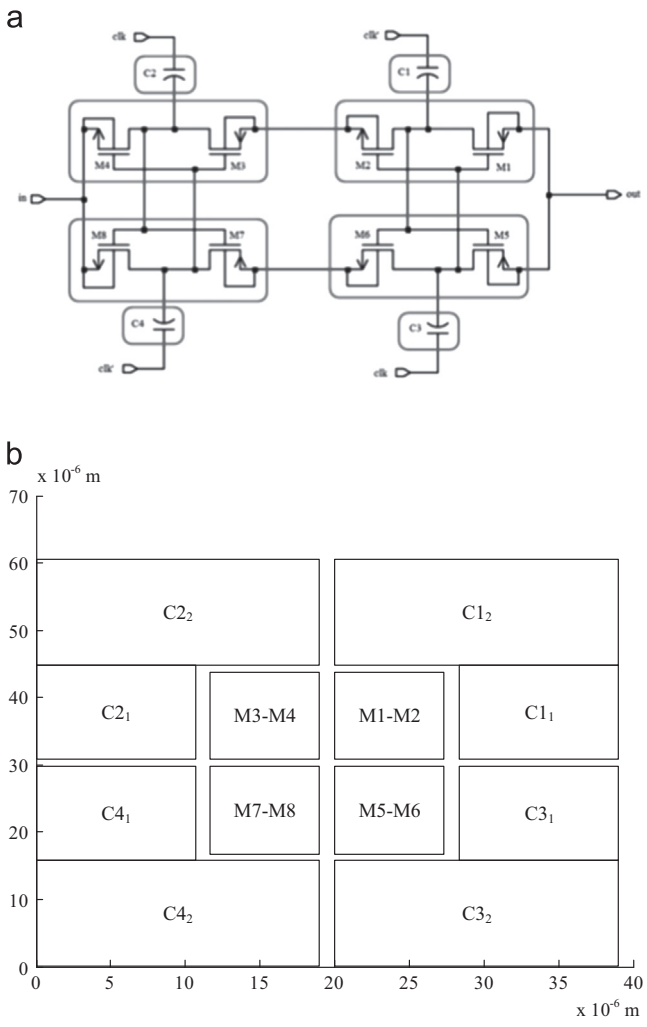

Fig. 9. (a) Schematic of a voltage doubler circuit. (b) Layout of the circuit in (a) where the area is minimized and, proximity and symmetry constraints are applied.

Table 1
Enumeration vs. optimization.

Method	Time (s)	Area ($\times 10^{-9}$ m^2)
Enumeration	0.459	2.36
Optimization*	0.081	2.36

The experiments are done on an Intel i7-3610QM processor with 6 GByte RAM.

* Interior point algorithm and branch and bound method are used.

the block A is replaced with the block $\tilde{A}$. This concludes that the area of the layout is convex if there exists proximity constraints between a block and its neighbors. □

All the previous results also apply if the height $h$is chosen as the free parameter rather than the width w.

5. Experimental verification

The proof of convexity, for a slicing floorplan, is verified on the layout of the voltage doubler circuit given in Fig. 9a. A floorplan with 2-D symmetry is used and the floorplan with the minimum area is given in Fig. 9b. The capacitors C1, C2, C3 and C4 are L-shaped and symmetrically placed in horizontal and vertical directions, also the transistor pairs M1–M2, M3–M4, M5–M6 and M7–M8 are symmetrically placed. Also a proximity constraint is added which forces the components to be separated at least 1 μm.

First, the area of the floorplan of the circuit in Fig. 9a is minimized by enumeration, where the number of fingers of the transistors is enumerated from 2 to 20 and the widths of the capacitors are enumerated from 5 μm to 50 μm in steps of 50 nm. Then, the area of the layout is assumed to be a convex function and a convex integer programming solver is used where the number of fingers is forced to have integer values and bounded in the range [2, 20], and the width of the capacitors are forced to be in the range [5 μm, 50 μm]. The solver makes use of the interior point algorithm from the MATLAB optimization toolbox [13] and the branch and bound methodology [14]. The results, area and processing time, obtained for enumeration and convex optimization methods are listed in Table 1. Both enumeration and convex optimization found the same solution, where the number of transistor fingers and widths of the capacitors is the same. The optimization method is approximately 6 times faster than the enumeration and the resulting dimensions of the components are shown in Fig. 9b. These results support that the solution space is convex and the optimal dimensions of the blocks may be efficiently found with a convex optimizer.

Although this problem cannot be solved with the approach in [3] because it cannot handle the symmetry constraints, we will relax these constraints to enable a computation time comparison. A shape function is constructed and the area of the floorplan of the circuit in Fig. 9a is minimized as described in [3]. The optimization lasts 0.096 s. Comparison with the approach described in [6] requires not only relaxing the symmetric placement constraints, but also the areas of the components are fixed for all variants and a geometric program is constructed. The tool “ggplab” [15] is used to solve the problem and the optimization lasts 0.147 s. Note that the results for these methods, that based on the shape function and that based on geometric programming, are reported for the sake of completeness. These methods are applied to the relaxed problems, thus, resulting layouts are not realistic and/or do not meet the constraints.

All the experiments were done in the MATLAB [13] environment on an Intel i7-3610QM processor with 6 GByte RAM.

6. Conclusion

Convex functions have a single minimum and their optimal solution may be found very efficiently. In this paper, it is proven that the area of a compact slicing floorplan is a convex function of its width (height), where the area of each component is formulated as a continuous convex function. Only two assumptions are made on these functions, which are readily satisfied by analog components, such as transistors, capacitors and resistors. Possible cases are considered, with and without dead space. The proof is done without making any transformations and any assumption on constant area. The convexity of floorplans with symmetry and proximity constraints is also proven. Making use of this proof, it is possible to efficiently optimize the area of slicing floorplans using a convex optimizer. A convex problem, with integer variables, may be solved optimally with an integer convex optimizer, however if a near optimal solution is acceptable, a continuous convex optimizer may be used which is faster. The convexity proof is also justified with quantitative results. This proof will especially impact floorplan optimization of analog layouts containing several capacitor blocks with many possible variants.

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