



VGA Card

VLSI PROJECT

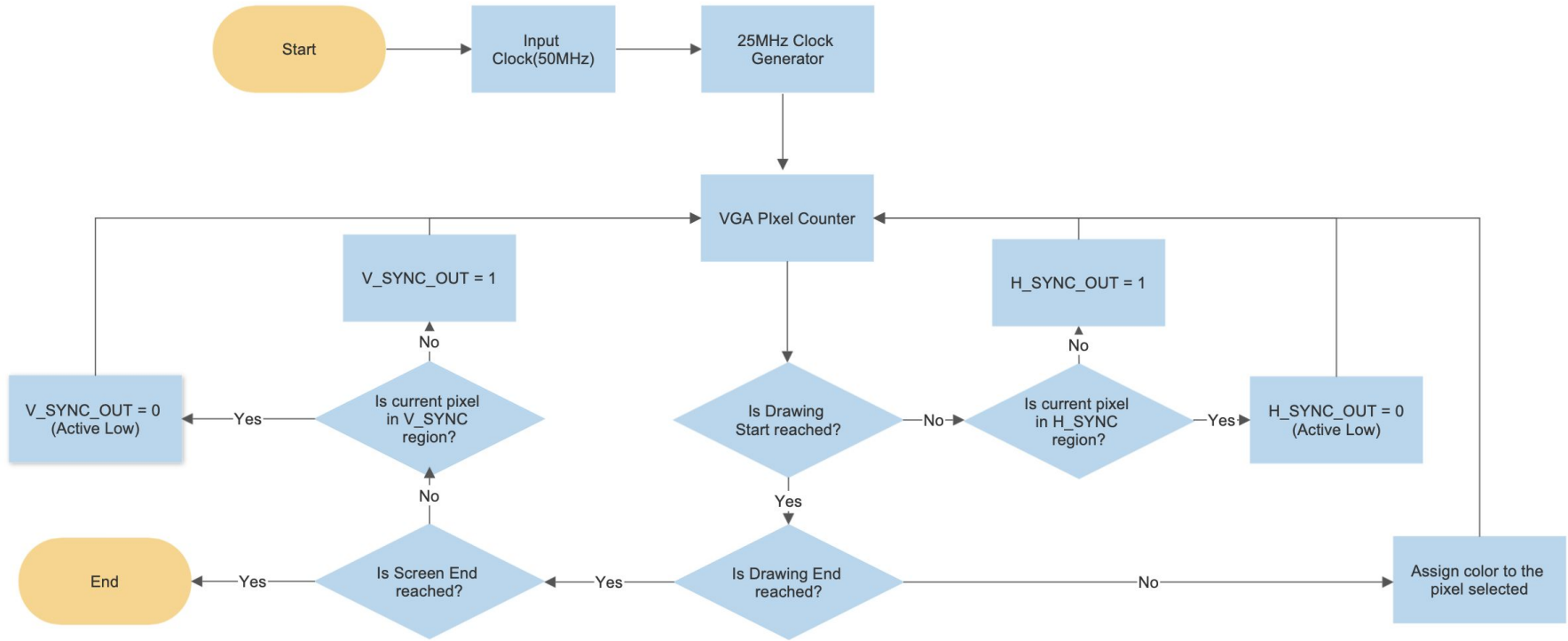
Ahish Deshpande - 2018102022

Shivansh - 2018102007

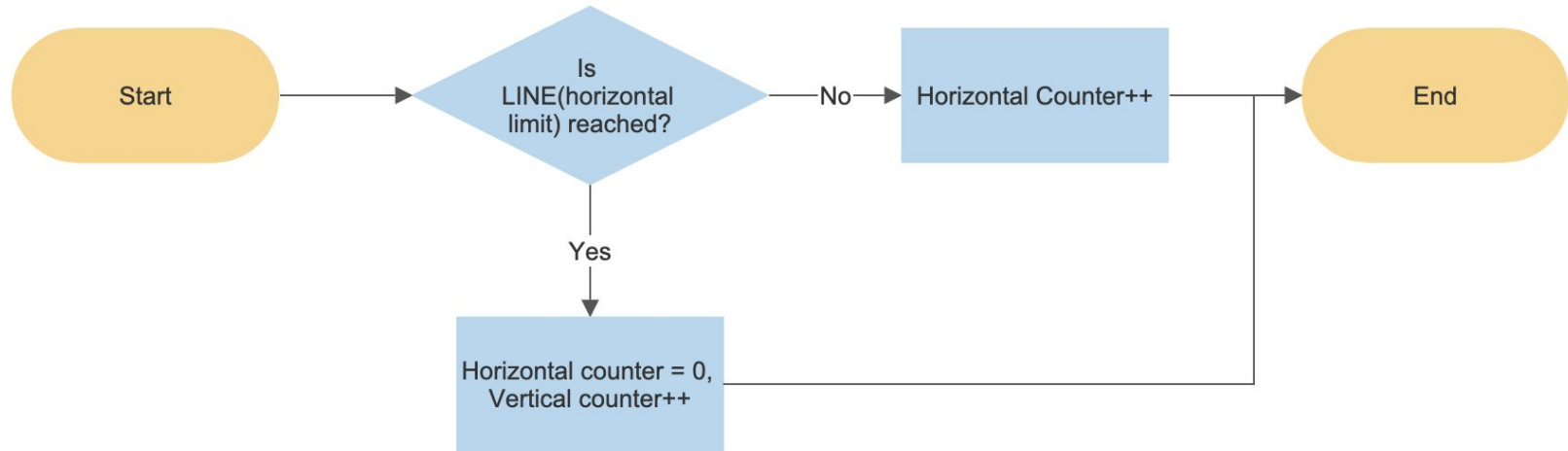
DESIGN



DESIGN : Overall Block Diagram



DESIGN : Pixel Counter Block Diagram



Flow that will be used

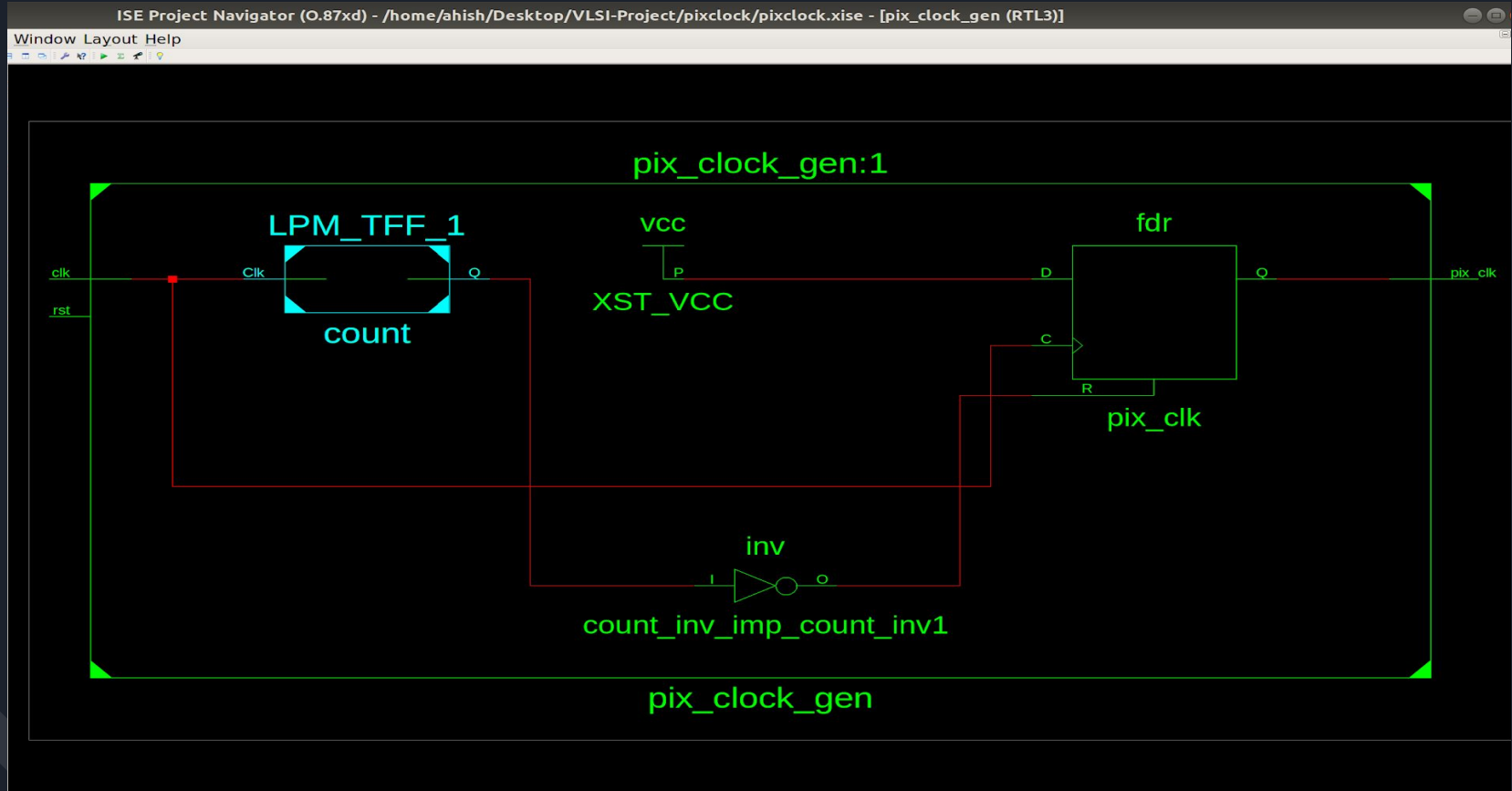
We have implemented our project using the FPGA flow and the ASIC flow.



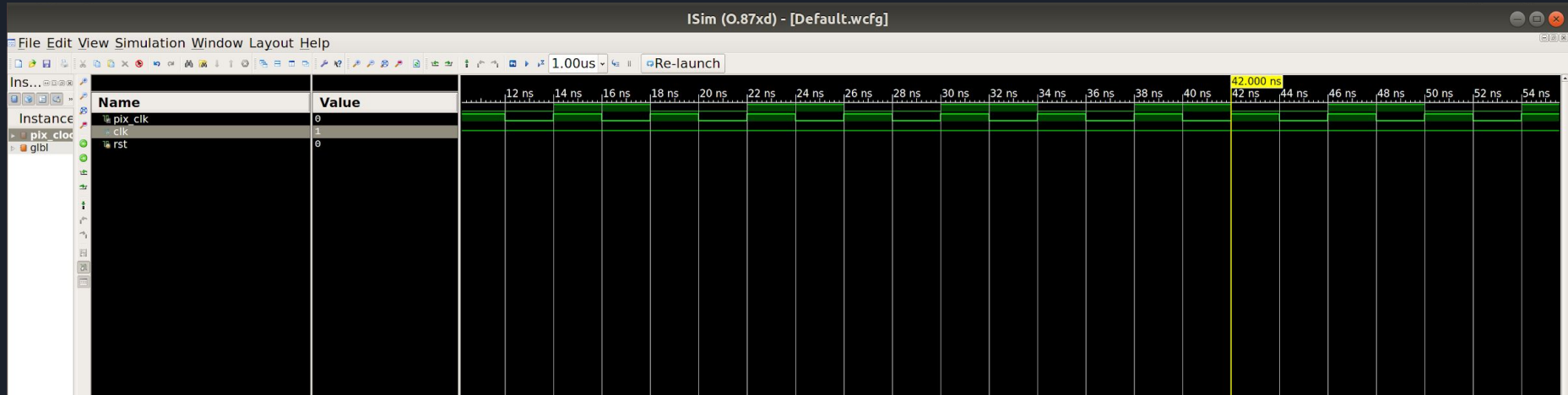
Illustrative Reports & Diagrams

The background features a series of dark gray, three-dimensional rectangular planes that recede into the distance, creating a sense of depth. A bright green parallelogram and a blue parallelogram are positioned on these planes, adding a pop of color to the monochromatic scheme.

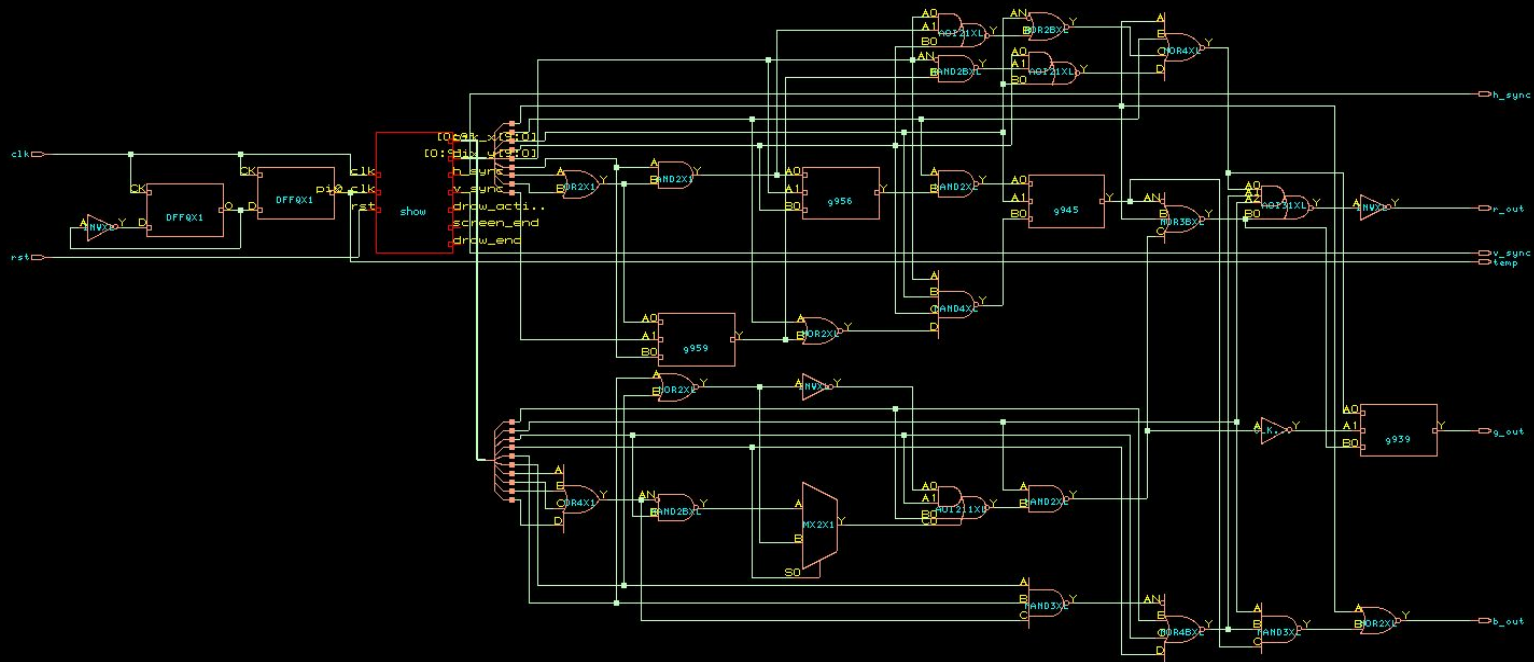
PIXEL CLOCK : Xilinx RTL Schematic



PIXEL CLOCK : Xilinx Timing Diagram



MAIN BLOCK : Genus RTL Schematic



The screenshot displays the ISim (0.87xd) - [Default.wcfg] window. The top menu bar includes File, Edit, View, Simulation, Window, Layout, and Help. Below the menu is a toolbar with various icons for file operations, simulation control, and viewing options. The main workspace is divided into three panes:

- Left Pane:** A list of signals with their current values.

Name	Value
h_sync	1
v_sync	1
r_out	0
g_out	0
b_out	0
temp	1
clk	0
rst	0
- Center Pane:** A timing diagram showing waveforms for the listed signals over a time range from 0 us to 1,000.000000 us. The time scale is set to 1.00us. The waveforms are green on a black background.
- Right Pane:** A console window showing the following text:

This is a Lite version of ISim.
WARNING: File "/home/shivansh/vlsi-project/final/screen_design.v" Line 56. For instance uut/show/, width 10 of formal port pix_y is not equal to width 9 of actual signal pix_y.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>

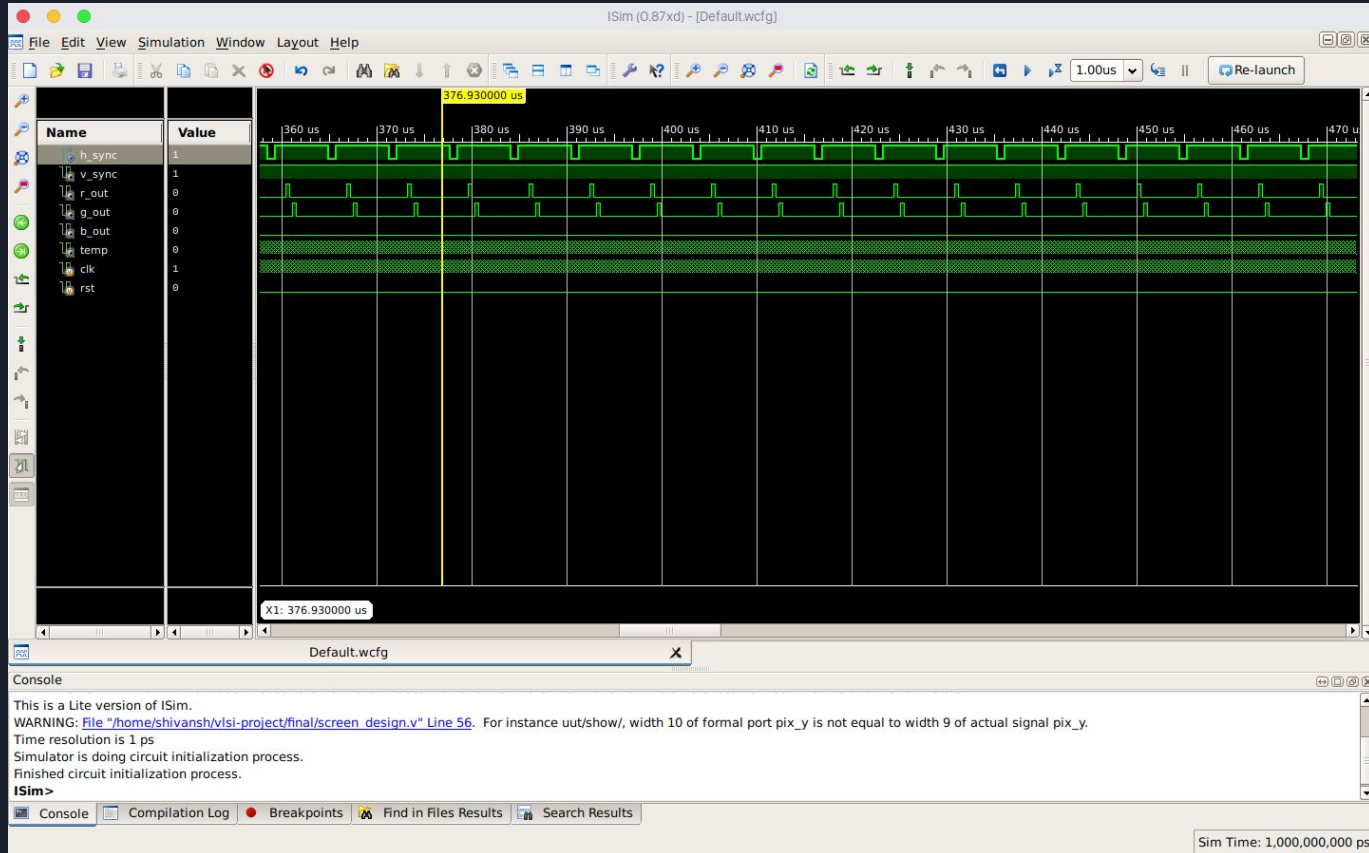
At the bottom, there is a status bar showing "Sim Time: 1,000,000,000 ps".

This is a Lite version of ISim.
WARNING: [File "home/shivansh/vlsi-project/final/screen_design.v" Line 56](#). For instance uut/show/, width 10 of formal port pix_y is not equal to width 9 of actual signal pix_y.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

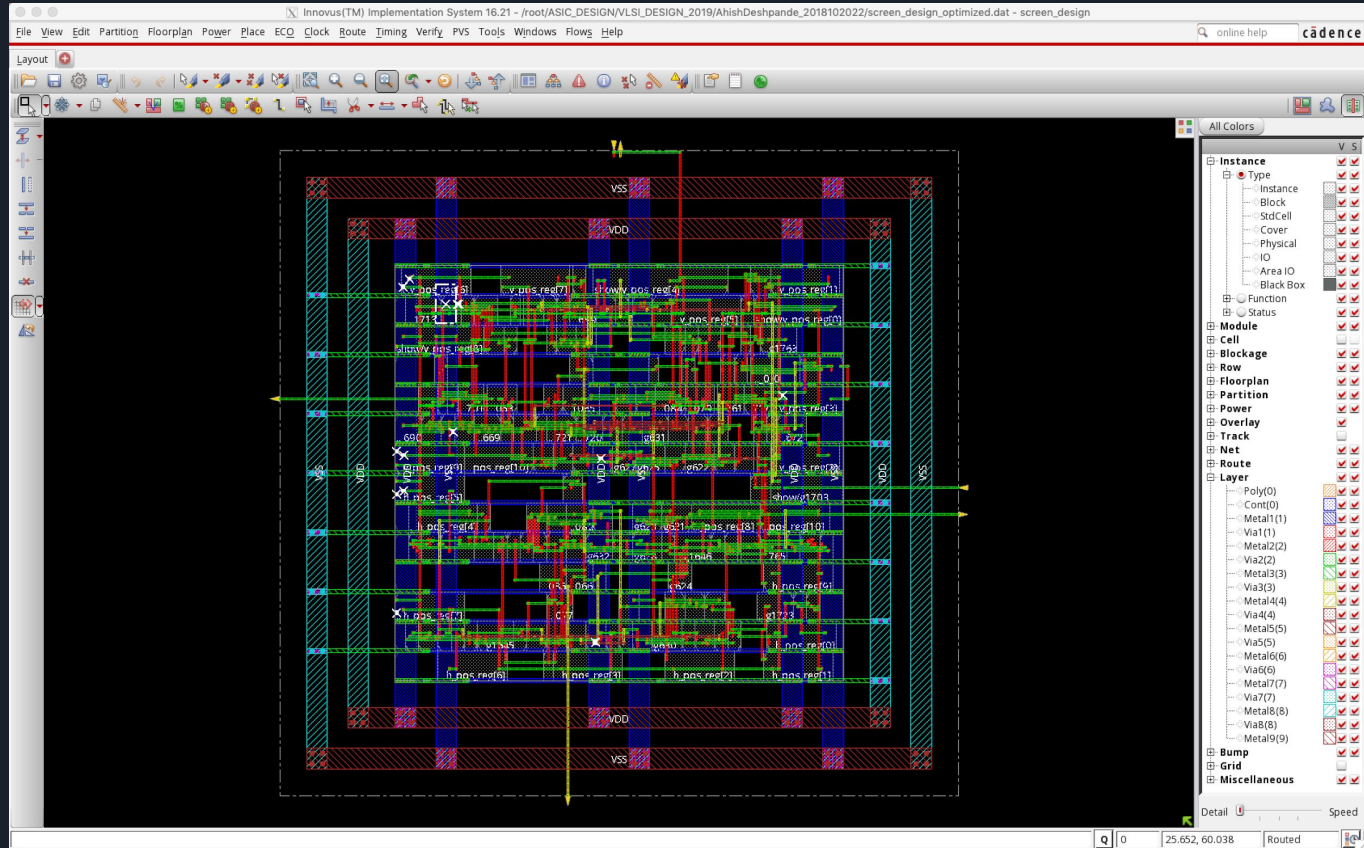
 Console
 Compilation Log
 Breakpoints
 Find in Files Results
 Search Results

Sim Time: 1,000,000,000 ps

MAIN BLOCK : Xilinx Timing Diagram- II



INNOVUS LAYOUT

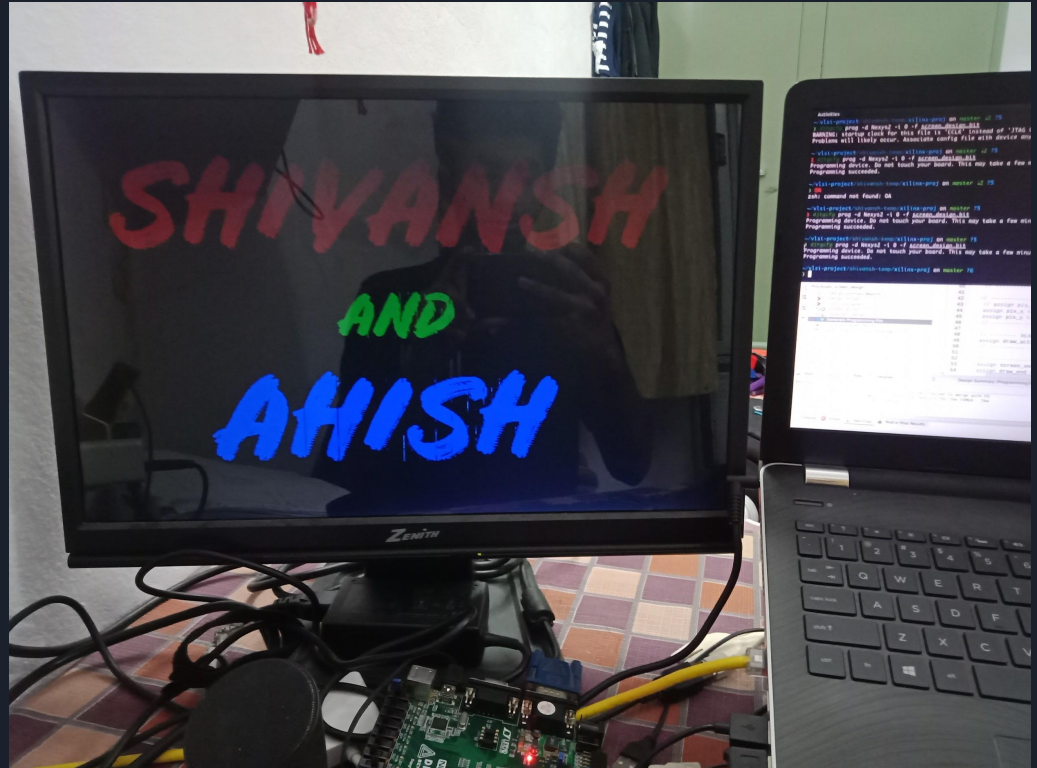
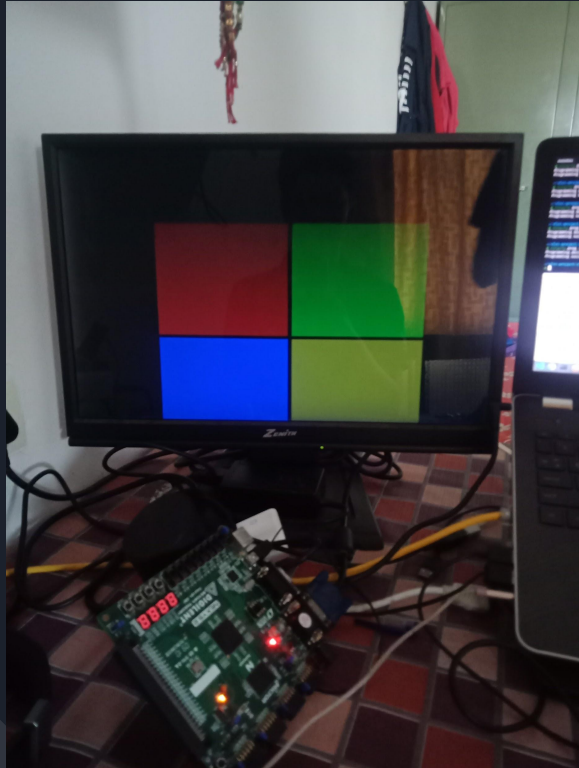


PROGRESS

(As of 17 Nov' 2019)

We are now able to generate bitmap of an image and display it on the monitor using our VGA card.

INITIAL IMAGES DISPLAYED



the Biggest Bitmaps processed yet!



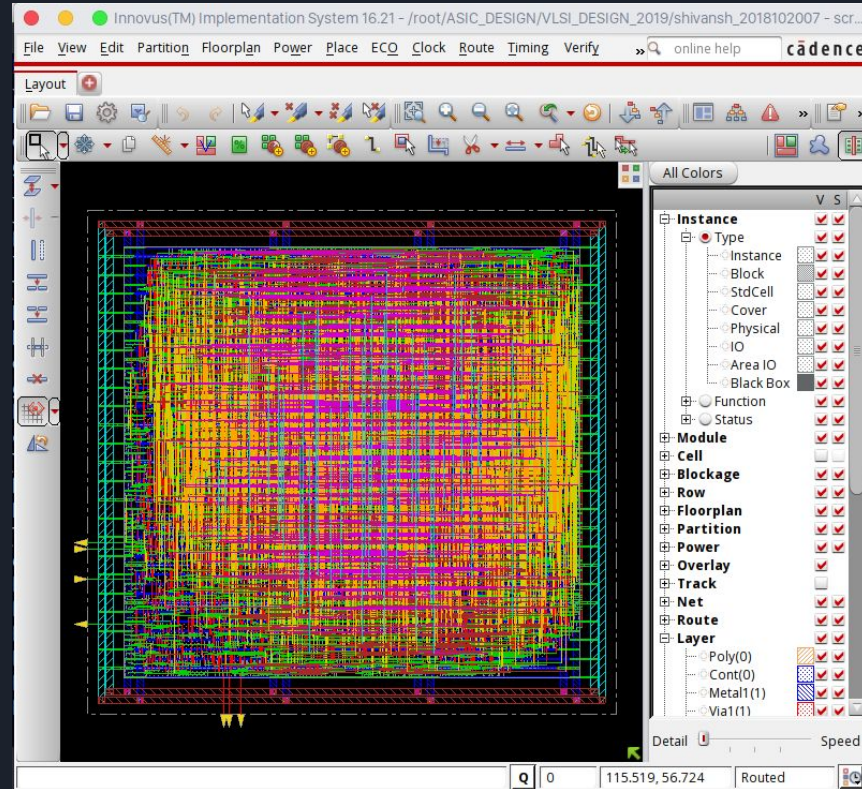
the Biggest Bitmaps processed yet!



the Biggest Bitmaps processed yet!



Innovus Layout of the circuit used for processing the previous image



RESULTS

& Comparison with Unoptimized
Project



PRE-OPTIMIZATION REPORTS

TOOL USED	AREA(μm^2)
GENUS	$1069 + 981 = 2050$
INNOVUS	$1069.4997 + 980.9424 = 2050.3921$

TOOL USED	POWER
GENUS	0.1965mW
INNOVUS	0.1493mW

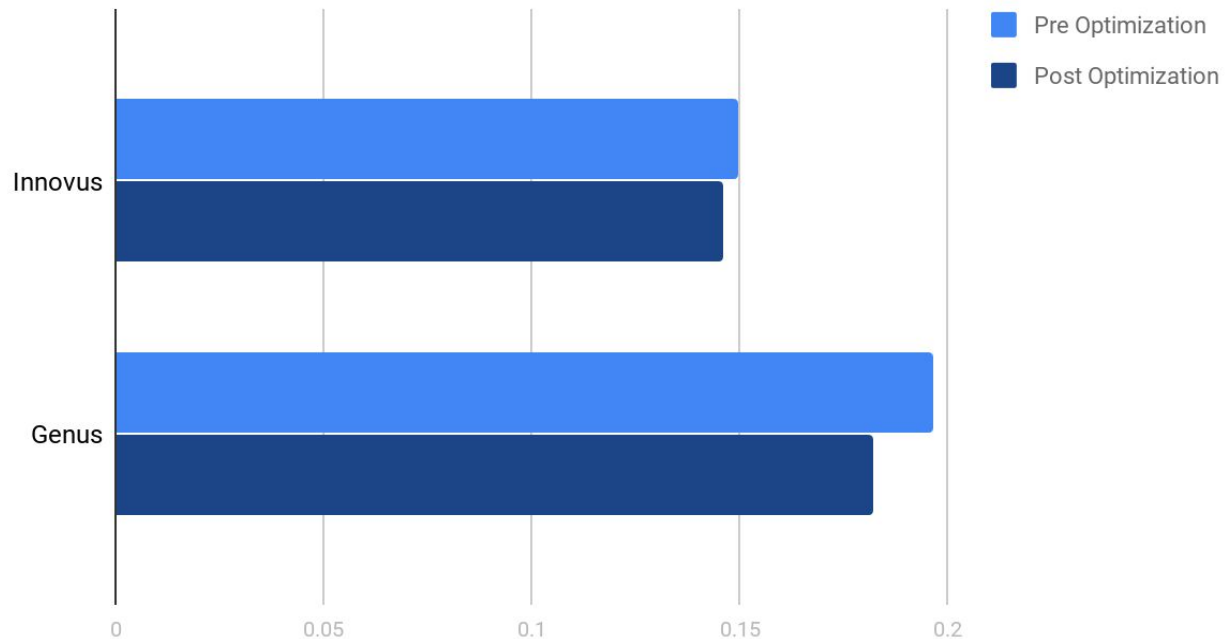
POST-OPTIMIZATION REPORTS

TOOL USED	AREA(μm^2)
GENUS	$1010 + 928 = 1938$
INNOVUS	$1030.1409 + 948.3957 = 1978.5366$

TOOL USED	POWER
GENUS	0.1819 mW
INNOVUS	0.1459 mW

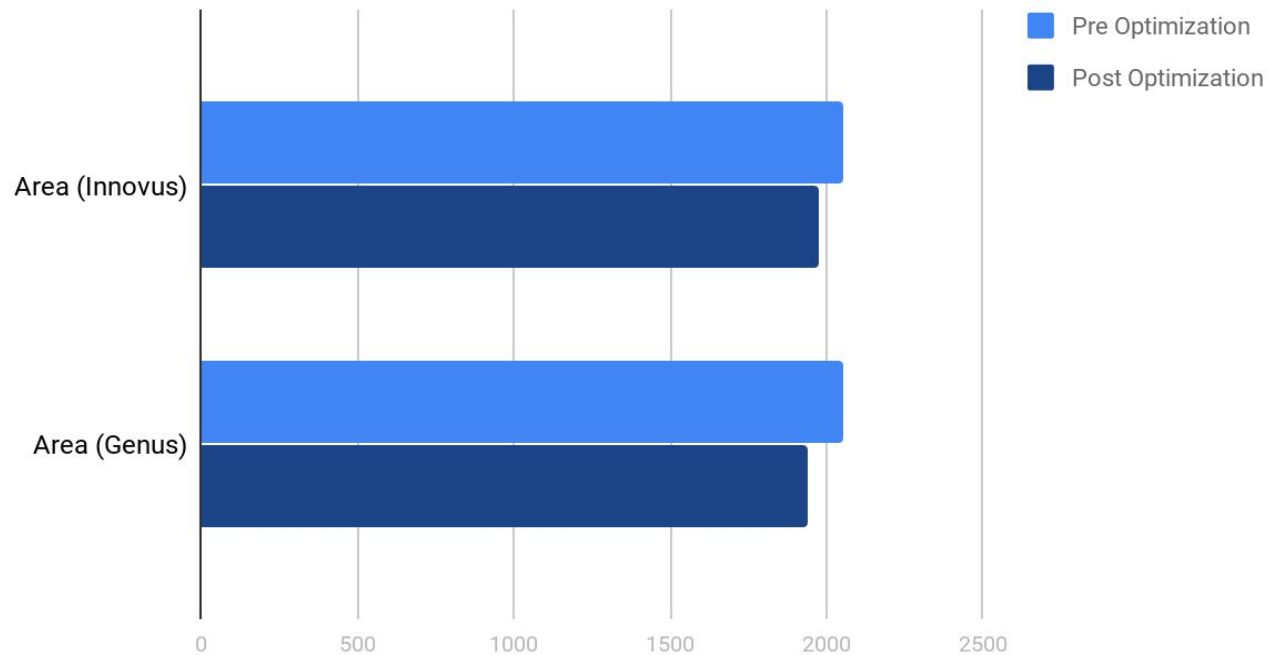
RESULT SUMMARY (POWER)

POWER



RESULT SUMMARY (AREA)

AREA



Thank You!

