VLSI Project

VGA Controller/Driver

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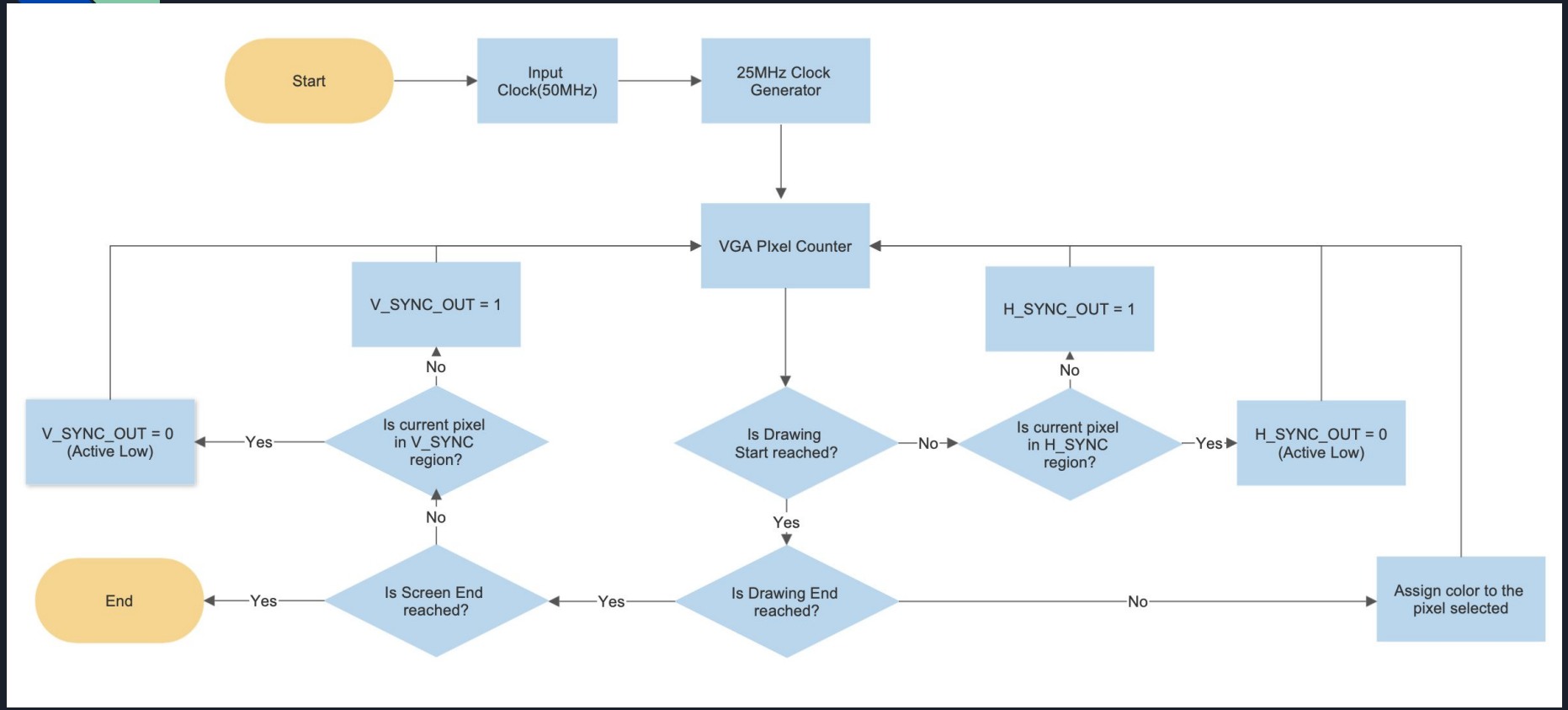
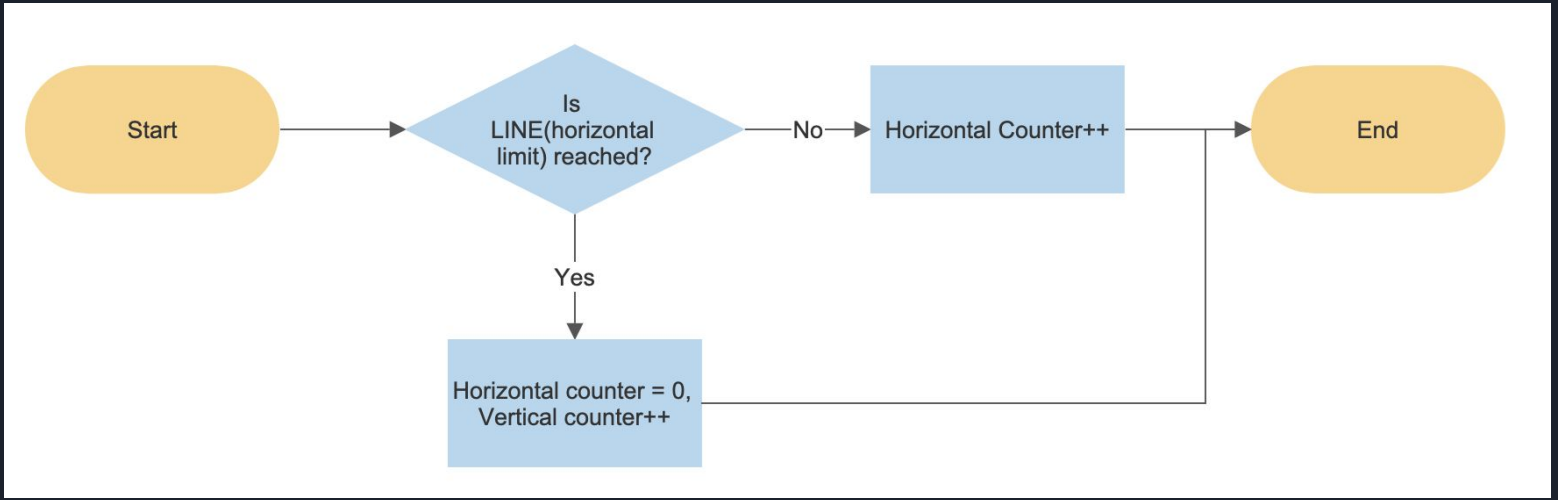
Design

Overall Block Diagram



Pixel Counter Block Diagram

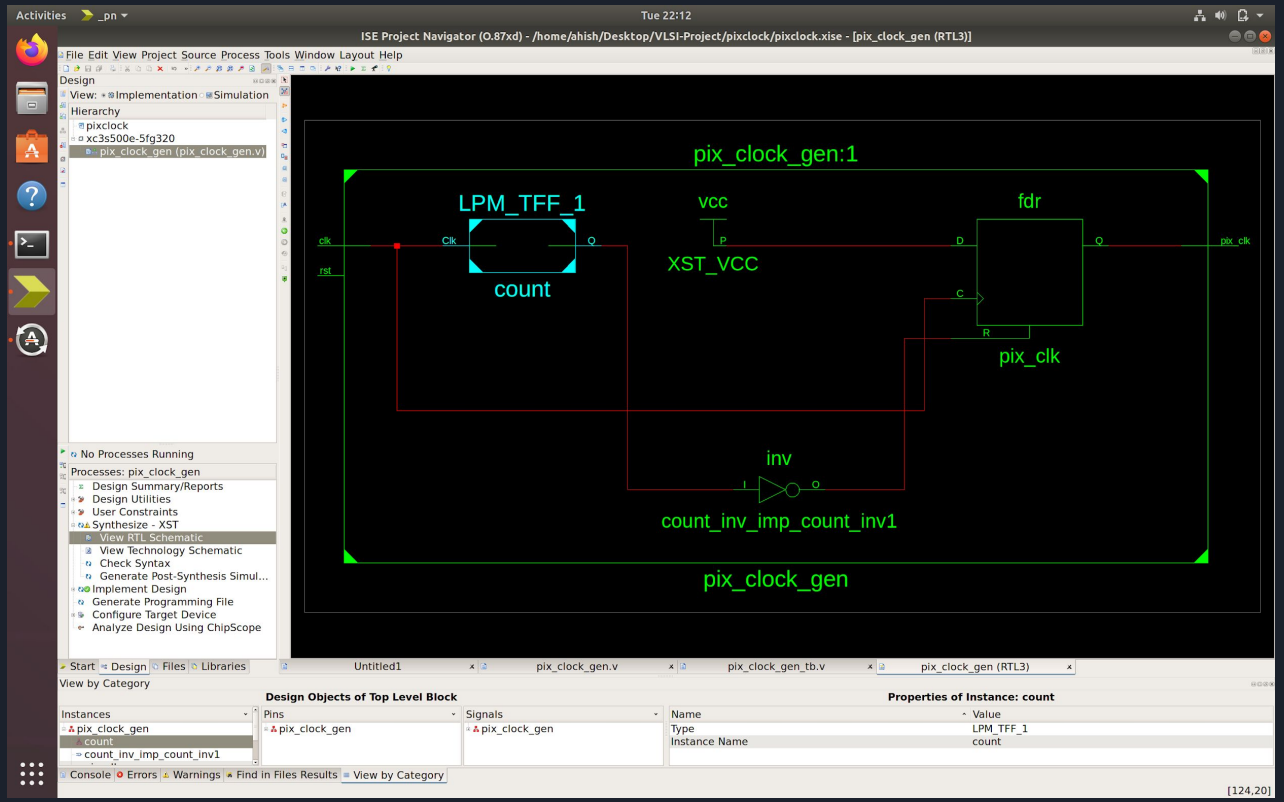


Flow that will be used

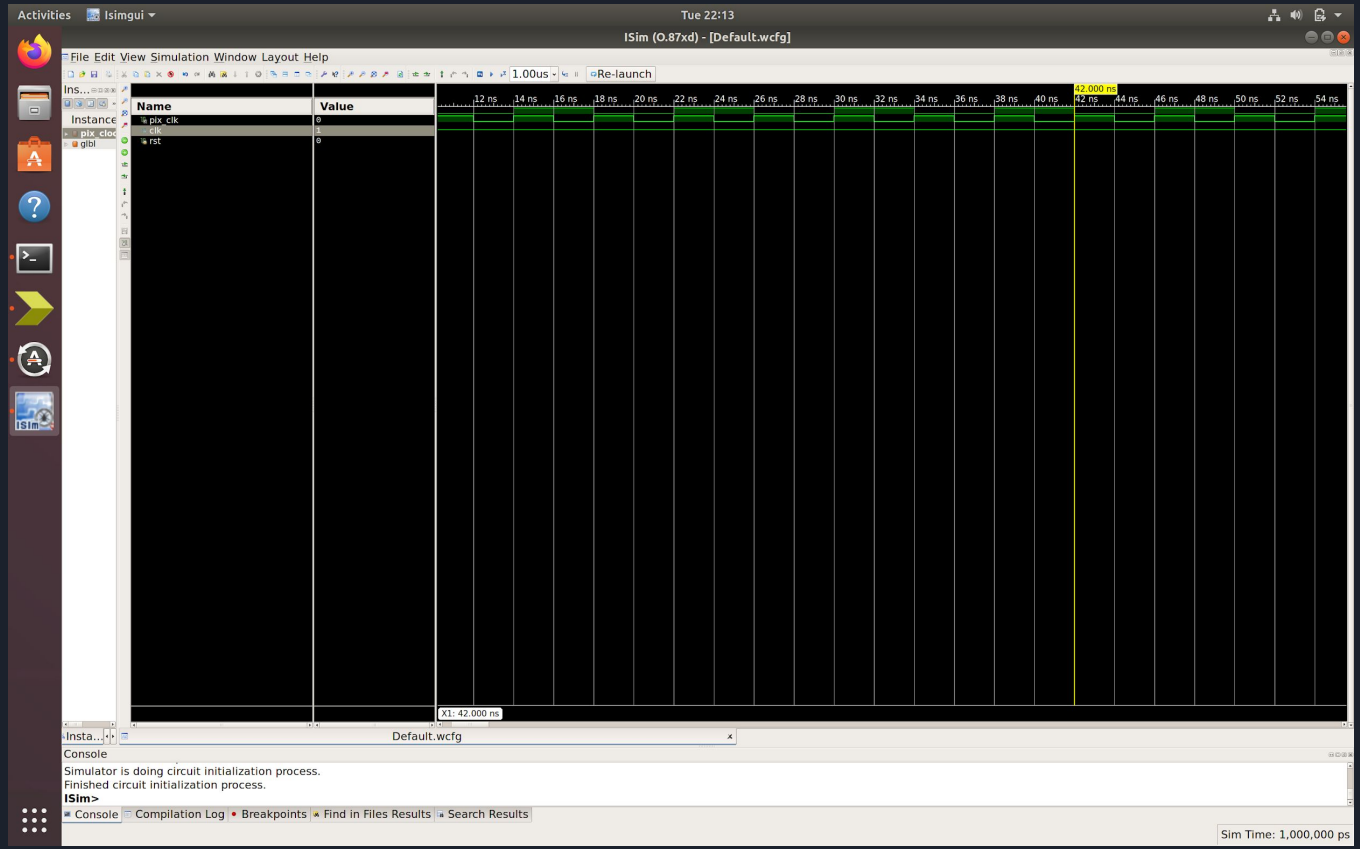
We plan to implement using the FPGA flow and the ASIC flow

Status

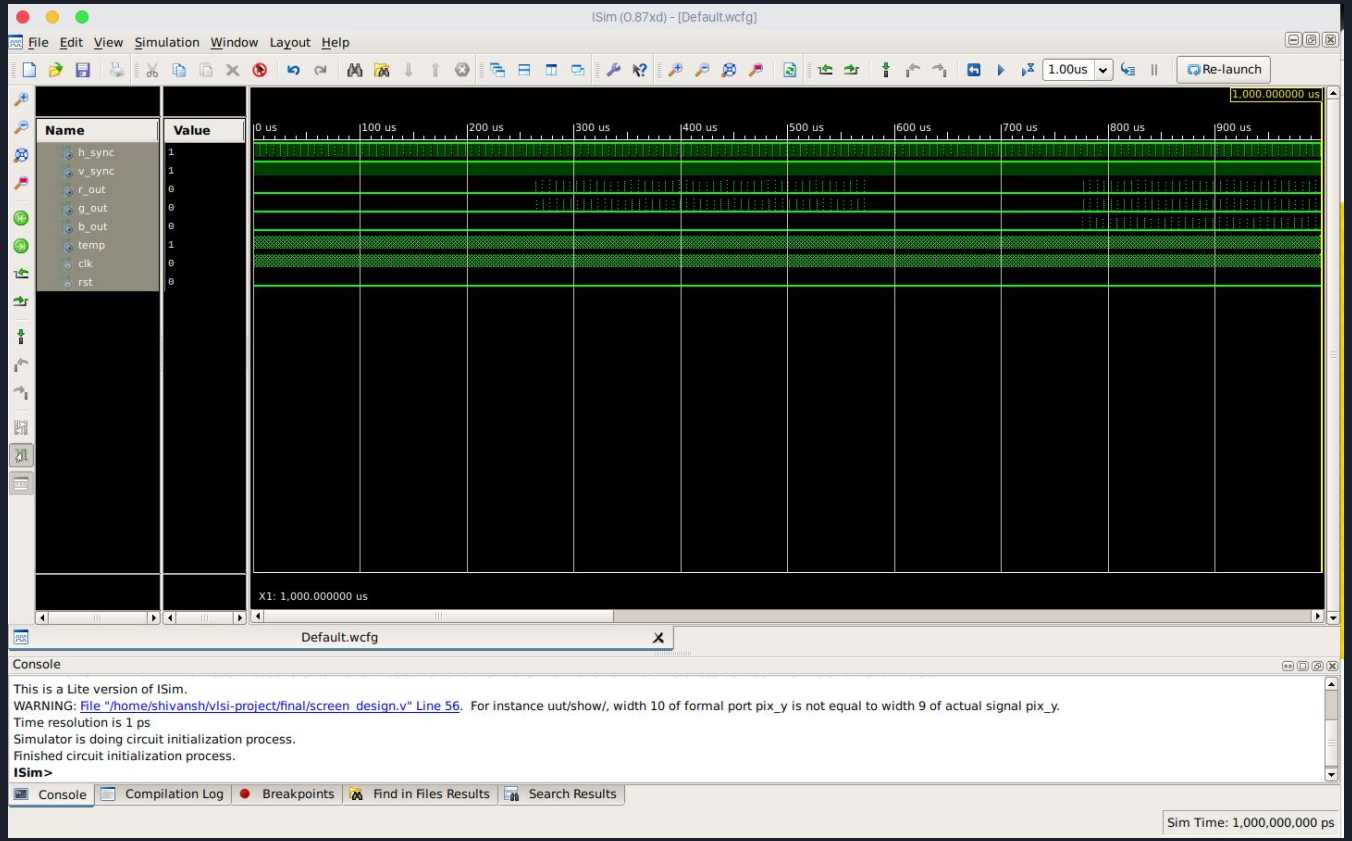
Xilinx RTL for Pixel Clock



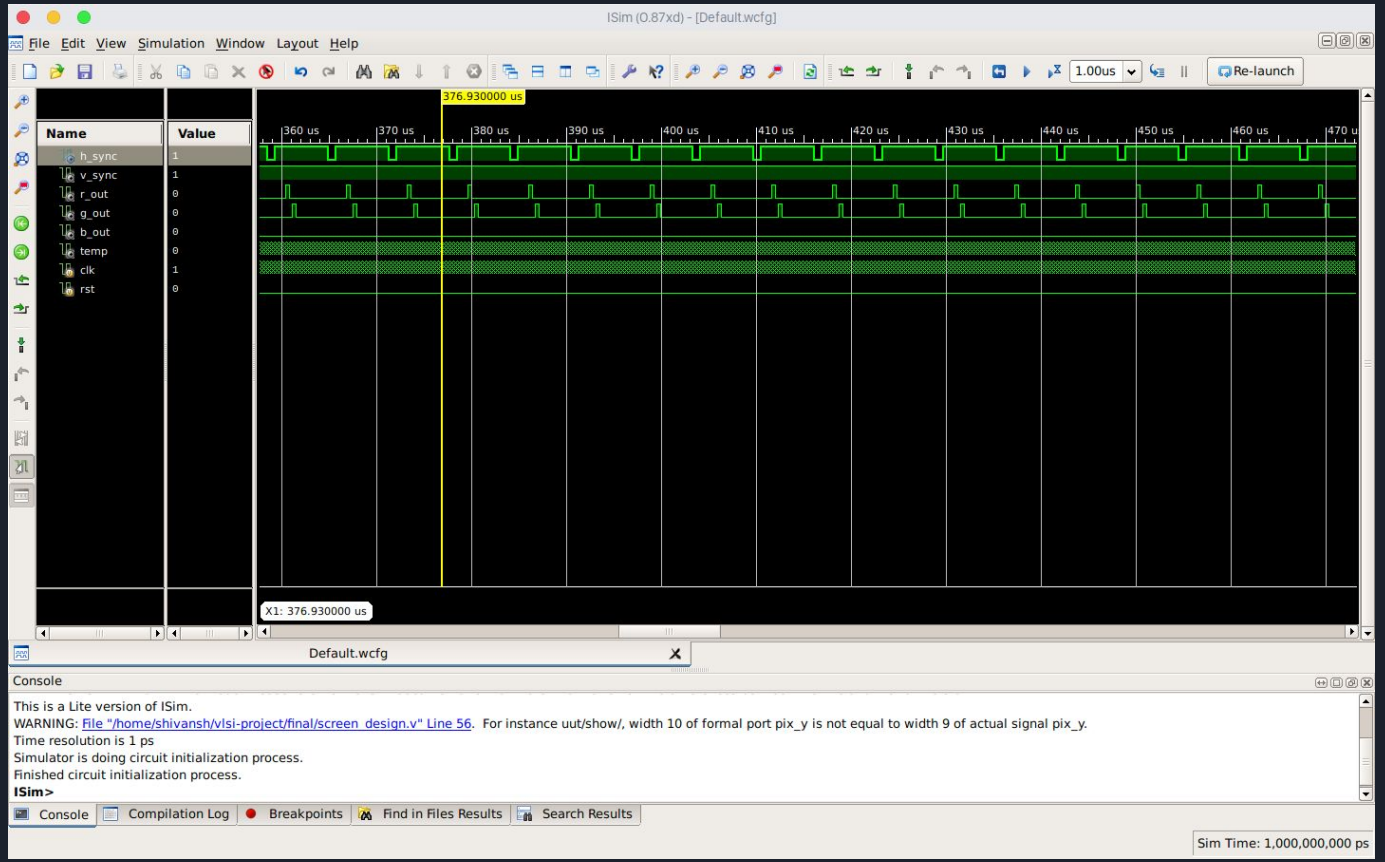
Xilinx Timing Diagram for Pixel Clock



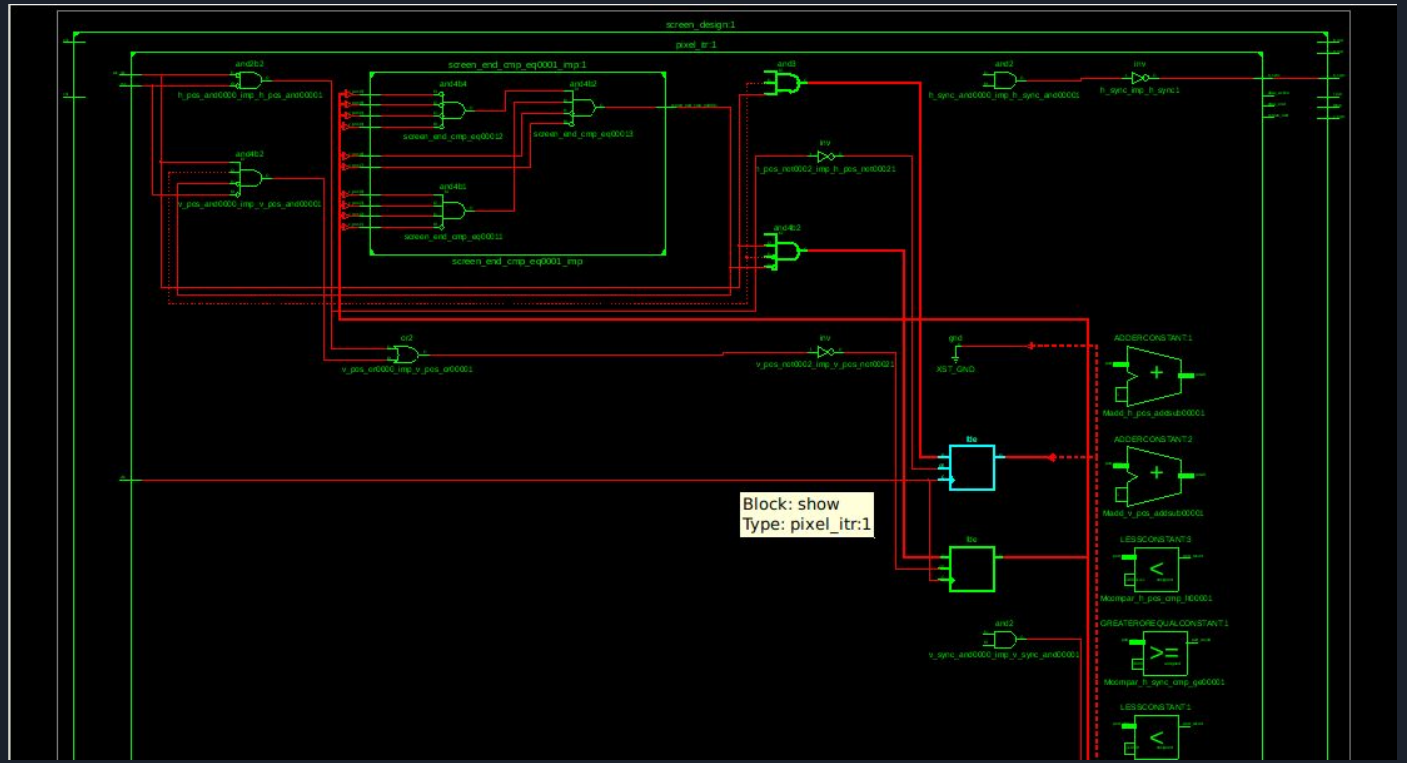
Xilinx Timing Diagram



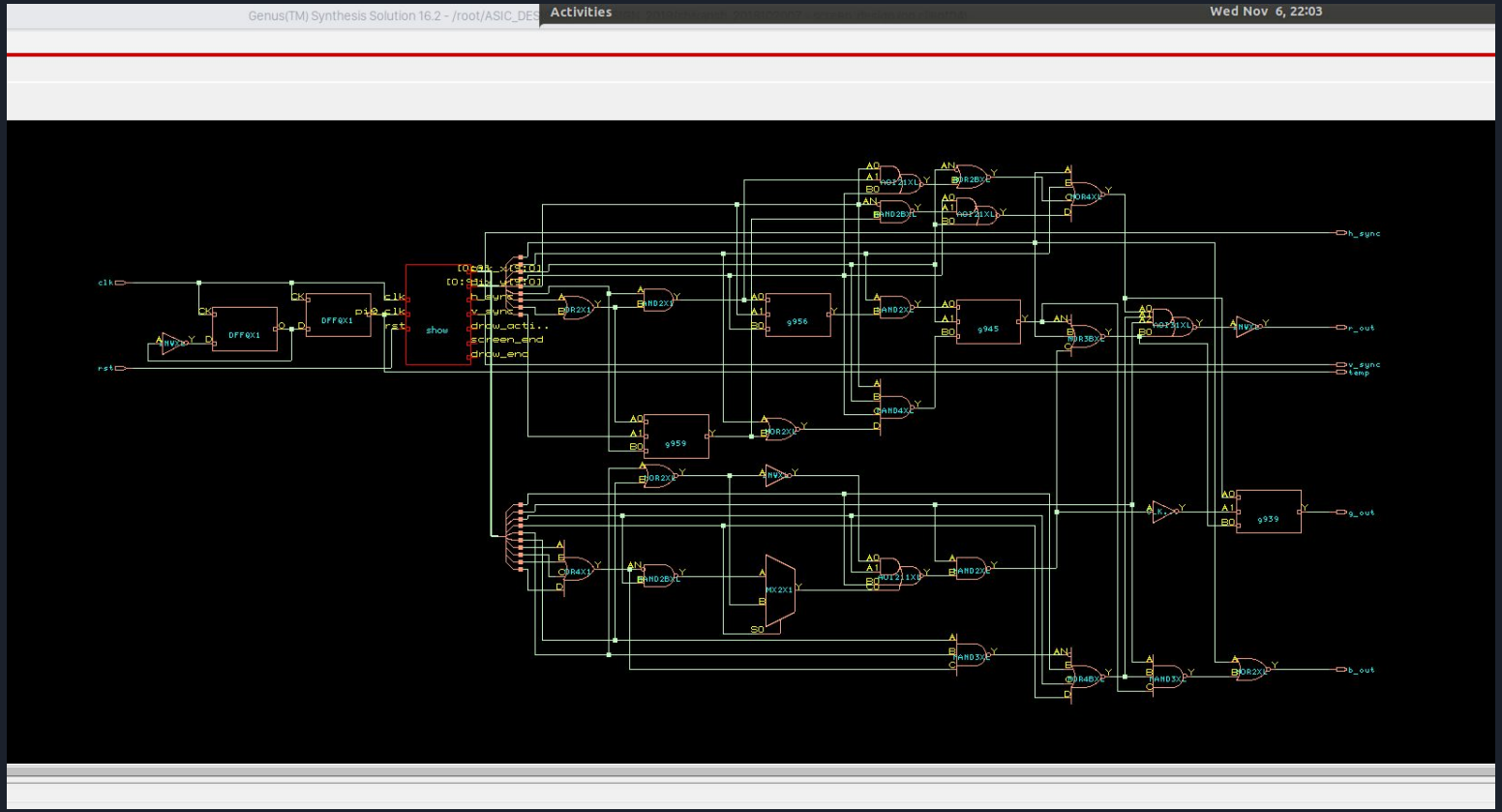
Xilinx Timing Diagram



Xilinx RTL for Pixel Counter



Schematic for assigning colors



What is to be looked for?

A similar project is not readily available online, but we can compare the specs with a similar project online.

We will tabulate the values found in the CAD softwares and try to get the same values from another project similar to this.

The two values can then be compared.

Thank You