



VGA Card

VLSI PROJECT

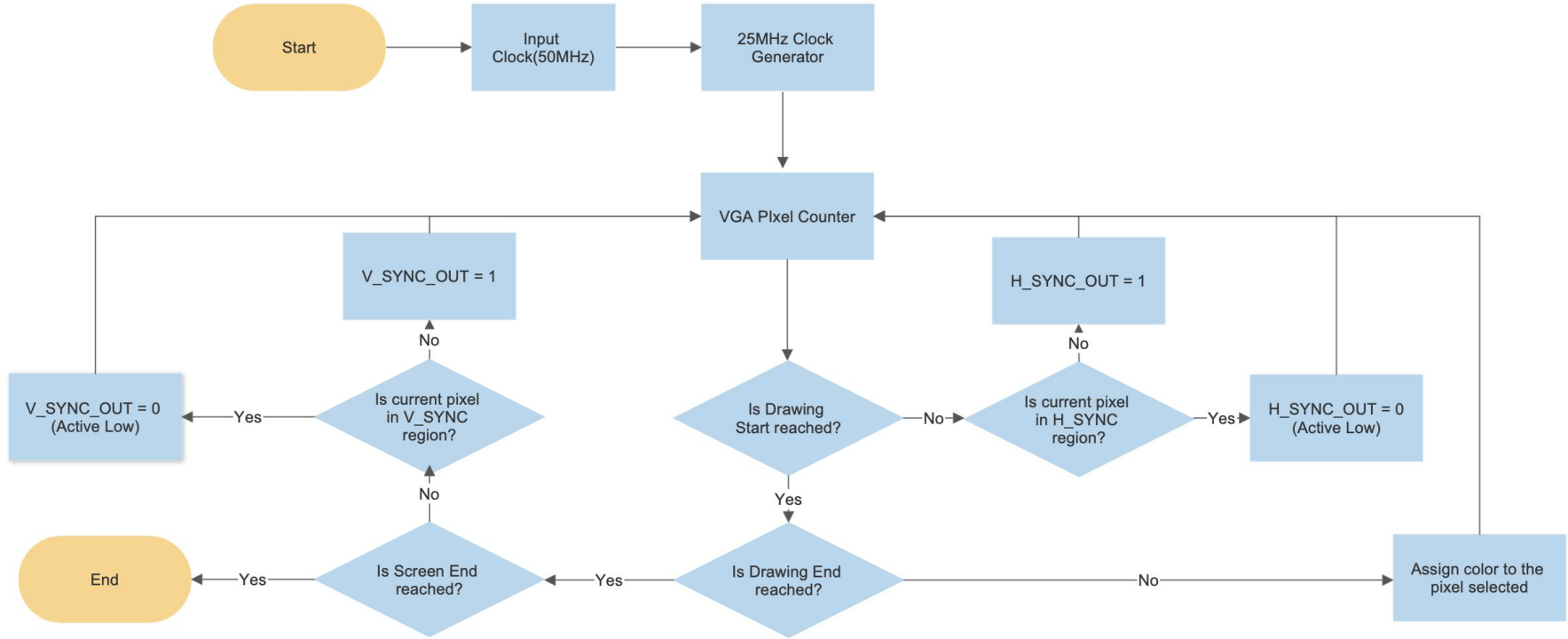
Ahish Deshpande - 2018102022

Shivansh - 2018102007

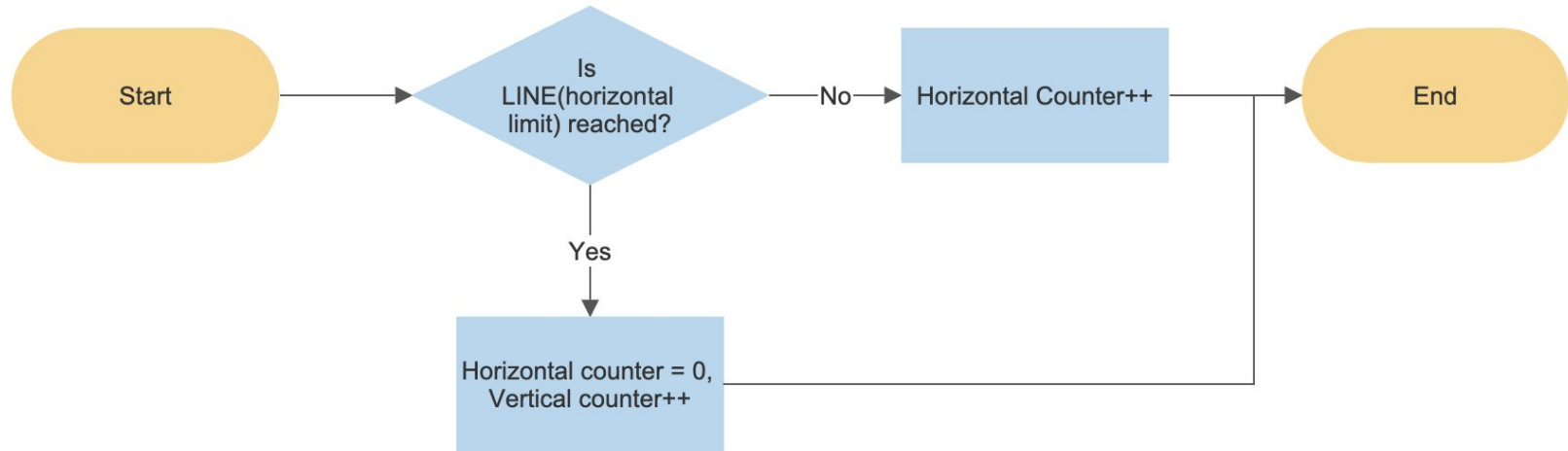
DESIGN



DESIGN : Overall Block Diagram



DESIGN : Pixel Counter Block Diagram



Flow that will be used

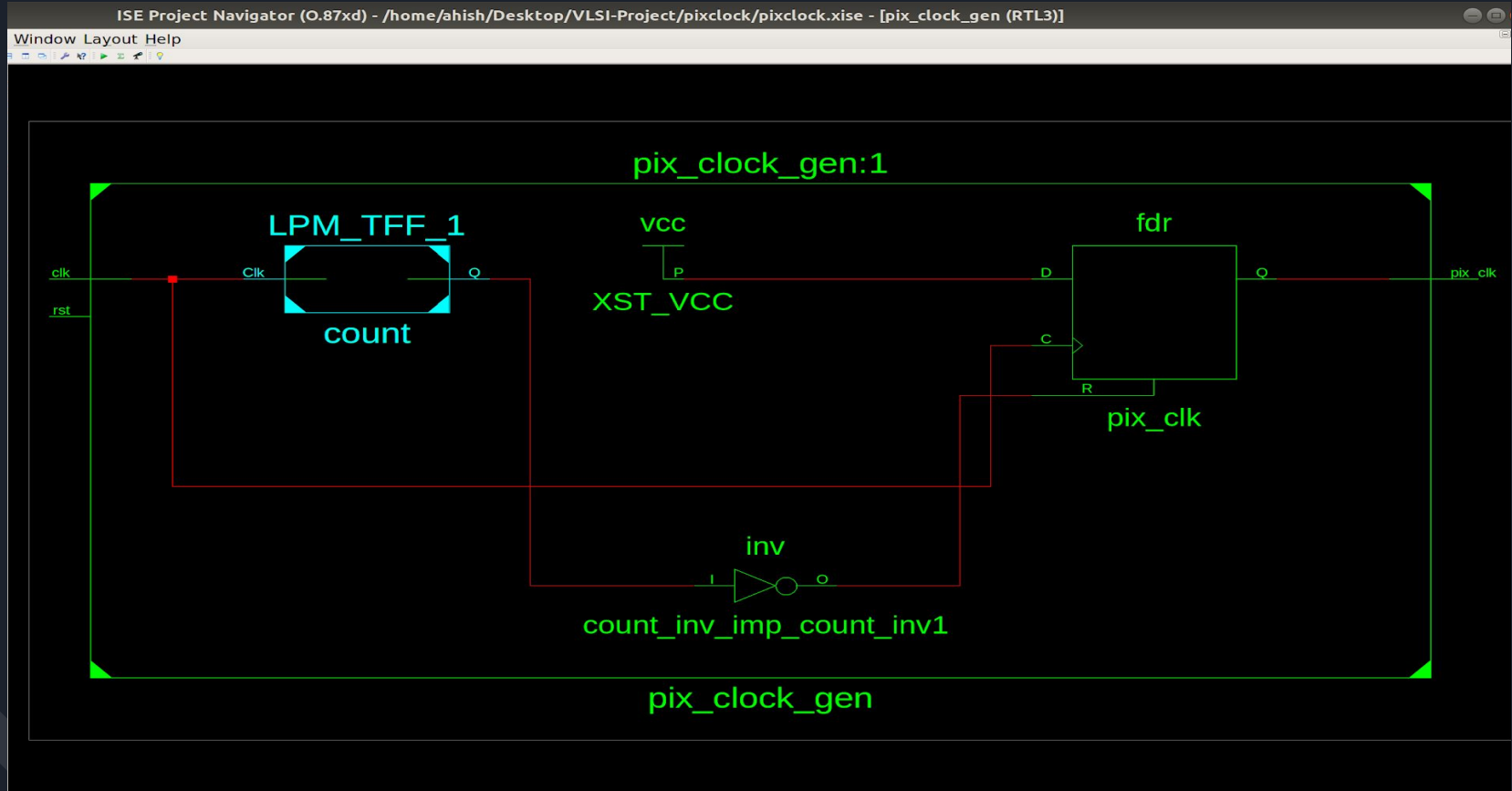
We have implemented our project using the FPGA flow and the ASIC flow.



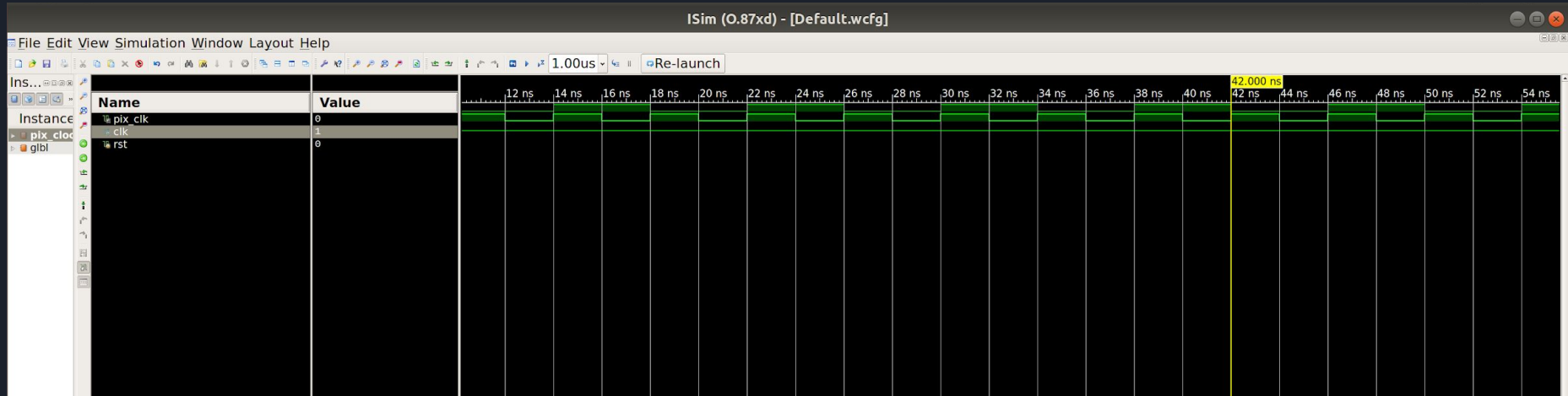
Illustrative Reports & Diagrams

The background features a series of dark gray, three-dimensional rectangular planes that recede into the distance, creating a sense of depth. A bright green parallelogram and a blue parallelogram are positioned on these planes, adding a pop of color to the monochromatic scheme.

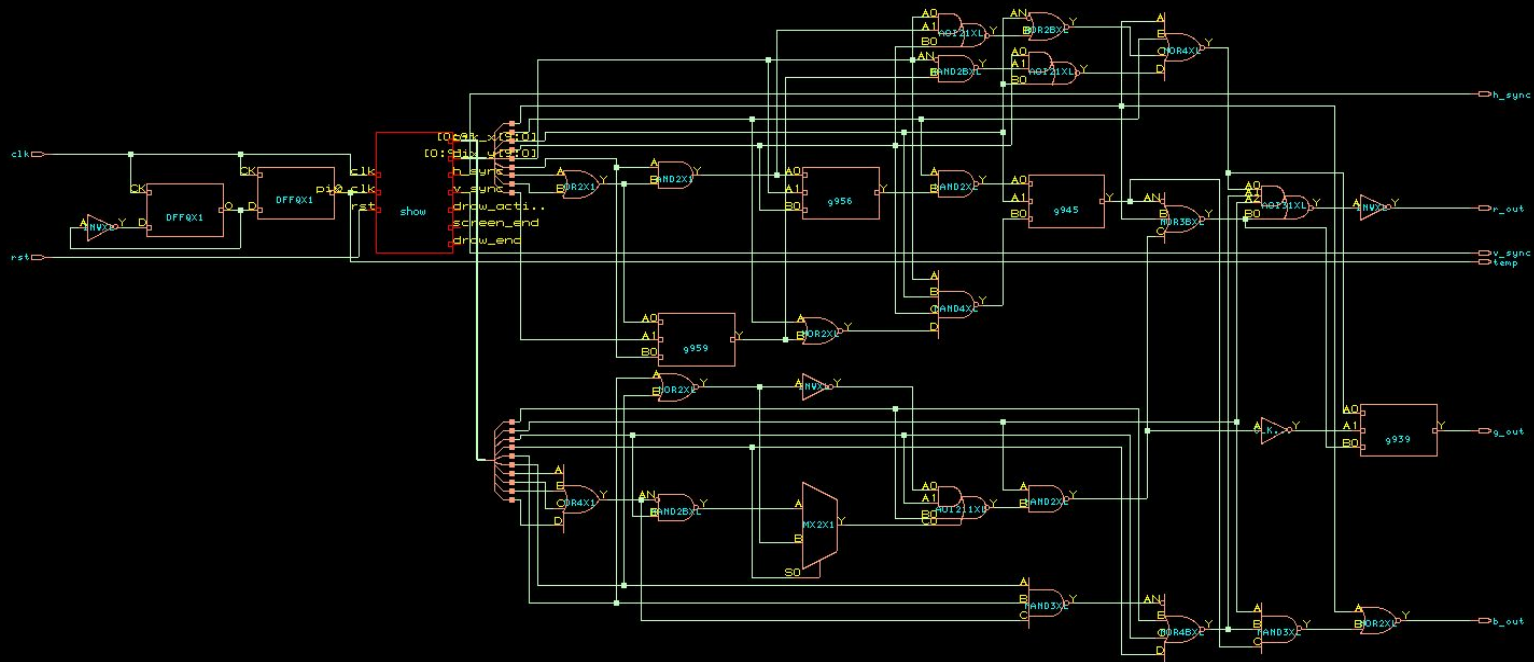
PIXEL CLOCK : Xilinx RTL Schematic



PIXEL CLOCK : Xilinx Timing Diagram



MAIN BLOCK : Genus RTL Schematic



The screenshot displays the ISim (0.87xd) - [Default.wcfg] application window. The top menu bar includes File, Edit, View, Simulation, Window, Layout, and Help. Below the menu is a toolbar with various icons for file operations, simulation control, and viewing options. The main workspace is divided into three panes:

- Left Pane:** A list of signals with their current values.

| Name | Value |
|--------|-------|
| h_sync | 1 |
| v_sync | 1 |
| r_out | 0 |
| g_out | 0 |
| b_out | 0 |
| temp | 1 |
| clk | 0 |
| rst | 0 |
- Top Right Pane:** A timing diagram showing a 1,000.000000 us time scale. The diagram displays several digital signals as green waveforms on a black background. The signals are labeled with their names: h_sync, v_sync, r_out, g_out, b_out, temp, clk, and rst. The time scale is marked from 0 us to 900 us in 100 us increments.
- Bottom Right Pane:** A console window titled "Default.wcfg" showing the following text:

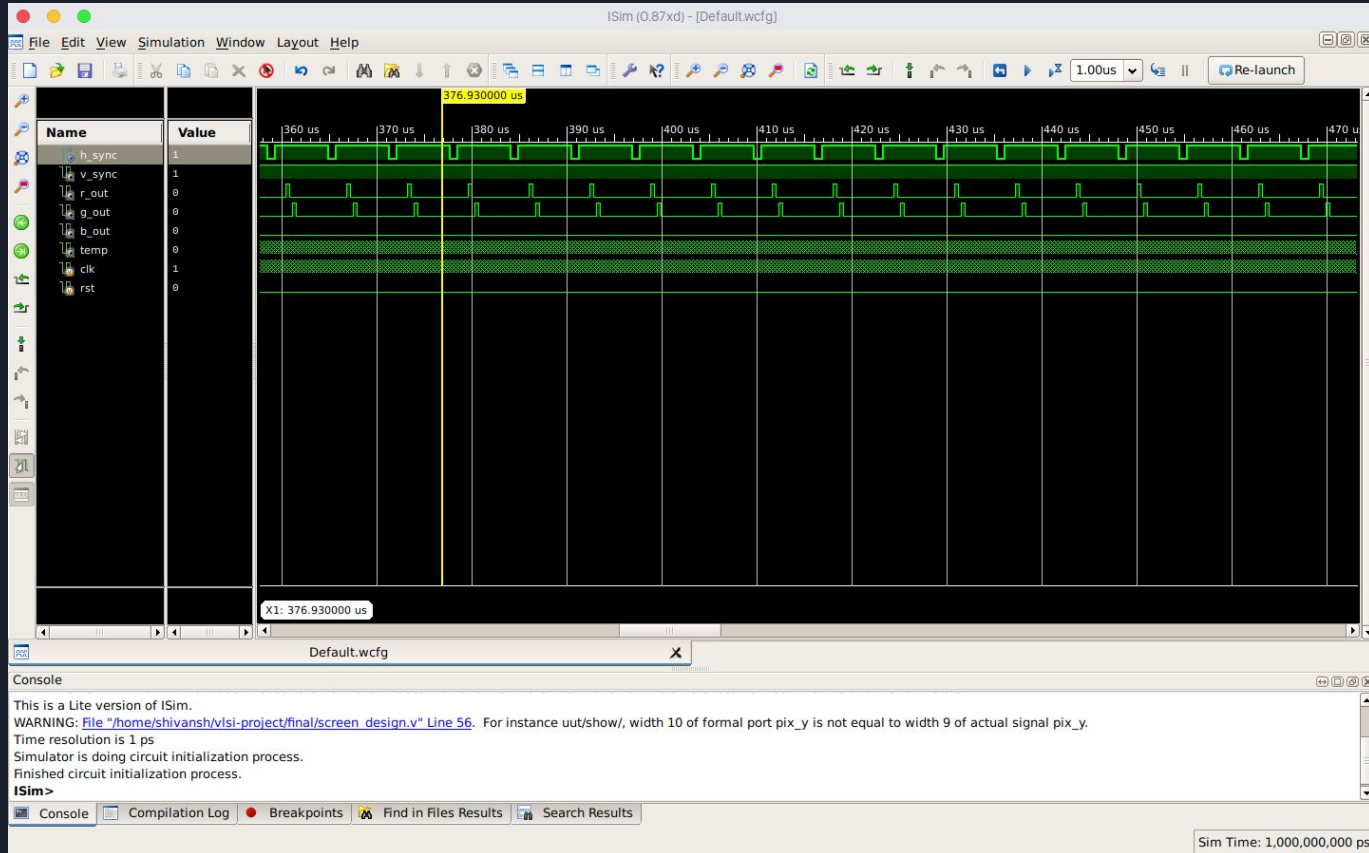

```

      This is a Lite version of ISim.
      WARNING: File "/home/shivansh/vlsi-project/final/screen_design.v" Line 56. For instance uut/show/, width 10 of formal port pix_y is not equal to width 9 of actual signal pix_y.
      Time resolution is 1 ps
      Simulator is doing circuit initialization process.
      Finished circuit initialization process.
      ISim>
      
```

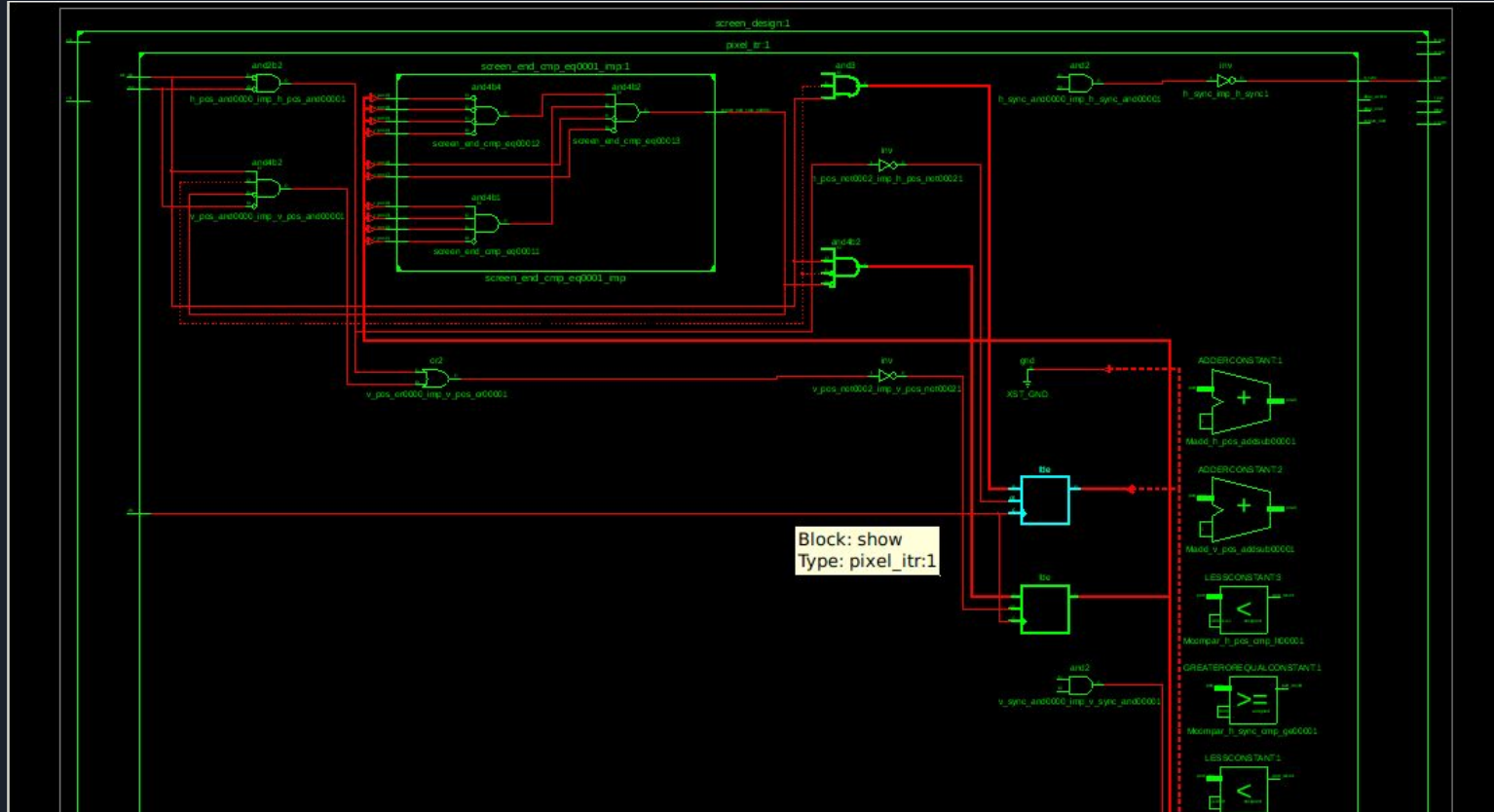
At the bottom of the window, there is a status bar showing "Sim Time: 1,000,000,000 ps".

Sim Time: 1,000,000,000 ps

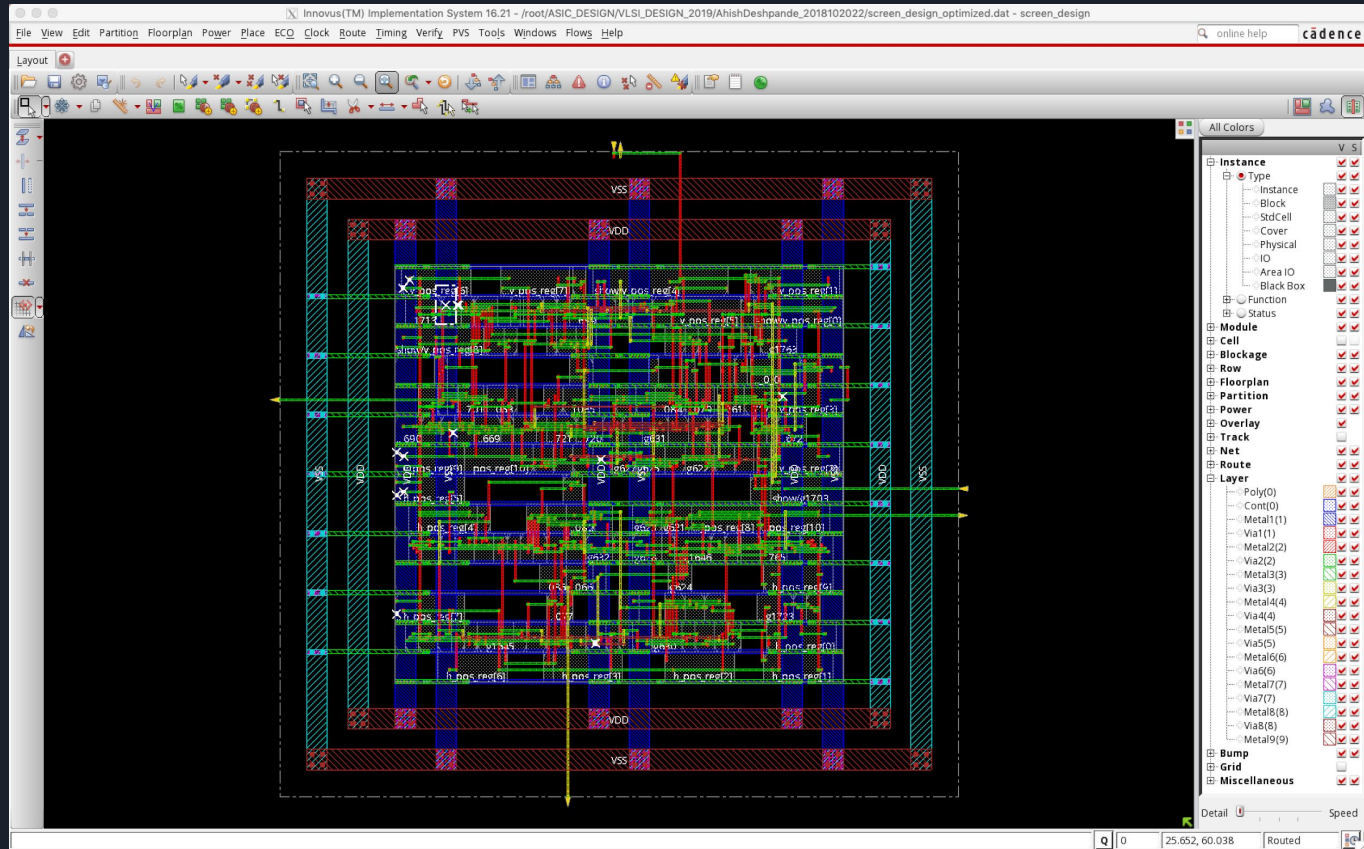
MAIN BLOCK : Xilinx Timing Diagram- II



PIXEL COUNTER : Xilinx RTL Schematic



INNOVUS LAYOUT



RESULTS

& Comparison with Unoptimized
Project



PRE-OPTIMIZATION REPORTS : AREA

| TOOL USED | AREA(μm^2) |
|-----------|------------------------------------|
| GENUS | $1069 + 981 = 2050$ |
| INNOVUS | $1069.4997 + 980.9424 = 2050.3921$ |

PRE-OPTIMIZATION REPORTS : POWER

| TOOL USED | POWER |
|-----------|----------|
| GENUS | 0.1965mW |
| INNOVUS | 0.1493mW |

POST-OPTIMIZATION REPORTS : AREA

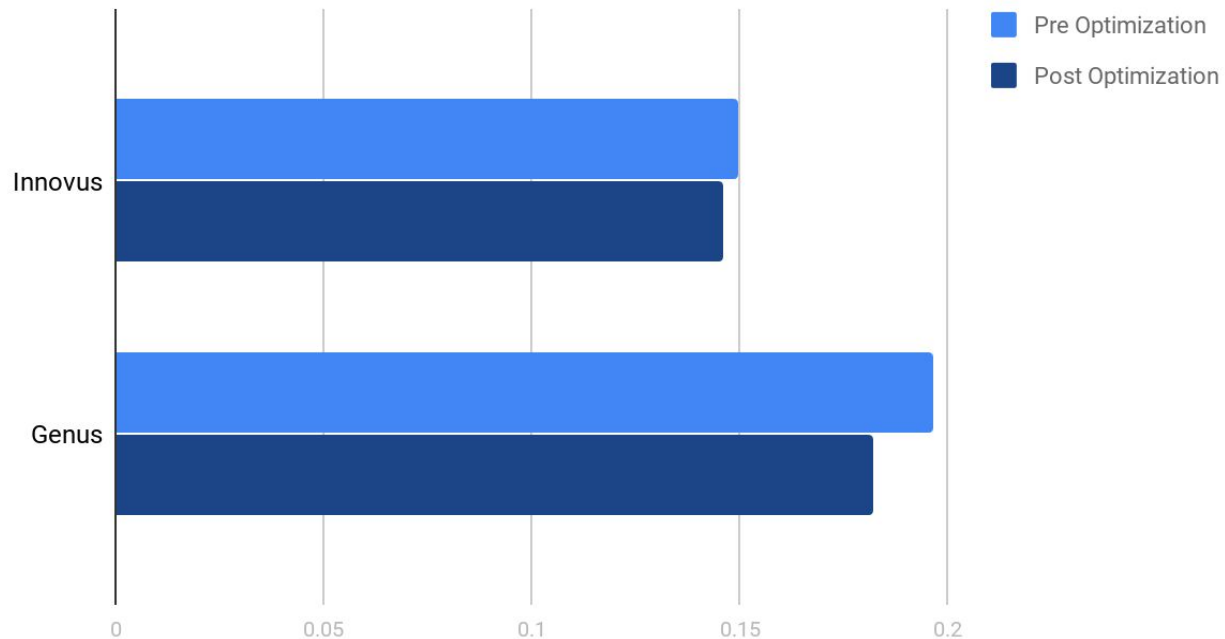
| TOOL USED | AREA(μm^2) |
|-----------|------------------------------------|
| GENUS | $1010 + 928 = 1938$ |
| INNOVUS | $1030.1409 + 948.3957 = 1978.5366$ |

POST-OPTIMIZATION REPORTS : POWER

| TOOL USED | AREA |
|-----------|-----------|
| GENUS | 0.1819 mW |
| INNOVUS | 0.1459 mW |

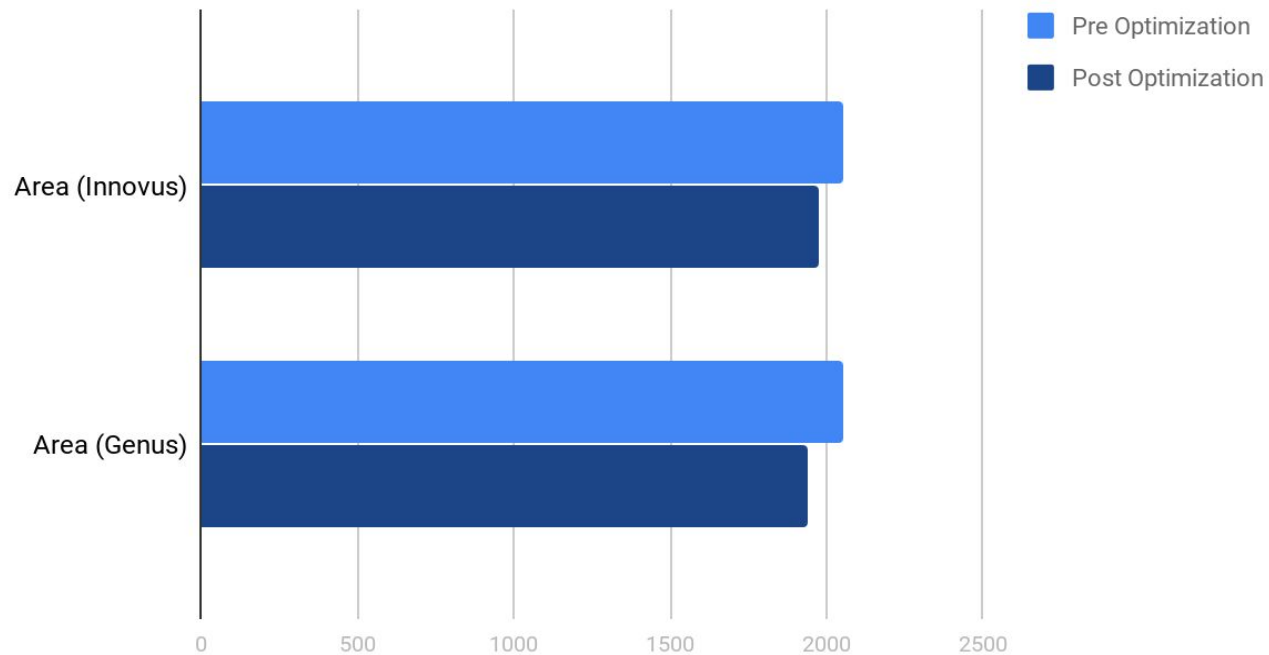
RESULT SUMMARY (POWER)

POWER



RESULT SUMMARY (AREA)

AREA



Thank You!

