VGA Card

VLSI PROJECT

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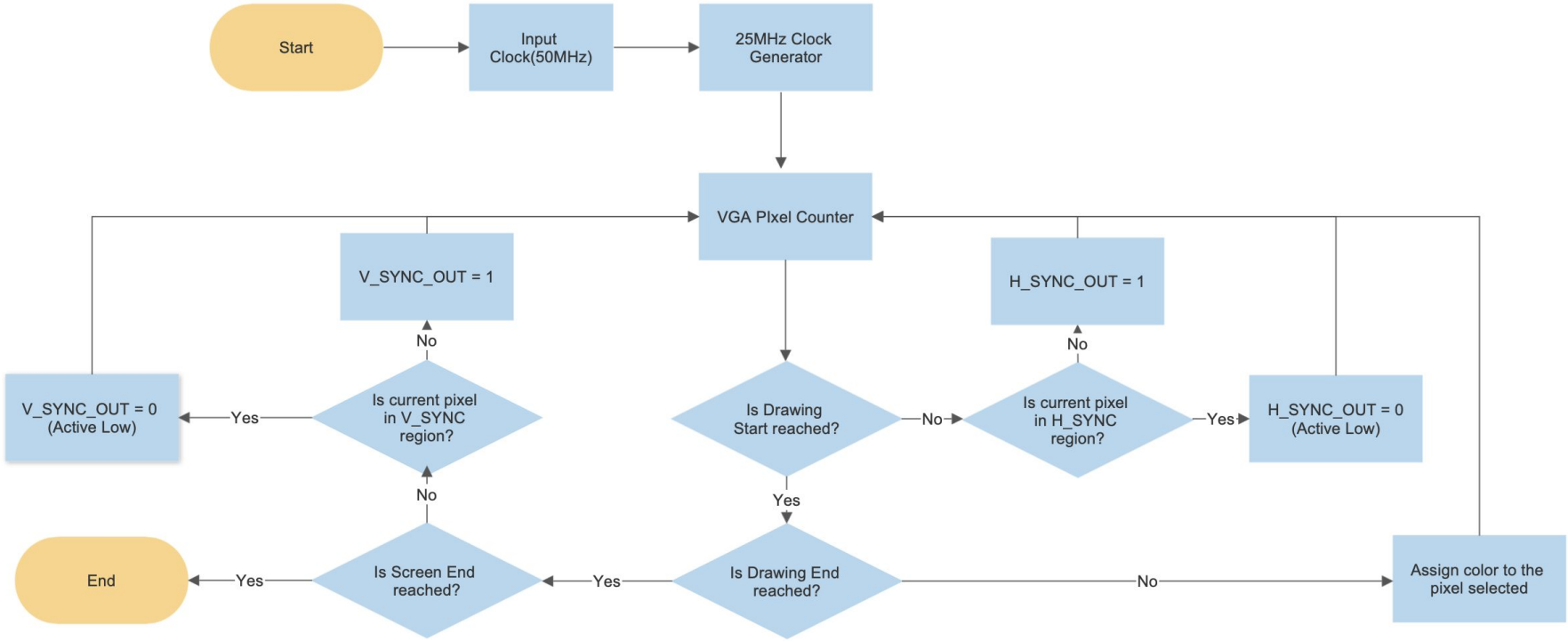
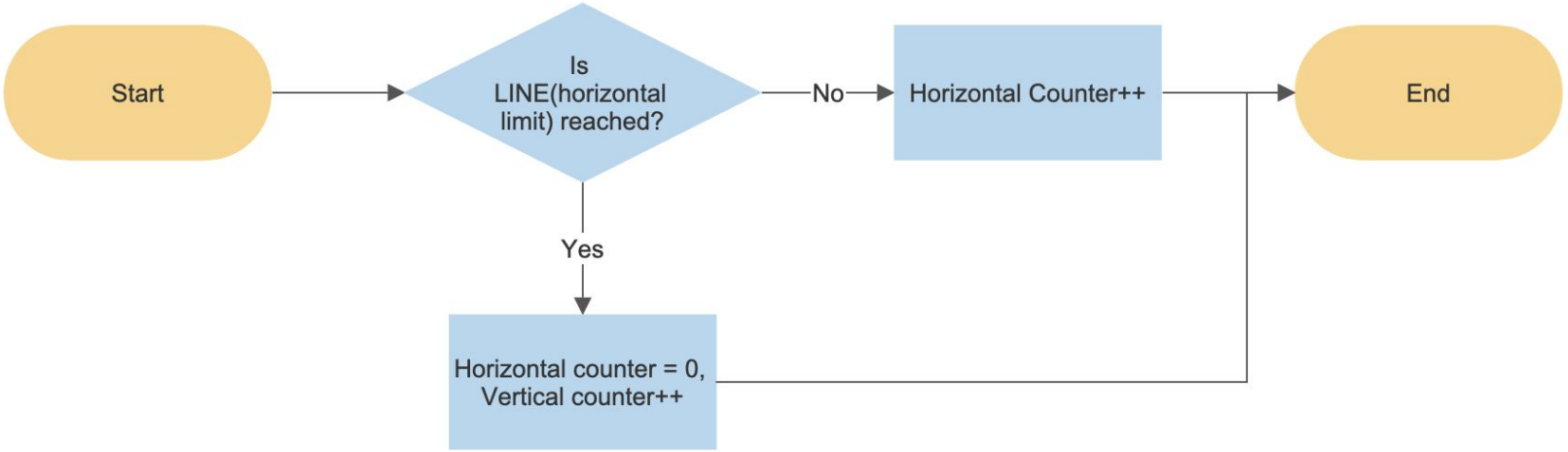
DESIGN

DESIGN : Overall Block Diagram



DESIGN : Pixel Counter Block Diagram

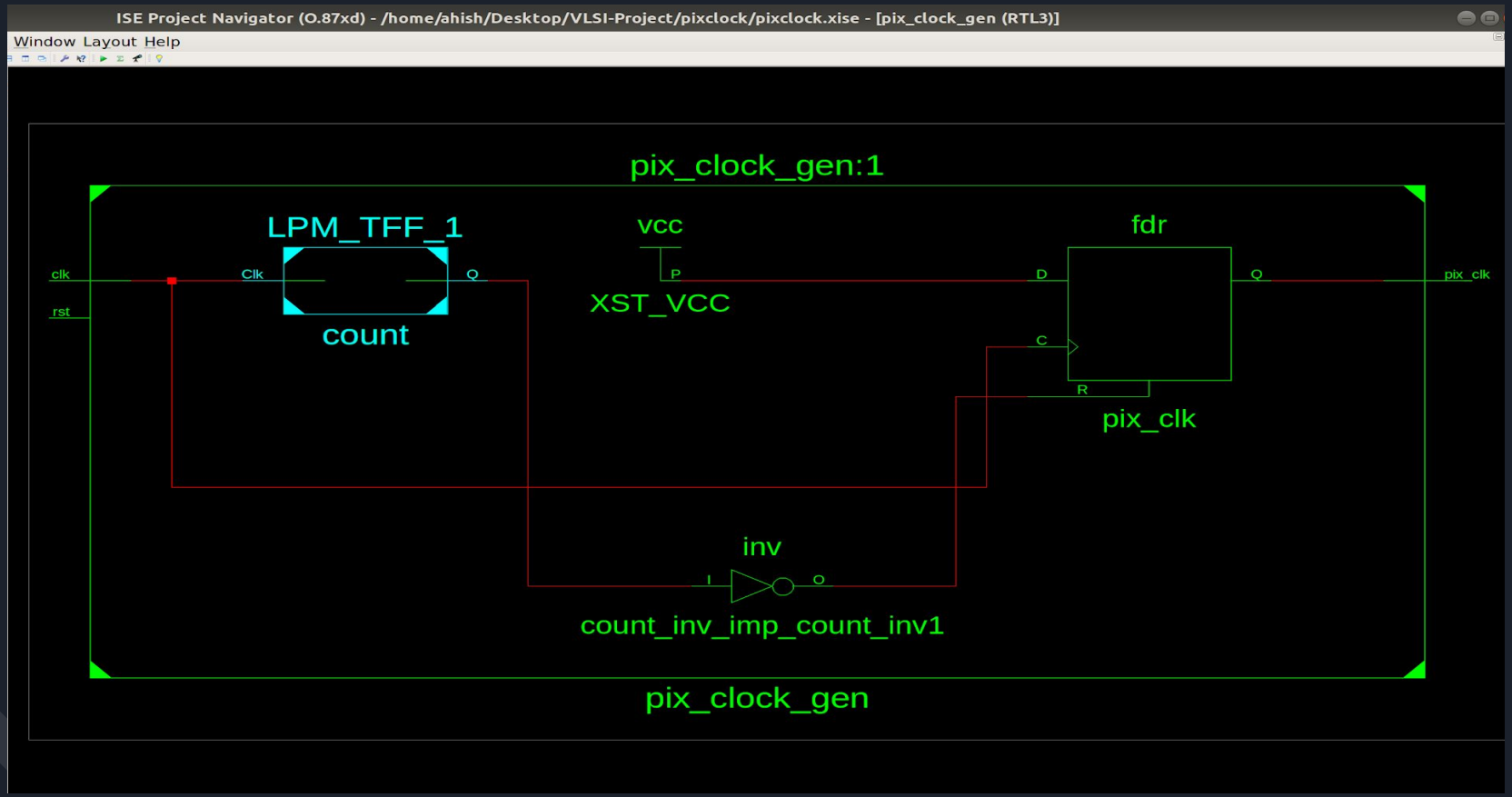


Flow that will be used

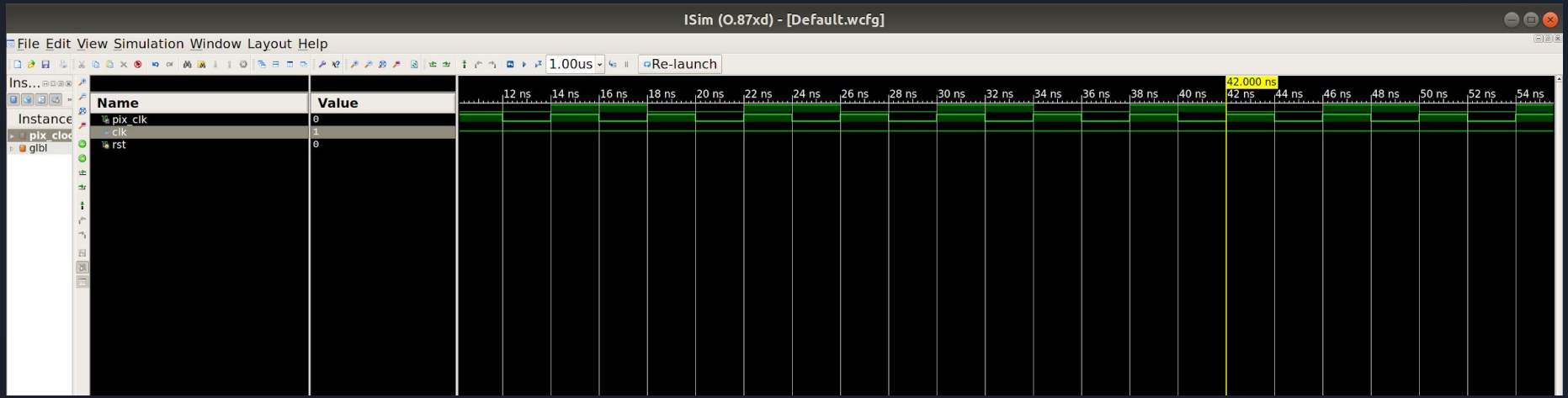
We have implemented our project using the FPGA flow and the ASIC flow.

Illustrative Reports & Diagrams

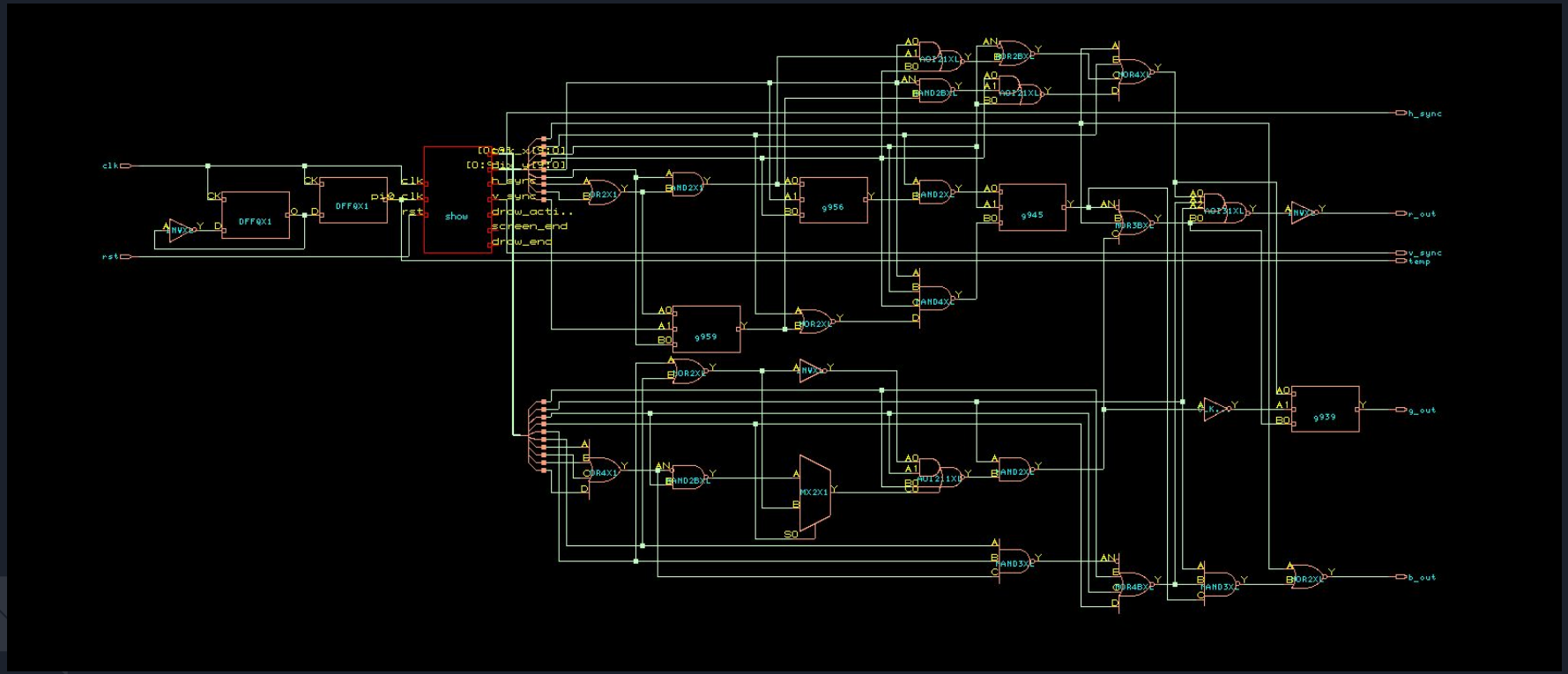
PIXEL CLOCK : Xilinx RTL Schematic



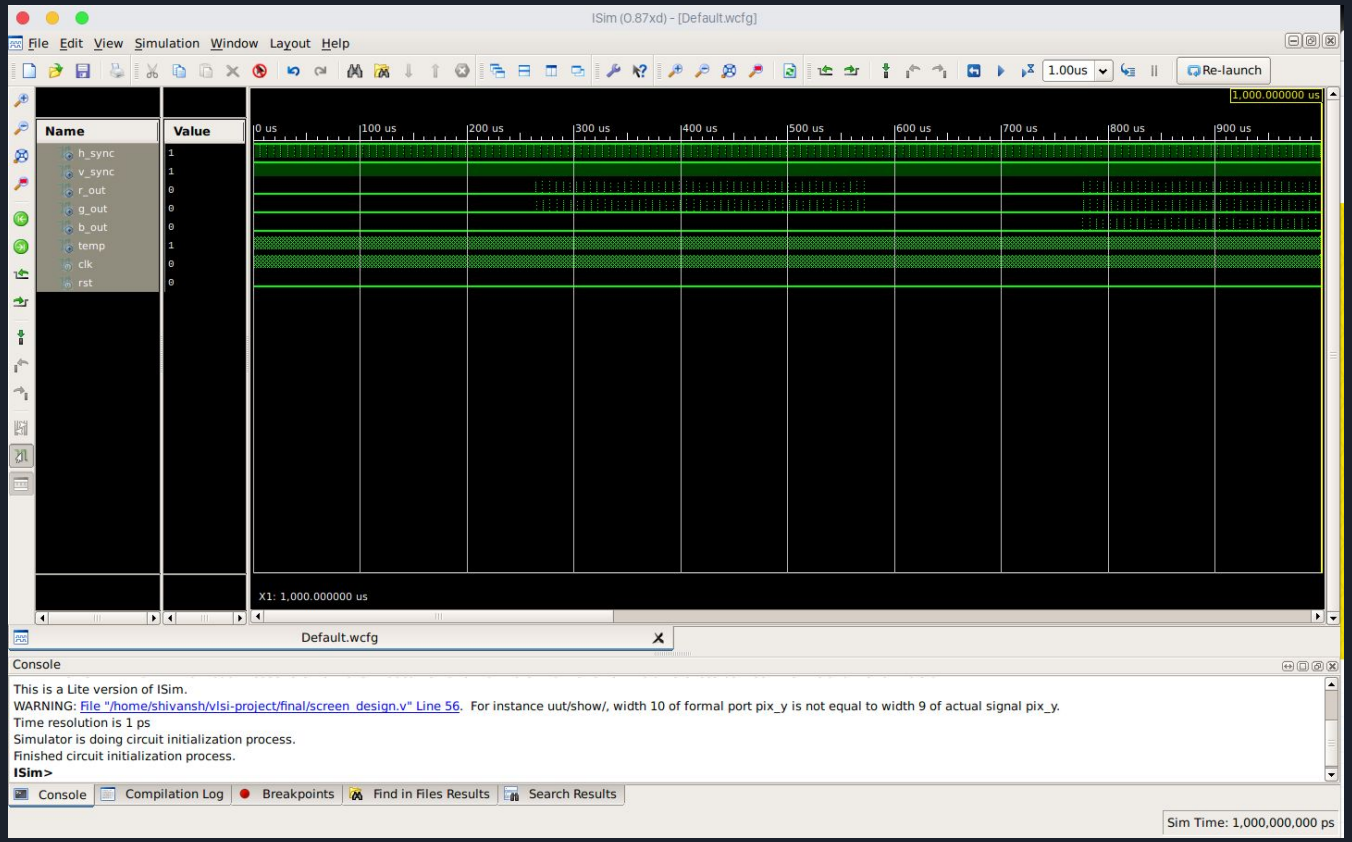
PIXEL CLOCK : Xilinx Timing Diagram



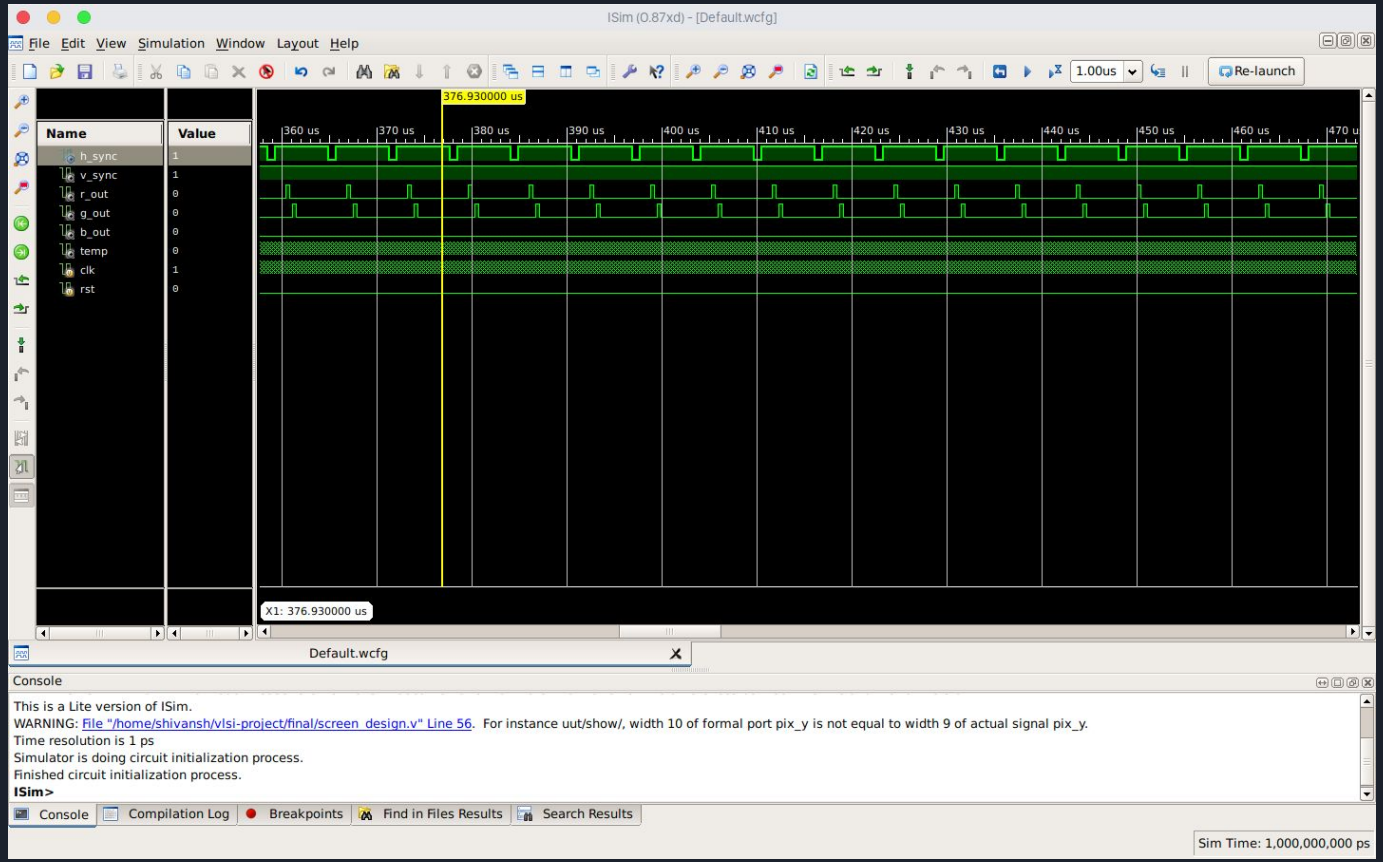
MAIN BLOCK : Genus RTL Schematic



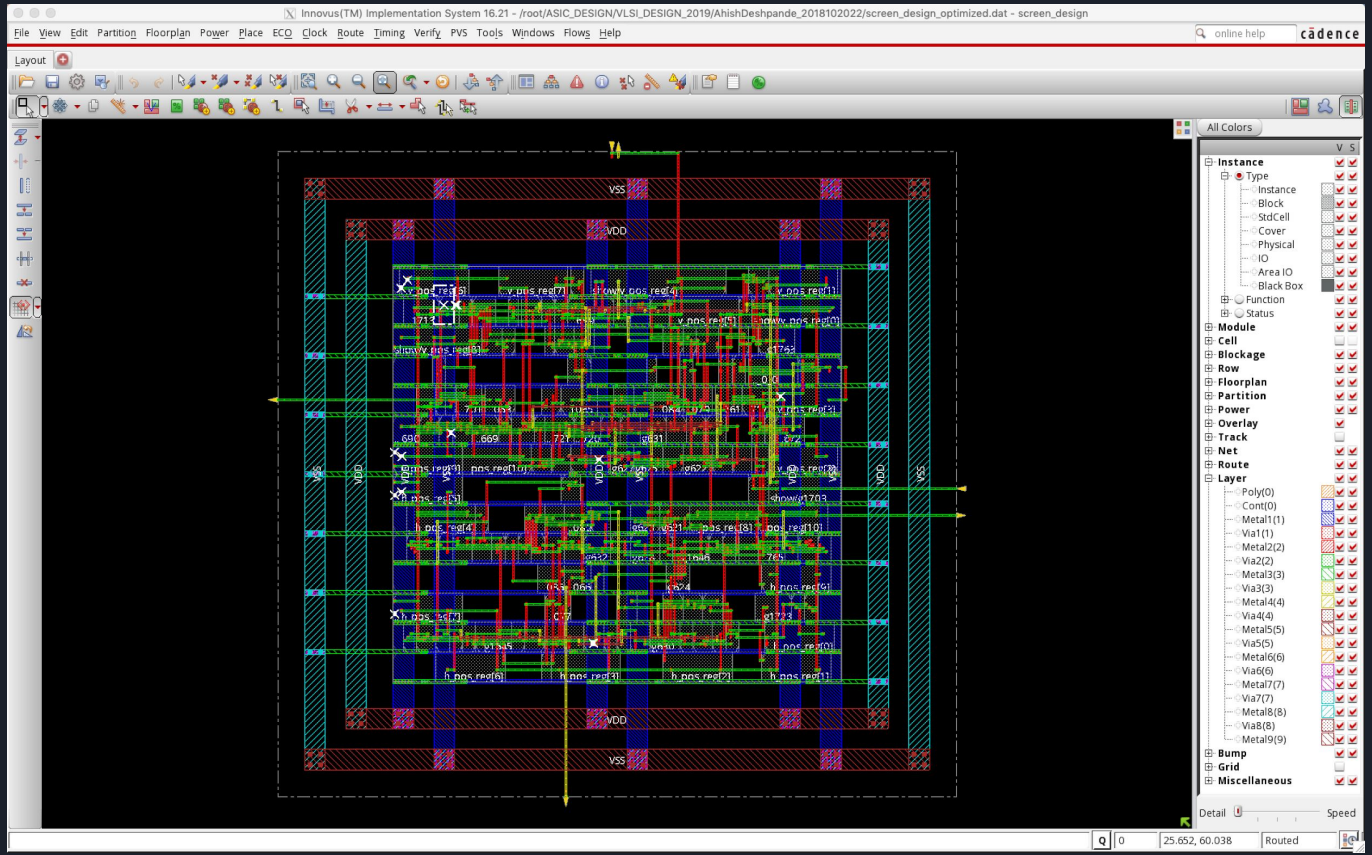
MAIN BLOCK : Xilinx Timing Diagram - I



MAIN BLOCK : Xilinx Timing Diagram- II



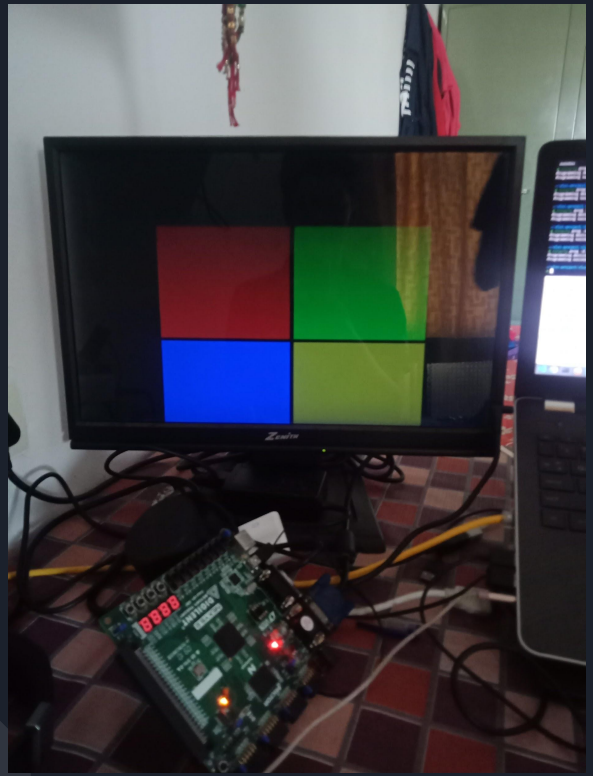
INNOVUS LAYOUT

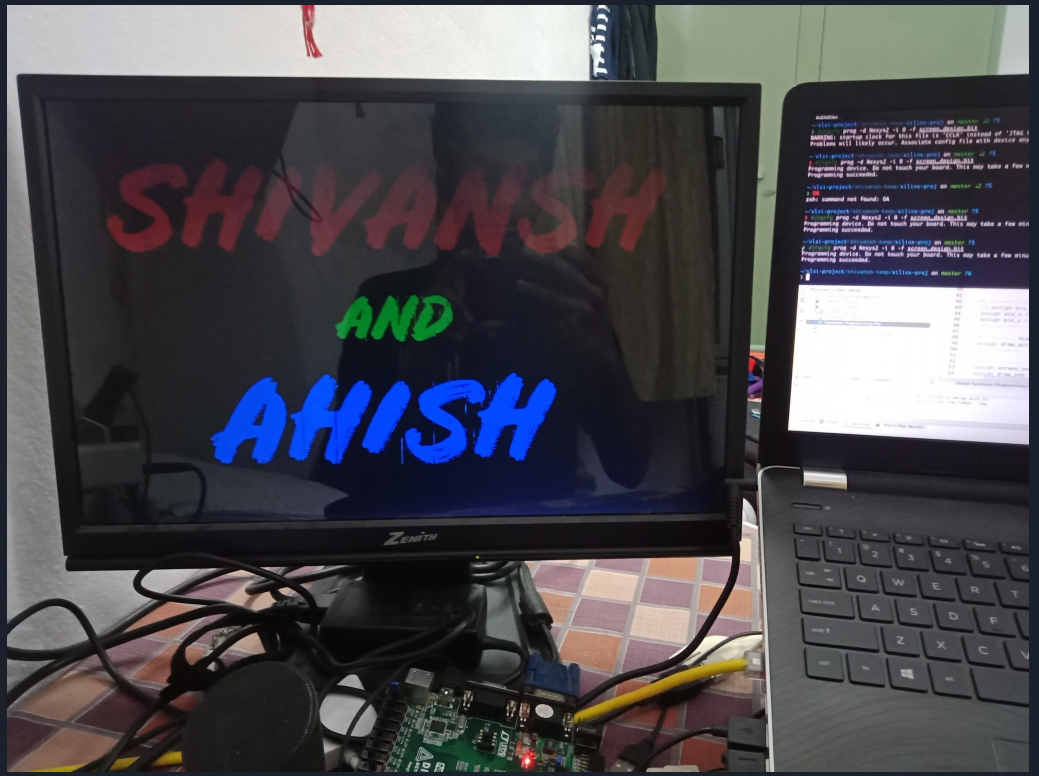


PROGRESS (As of 17 Nov' 2019)

We are now able to generate bitmap of an image and display it on the monitor using our VGA card.

INITIAL IMAGES DISPLAYED





the Biggest Bitmaps processed yet!

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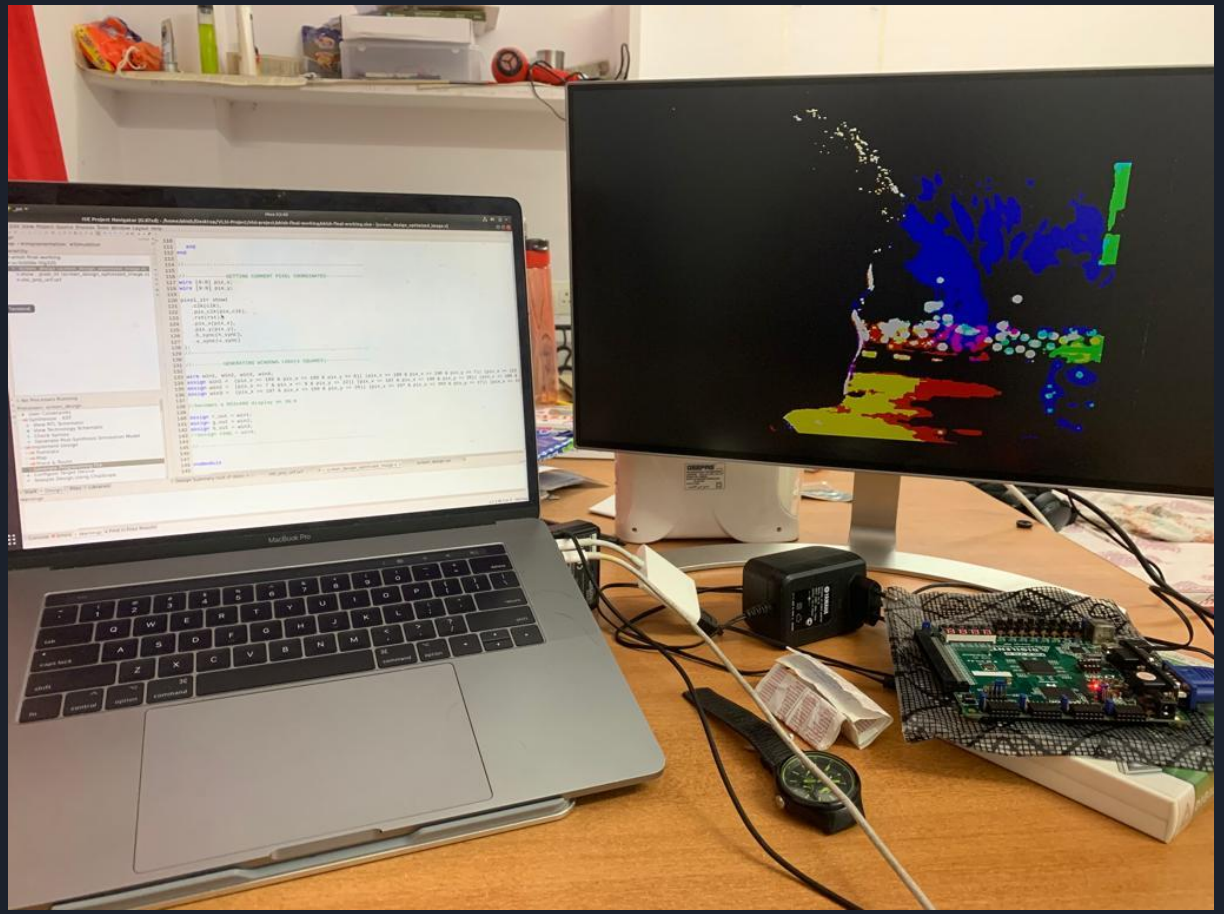
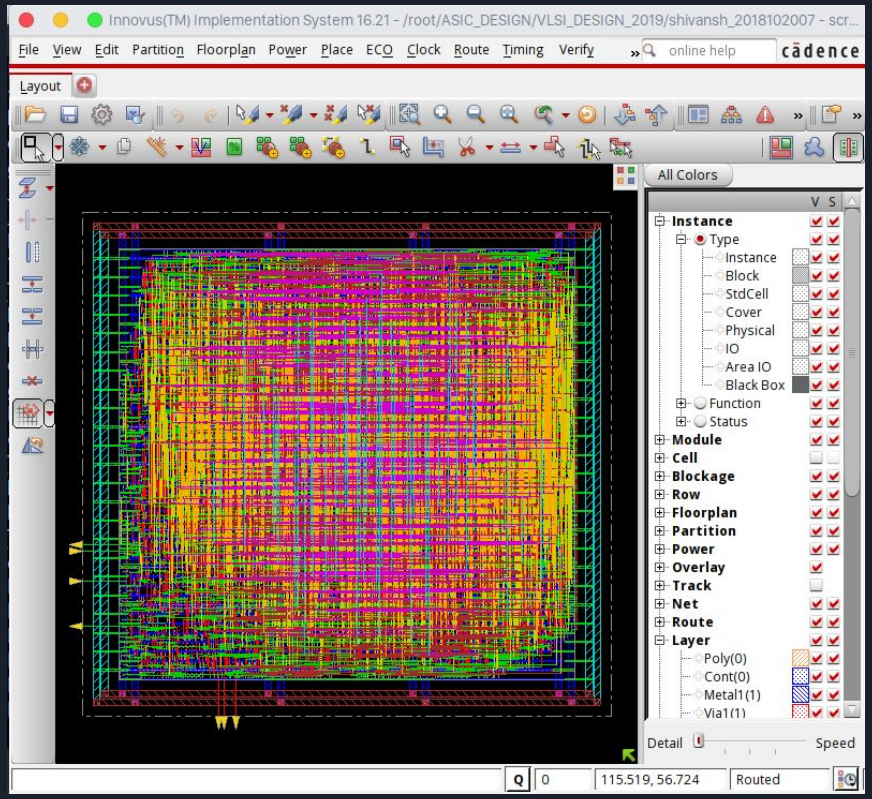


the Biggest Bitmaps processed yet!

Innovus Layout of the circuit used for processing the previous image



RESULTS

& Comparison with Unoptimized Project

PRE-OPTIMIZATION REPORTS

TOOL USED	AREA(μm^2)
GENUS	1069 + 981 = 2050
INNOVUS	1069.4997 + 980.9424 = 2050.3921

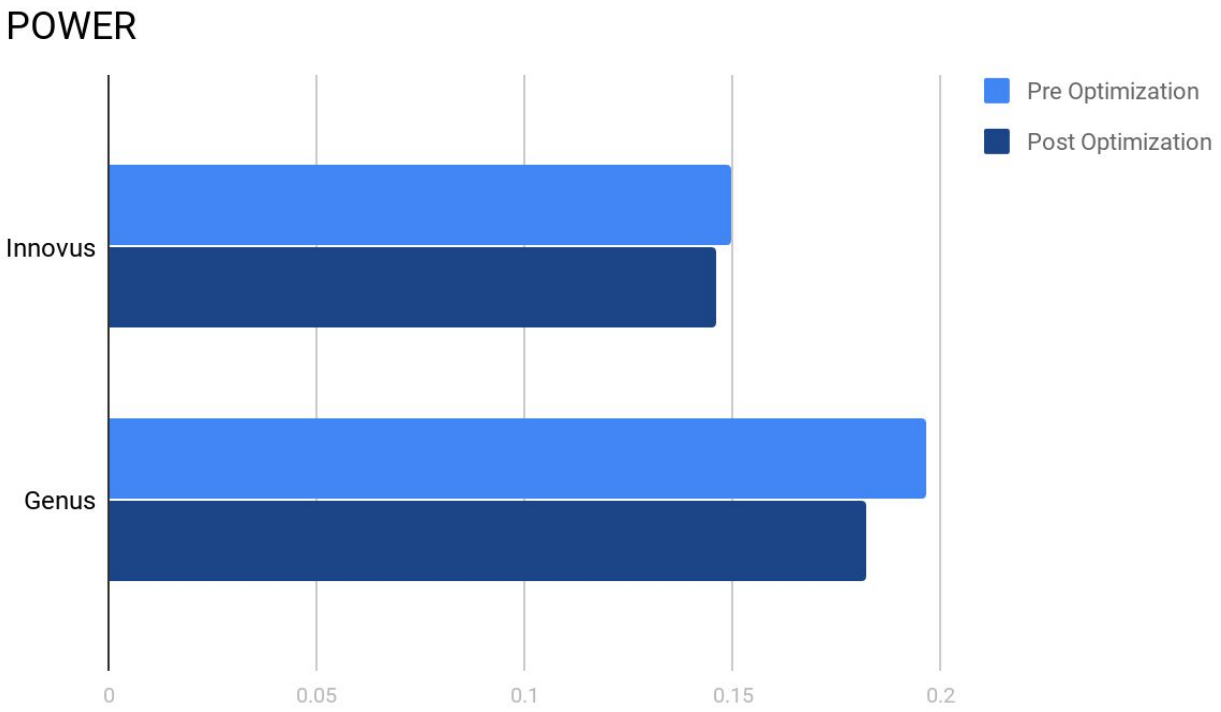
TOOL USED	POWER
GENUS	0.1965mW
INNOVUS	0.1493mW

POST-OPTIMIZATION REPORTS

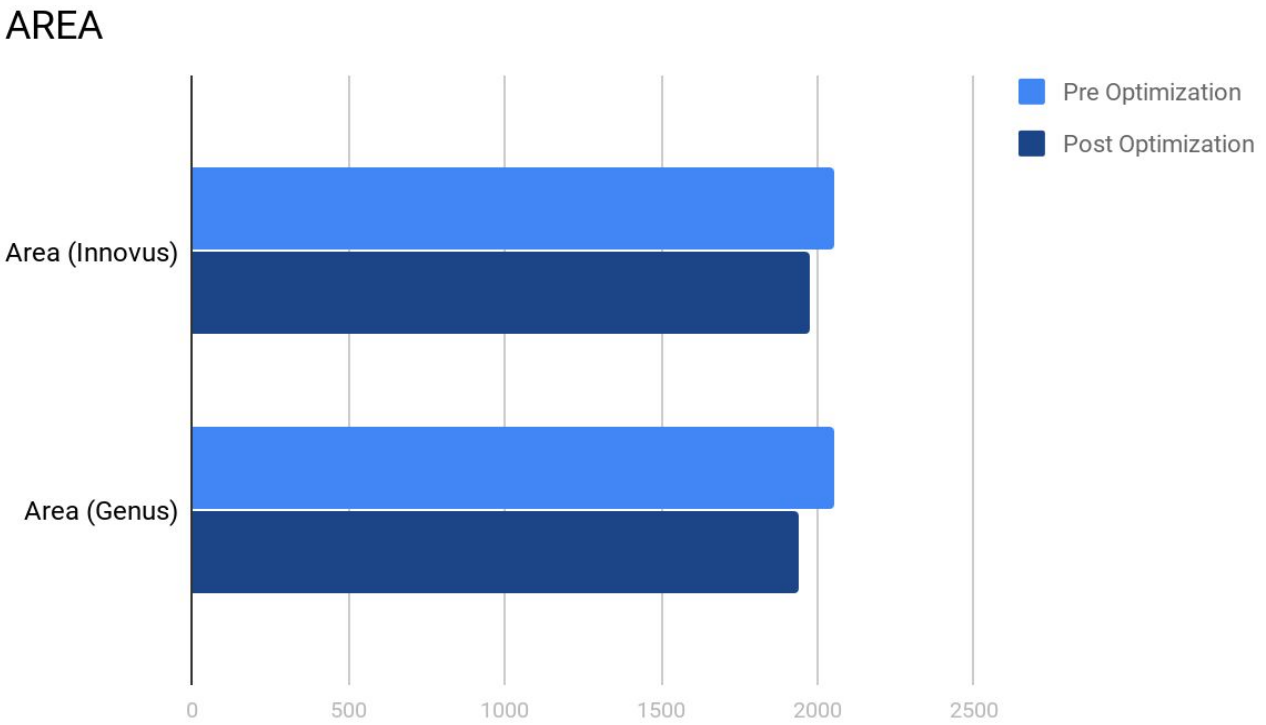
TOOL USED	AREA(μm^2)
GENUS	1010 + 928 = 1938
INNOVUS	1030.1409 + 948.3957 = 1978.5366

TOOL USED	POWER
GENUS	0.1819 mW
INNOVUS	0.1459 mW

RESULT SUMMARY (POWER)



RESULT SUMMARY (AREA)



Thank You!