

VLSI Assignment - 7 Report

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1 Aim

The aim of this assignment is to design ASIC(from Verilog code till GDSII File) using Cadence and perform full FPGA Flow(from Verilog to Dumping code into FPGAs) for the following Digital Blocks:

1. Universal Shift Register

- Design using Logic gates & FF's

2. FSM

- It is to be implemented as a Moore machine
- CLK used to clock the FSM
- RESET asserted high to reset the FSM to its initial state
- ONE asserted high to input a "1".
- OUT asserted high when at least two "0"s and two "1"s have occurred as inputs.
- Assuming that all inputs have been externally synchronized with CLK.

2 Introduction

For this assignment, **Xilinx ISE** and **Cadence** will be used to do the following:

1. Xilinx ISE

- (a) Create and submit **Verilog Code, Testbench & Implementation Constraints File**
- (b) Take screenshots of **RTL Schematics & Timing Diagram** depicting all logic gates present in the design and all possible combinations of test inputs, respectively
- (c) Report **Area, Power & Delay** of the design

2. Cadence

- (a) **Genus**
 - i. **Area, Power & Timing** Reports
 - ii. **Netlist** generated
 - iii. Screenshot of **RTL Schematic**
- (b) **NCLaunch**
 - i. Screenshot of **Timing Diagram**
- (c) **Innovus**
 - i. **Area & Power** report
 - ii. **Timing**(pre-place, post-place, post-rout, & sign-off) report
 - iii. Screenshot of **Physical Design**

3 Procedure

The following procedure will be followed:

1. Write the required Verilog code and testbench using **Xilinx ISE**
2. Using the above, generate the RTL Schematics and Timing Diagram in Xilinx
3. The Area, Power & Delay reports can also be generated now
4. Using the Verilog code already written, use **Cadence NCLaunch** to generate a Timing Diagram
5. Next, use **Cadence Genus** to generate Area, Power and Timing reports of the gates and sequential circuits generated. The netlist will also be generated here
6. Use the generated netlist with **Cadence Innovus** to optimize the design. The Timing reports for pre-placement, post-placement, pre-route, post-route & sign-off are then generated along with the Power and Area reports. The optimized netlist is also generated.
7. **Cadence Innovus** will also generate the physical design

4 Result & Discussion

The attached screenshots show the values for the function for all values of the input.

Tabulating the values observed in the reports from Genus(without optimization) and Innovus(with optimization):

Design	Genus		Innovus	
	Area(<i>units</i>)	Power(<i>nW</i>)	Area(<i>units</i>)	Power(<i>nW</i>)
Shift Register	148	4008.869	148.3524	3912
FSM	182	5054	174.087	4704.965

1. We observe that the **power** dissipated by the design is proportional to the **area/size** of the design.
2. We can also observe that the power consumed by the design **can be significantly reduced** by optimizing the design.

5 Conclusion

We can conclude that:

- The required designs were successfully implemented using **Xilinx ISE** and **Cadence**
- We can construct more complicated circuits using self-made building blocks

- The power dissipated by the circuits is **proportional** to the size of the design
- The power consumption of the design can be significantly reduced by **optimizing the design** appropriately

6 References

1. *www.asic-world.com*
2. *www.xilinx.com*
3. *www.cadence.com*
4. *electronics.stackexchange.com*
5. *Tutorials and Lab Sessions*