VLSI Assignment - 1 Report

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1 Aim

The aim of this assignment is to write Verilog code and testbench for the following combinational gates:

AND, OR, NOR, NAND, XOR, NOT and **XNOR**.

We also want to write Verilog code and test bench for the following compound combinational circuits.

1. **Y = AB + CD**
2. **Y = (ABC + DE).F**
3. **Y = ((A+B')(CD+E))'**

We will also write their truth table and find the:

- RTL Schematics
- Area
- Power
- Timing Diagram

2 Introduction

For this assignment, we will be using **Xilinx ISE**, and **Cadence**.
We will generate the following using Xilinx ISE:

- RTL Schematics
- Timing Diagram

We will generate the following using **Cadence**:

- Area Report
- Power Report
- Timing Report
- Netlist

3 Procedure

The following procedure will be followed:

1. Write the required Verilog code and testbench using **Xilinx ISE**
2. Using the above, generate the RTL Schematics and Timing Diagram in Xilinx
3. Using the Verilog code already written, use **Cadence NCLaunch** to generate a Timing Diagram
4. Next, use **Cadence Genus** to generate Area, Power and Timing reports of the gates and combinational circuits generated. The netlist will also be generated here
5. Use the generated netlist with **Cadence Innovus** to optimize the design. The Timing reports for pre-placement, post-placement, pre-rout and post-rout are then generated along with the Power and Area reports. The optimized netlist is also generated.

4 Result & Discussion

The attached screenshots show the values for the function for all values of the input(thus generating the required truth table).
Tabulating the values observed in the reports from Genus(without optimization) and Innovus(with optimization):

Design	**Genus**		**Innovus**	
	Area*(units)*	**Power***(nW)*	**Area***(units)*	**Power***(nW)*
AND	5	112.983	4.5414	90.69
OR	5	135.769	4.5414	135.2
NOR	3	92.834	3.027	89.96
NAND	3	69.083	3.027	49.93
XOR	8	340.607	8.325	235.4
NOT	2	53.174	2.270	48.51
XNOR	8	204.259	7.569	134.3
F1	8	218.452	7.569	169.8
F2	11	325.562	11.353	213.6
F3	13	367.735	12.867	285.3

1. We observe that the **power** dissipated by the design is proportional to the **area/size** of the design.
2. We can also observe that the power consumed by the design **can be significantly reduced** by optimizing the design.

5 Conclusion

We can conclude that:

- The required designs were successfully implemented using **Xilinx ISE** and **Cadence**
- The power dissipated by the circuits is **proportional** to the size of the design
- The power consumption of the design can be significantly reduced by **optimizing the design** appropriately

6 References

1. *www.asic-world.com*
2. *www.xilinx.com*
3. *www.cadence.com*
4. *electronics.stackexchange.com*
5. *Tutorials and Lab Sessions*