VLSI Assignment - 2 Report

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Contents

1 Aim

The aim of this assignment is to design ASIC(from Verilog code till GDSII File) using Cadence and perform full FPGA Flow(from Verilog to Dumping code into FPGAs) for the following Digital Blocks:

1. **MUX** - 2*1, 4*1, 8*1
   - Design 2*1 MUX using Logic gates
   - Create 4*1 MUX using 2*1 MUXs
   - Create 8*1 MUX using 4*1 & 2*1 MUXs
2. **DEMUX** - 1*4, 1*4, 1*8
   - Design 1*2 DEMUX using Logic gates
   - Create 1*4 DEMUX using 1*2 DEMUXs
   - Create 1*8 DEMUX using 1*2 & 1*4 DEMUXs
3. **DECODER** - 1*2, 2*4, 3*8
   - Design 1*2 DECODER using Logic gates
   - Create 2*4 DECODER using 1*2 DECODERs
   - Create 3*8 DECODER using 1*2 & 2*4 DECODERs

   It will also have an *Enable* pin.
4. **PRIORITY ENCODER** - 3*8
   - Design 3*8 PRIORITY ENCODER using Logic gates

   It will also have an *Enable* pin.

2 Introduction

For this assignment, **Xilinx ISE** and **Cadence** will be used to do the following:

1. **Xilinx ISE**
   (a) Create and submit **Verilog Code**, **Testbench** & **Implementation Constraints File**
   (b) Take screenshots of **RTL Schematics** & **Timing Diagram** depicting all logic gates present in the design and all possible combinations of test inputs, respectively
   (c) Report **Area**, **Power** & **Delay** of the design

2. **Cadence**
   (a) **Genus**
      i. **Area**, **Power** & **Timing** Reports
      ii. **Netlist** generated
      iii. Screenshot of **RTL Schematic**
   (b) **NCLaunch**
      i. Screenshot of **Timing Diagram**
   (c) **Innovus**
      i. **Area** & **Power** report
      ii. **Timing**(pre-place, post-place, post-rout, & sign-off) report
      iii. Screenshot of **Physical Design**

3 Procedure

The following procedure will be followed:

1. Write the required Verilog code and testbench using **Xilinx ISE**
2. Using the above, generate the RTL Schematics and Timing Diagram in Xilinx
3. The Area, Power & Delay reports can also be generated now
4. Using the Verilog code already written, use **Cadence NCLaunch** to generate a Timing Diagram
5. Next, use **Cadence Genus** to generate Area, Power and Timing reports of the gates and combinational circuits generated. The netlist will also be generated here
6. Use the generated netlist with **Cadence Innovus** to optimize the design. The Timing reports for pre-placement, post-placement, pre-rout, post-rout & sign-off are then generated along with the Power and Area reports. The optimized netlist is also generated.
7. **Cadence Innovus** will also generate the physical design

4 Result & Discussion

The attached screenshots show the values for the function for all values of the input.
Tabulating the values observed in the reports from Genus(without optimization) and Innovus(with optimization):

Design	Genus		Innovus	
	Area*(units)*	**Power***(nW)*	**Area***(units)*	**Power***(nW)*
MUX(2x1)	7	221.427	6.8121	193.1
MUX(4x1)	20	880.651	20.4363	623.7
MUX(8x1)	48	1706.430	47.6847	1548
DEMUX(1x2)	9	241.631	9.0828	204.2
DEMUX(1x4)	27	695.922	27.2484	611
DEMUX(1x8)	64	1571.074	63.5796	1207
DECODER(1x2)	9	241.631	9.0828	206.8
DECODER(2x4)	27	679.918	27.2484	602.1
DECODER(3x8)	64	1432.922	63.5796	1203
PRIORITYENCODER(3x8)	51	1503.507	50.7123	1216

1. We observe that the **power** dissipated by the design is proportional to the **area/size** of the design.
2. We can also observe that the power consumed by the design **can be significantly reduced** by optimizing the design.

5 Conclusion

We can conclude that:

- The required designs were successfully implemented using **Xilinx ISE** and **Cadence**
- We can construct more complicated circuits using self-made building blocks
- The power dissipated by the circuits is **proportional** to the size of the design
- The power consumption of the design can be significantly reduced by **optimizing the design** appropriately

6 References

1. *www.asic-world.com*
2. *www.xilinx.com*
3. *www.cadence.com*
4. *electronics.stackexchange.com*
5. *Tutorials and Lab Sessions*