J, H-Section Solution.

National University of Computer and Emerging Sciences, Lahore Campus

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Exam:	Quiz 07	Roll No.	

Instruction/Notes:

Question 01: Let us consider the following decomposition of the instruction processing

Fetch Instruction (FI): Read the next expected instruction into a buffer.
Decode Instruction (DI): Determine the opcode and the operand specifiers.
Fetch Operands (FO): Calculate the effective address of each source operand and fetch each operand from the memory. Operand in registers need not to be fetched.
Execute Instruction (EI): Perform the indicated operation and store the result if any, in the specified destination operand location.
Write Operand (WO): Store the result in memory.
Given below is a set of instructions. There implementation through pipelining has some data hazards. You have to solve those hazards by using ~~any~~ technique.

I1: mov word [sum], ax
I2: sub word [sum], dx
I3: mov word [sum], 01
I4: add bx, [sum]

(Data Forwarding)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
I1	FI	DI	FO	EI	WO										
I2		FI	DI	FO	EI	WO									
I3			FI	DI	FO	EI	WO								
I4				FI	DI	FO	EI	WO							

Question 02: There are 128 blocks in a cache memory, which can store one word each. To which block number does main memory word address 900 would map in the case of a direct mapped cache?

900 % 128 = 4