ENCS333 Project , 2nd Semester 2021

Project:

Teams of 3 students design and implementation while optimizing for speed, area, and/or power. Group collaboration and engineering design for one of the idea only below:

1. **Project 1: Low power cam design using 9T SRAM cell**

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2. **Project 2: Design of a 2-bit binary parallel ripple carry adder using CMOS NAND gates with Microwind (process need to be less than 25nm) and EDA tool for verification.**

GRADES: Grading is based upon the following factors

- In-class presentations on Jun1 and Jun 3rd , sign up on the sheet and fill all needed field, power , area speed in this link https://docs.google.com/spreadsheets/d/1V0C8rJUBFlPlVkP5msyjHoZ-FEp8wtdoiZPwF_CqFNI/edit?usp=sharing
- **Report need to be submitted on or before May 31st**
- Status reports and final project report in the paper format using Turnitin , less than 20%similiarity, more than that will no be accepted
- Technical competency in pursuing project goals
- Proficiency in collaboration, as measured by overall project integration and success

Grading:

- **Final Report -IEEE format** cover all needed data as specified below , similar to the paper loaded to you
- Introduction/comparison ____ / 10
- Specifications and results
  - Area ____ / 10
  - Delay ____ / 10
  - Size ____ / 10
- Schematic Quality/size ____ / 10
- Layout Quality/optimized ____ / 10
- Implementation
  - RC Models ____ / 10
  - Test Cases ____ / 10
  - Spice Simulation ____ /10
  - Result/conclusion ____ / 10

- **Total** ____ **/ 100**
- Innovation in the design +20
- **Presentations : Print summary of your report , it should include all sections as mentioned above**
    - **Design**
    - **Power**
    - **Area**
    - **Speed**
    - **Optimization**
- **Note: we need Spice simulation for schematic**