# Electronic Devices and Circuits 1 2EI4
# Project 2
# “Ideal” Voltage Controlled Switches

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Ahmad Molhim, molhima, 400440228]**

## Properties of Ideal Switch

An ideal switch is a switch that does not consume or dissipate power from the source and supplies the whole power to the load, Therefore, it is always desirable to have switches perform as close as possible to ideal switches. To do so the switch must posses the properties of an “Ideal Switch”. An ideal switch should have zero resistance when its closed or in its “ON” state, meaning that it allows an infinite amount of current to flow without any resistance which results in no power dissipation, Infinite resistance when it’s open or in its “OFF” state, meaning that the switch does not allow any current to flow when it’s open, forming a complete break in the circuit. The Ideal switch must have no time delay when changing between its states, however this feature is very hard to implement in real life as there will always be time delay due to mechanical or electronic factors. The voltage drop across the terminals of the switch must be zero when the switch is in its “ON” state regardless of the surrounding circuit, and there should be no limit on the amount of device-voltage in the “OFF” state so that the switch blocks any voltage without allowing any current to flow. Simply put an Ideal Switch must have limitless speed, unlimited power handling capabilities and operates at 100% efficiency.

While the concept of an ideal switch is beneficial in theory, the actual performance of real switches can be influenced by non-ideal characteristics in electronic circuits, for example switches will always have contact resistance when they’re “ON” leading to voltage drops and power dissipation affecting the performance of the circuit. They also have finite leakage current meaning that a small amount of current may flow through the switch even in its “OFF” state, this leads to potentially compromising the efficiency and performance of the circuit. Moreover, as discussed before about the time delay when the switch changes states, one of the electronic features that cause a time delay is the capacitance. Capacitors could cause a time delay due to their charging and discharging times. The resistance of the load is also a reason for the time delay as it impacts the time the switch reaches a steady state. This time delay could impact the overall operational speed of the circuit. Another non-ideality is the contact bounce which happens due to the rapid and repeated opening and closing of the switch, and it could cause electrical noise causing interference with nearby components and signals affecting the overall performance of the circuit. Considering these non-idealities is crucial in circuit design, as they can impact the overall efficiency of the circuit.

# Test Plan for Switch 1:

## Voltage drop when switch is “ON”:

Use the oscilloscope Channels 1 and 2 to measure the difference between V1 and V2, with Vsupply at 5V and Vcontrol at 0V.

## Current leakage When Switch is “OFF”:

Measure the voltage at V1 when switch is “OFF” at Vcontrol = 5V, then use Ohm’s law to obtain leakage current.

## Power Dissipated:

Measure the voltage at V1 when switch is “OFF” at Vcontrol = 5V, then calculate the power using $P = V^2/R$.

## Switching Time:

Measure the time it takes the switch to change from one state to another using the data feature on Waveforms.

# Test Plan for Switch 2:

## Voltage drop when switch is “ON”:

Use the oscilloscope Channels 1 and 2 to measure the difference between V1 and V2, with Vsupply at 5V and Vcontrol at 0V.

## Measure the resistance of the switch when it’s ON:

Measure the voltage drop when the switch is “ON” at Vcontrol = 0V, and Vsupply = 5V. Then use the voltage drop value to determine the resistance.

## Current leakage When Switch is “OFF”:

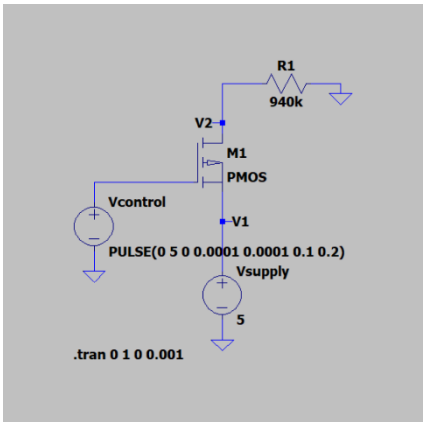
Measure the voltage at V1 when switch is “OFF” at Vcontrol and Vsupply = 5V, then use Ohm’s law to obtain leakage current.

## Switching Time:

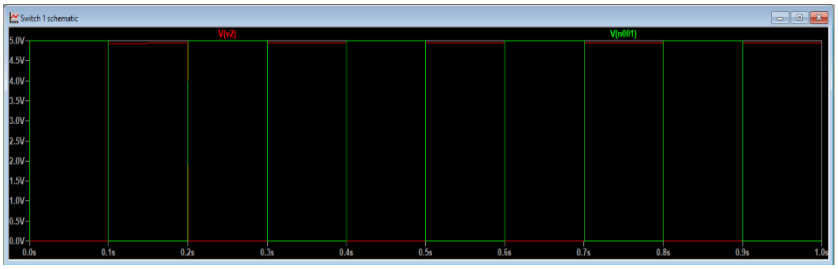
Measure the time it takes the switch to change from one state to another using the data feature on Waveforms

# Switch 1 Circuit Schematic

## LTSpice Simulation

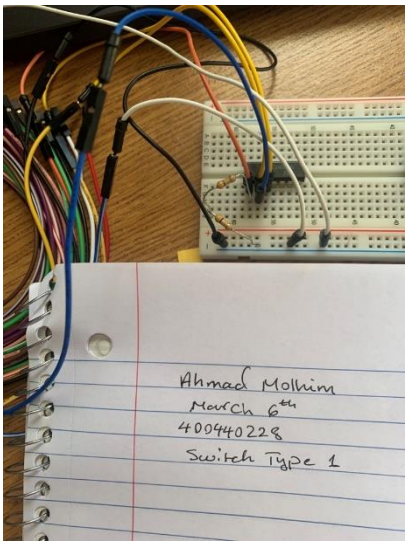



*This is a picture of Switch 1 schematic.*

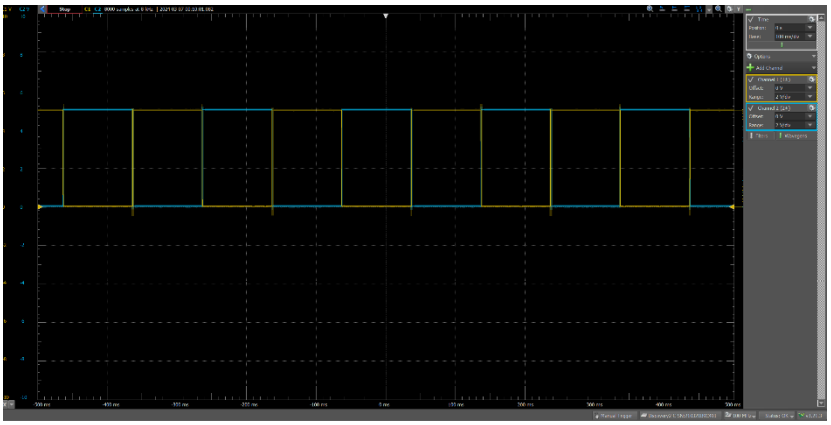



*LTSpice simulation of circuit behavior, measuring the voltage at Vcontrol and V2*

## Physical Circuit



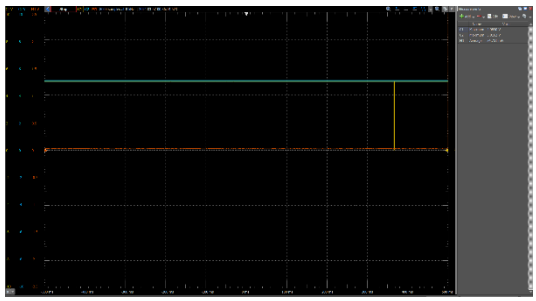
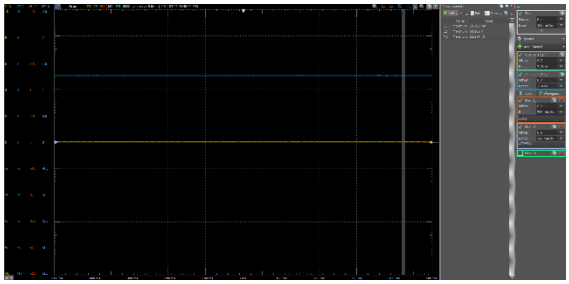
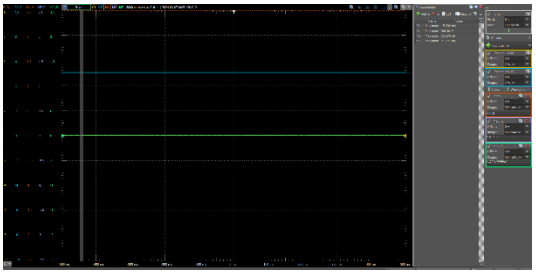

*Picture of physical circuit built on a breadboard.*



*Simulation of circuit behavior using Waveforms and AD2, measuring voltage*

The behavior of the circuit shows that V2 and V1 should be 0V when Vcontrol = 5V and vice versa. When the switch is closed, in its “ON” state V1=V2, and i1=i2=0 when the switch is open in its “OFF” State. To minimize the leakage current, a high resistance of 940K was used. This basic behavior of the circuit was shown using the LTSpice simulation and Waveforms simulation using a built physical circuit.

# Measurements Performed According to Test Plan

| Test | Results | Proof |
|---|---|---|
| Voltage Drop when Switch is “ON | Created a Math Channel on Waveforms to calculate the difference between V2 and V1 when Vcontrol = 0V and Vsupply = 5V<br><br>Voltage drop in “ON” sate = 24.57mV |  |
| Current Leakage when Switch is “OFF” | Created a Math Channel on waveforms that calculate the current using Voff/R when Vcontrol = 5V and Vsupply = 5V<br><br>Current leakage = 16.37nA |  |
| Power Dissipated | Created a Math Channel on Waveforms to calculate the power using $Voff^2/R$<br><br>Power Dissipated = 2.127uW |  |
| Switching Time between States | Used The Data feature on Waveforms to measure the time it takes for the switch to change states.<br><br>Switching time = 0.03s | Data Was too big couldn’t the transition between states will not fit in one picture |

## Theoretical Explanation

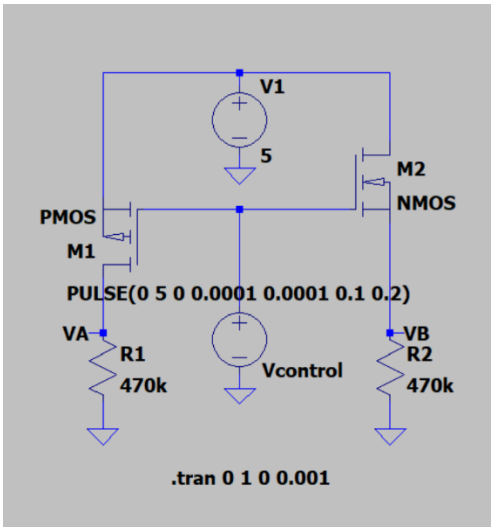
After testing the designed circuit of the switch on a breadboard it appeared to me that the discrepancies between the behavior of the physical circuit and the Ideal switch are mostly due to the behavior of the components used and the material they were made of. For example, an Ideal switch will have no voltage drop across its terminals when the switch is “ON”. However, as shown above the voltage drop across the closed terminals of the switch was 24.57mv which is a very low amount of voltage, yet it does not represent the behavior of an Ideal Switch. This voltage drop could be attributed to the internal resistance of the MOSFET used which we cannot do anything about. The test result also showed that there was a current leakage of 16.37nA which also conflict with the properties of the ideal switch. The power dissipated by the switch was shown to be 2.127uW which is also due to the internal resistance of the MOSFET, and this shows the inefficiencies of the used components which show how these affected the main objective of this project, which is creating an Ideal switch, since ideal switches will have 0 power loss. Moreover, the transition time between the switch’s states was also tested, switching time was measured to be 0.03s which is not the same as that of an ideal switch which has a switching time of 0s. The delay in transitioning between the states is mostly due to mechanical properties of the switch but could also be due to electrical properties such as capacitance. All the points discussed above are reasons to why it is almost impossible to create an Ideal Switch

## Design Trade-offs

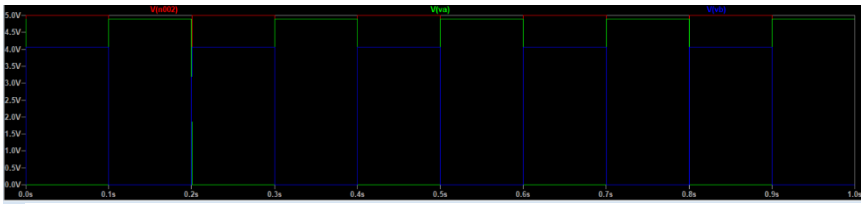
A single p-channel MOSFET with two 470k resistors were used to create this circuit, which provides a cheaper design due its simplicity and low complexity meaning that it will require less time and effort to build and test. A low complex design could also lead to cost savings since less components are being used, and enhanced reliability as there are fewer points of potential failure. From a user perspective, a less complex and more intuitive design can improve user experience and accessibility. Using high resistance in such a circuit has its advantages and disadvantages. The higher the resistance used the lower the leakage current will be leads to a more accurate outcome which ensures that the switch is operating within its parameters and getting closer to its optimal behavior, however using higher resistance can be more expensive especially at very high resistance values causing the design cost to increase. High resistance values could also increase the time delay of the operations.

# Switch 2 Circuit Schematic

## LTSpice Simulation

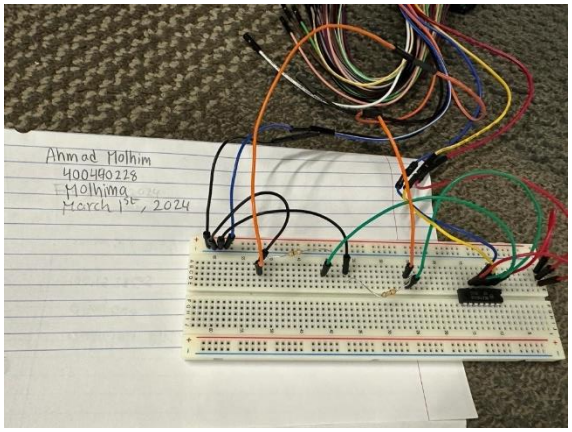



*Picture of switch 2 schematic on LTSpice.*

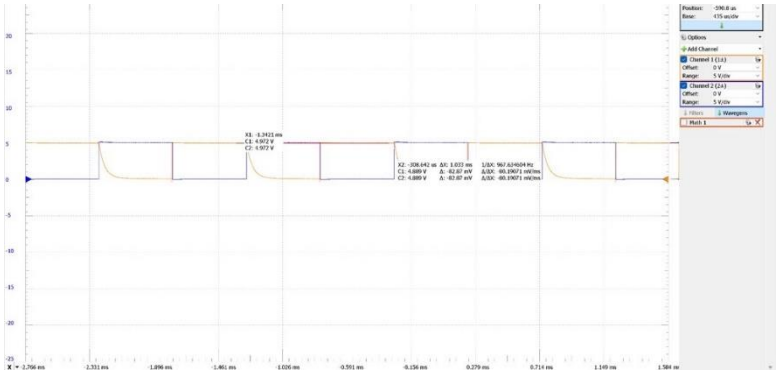


*Simulation of basic behavior of circuit using LTSpice simulator*

## Physical Circuit




*Picture of physical circuit built on a breadboard.*



*Simulation of circuit behavior using Waveforms and AD2, measuring voltage*

The basic behavior of the circuit shows that when Vcontrol = 5V, VA should be 0V, when Vcontrol and V1 are measured.

## Measurements Performed According to Test Plan

| Test | Results |
|---|---|
| Voltage drop when switch is “ON”: | Measured the voltage drop between V1 and V2 to be 24mV |
| Current Leakage when switch is “OFF”. | Current leakage was measured to be 0.06uA |
| Measure the resistance of the switch when it’s ON | Using Von and $I_{leakage}$, Ron was calculated to be 1.79kΩ |
| Switching Time | 0.01728 - 0.01532 = 0.0196ms |

## Theoretical Explanation

The observations from the test show that switch non-idealities should always be taken into consideration when creating a switch to come out with the most accurate results possible, since it is almost impossible to create an ideal switch that has no current leakage, or internal resistance or voltage drop in the “ON” state or switch instantaneously. This is due to the behavior of the components used and their material imperfection in the design and many other electrical or mechanical properties.

## Design Trade-offs

In this switch design I used to MOSFETS, one n-channel MOSFET and one p-channel MOSFET to produce a dual-output switch. The use of two MOSFETS together resulted in a lower output voltage. In this design I aimed for a simple and low complex design by only using, two MOSFETS and two resistors. However, in this case the simplicity and low cost of the design did not play in favor of the results, since there was a higher current leakage of 0.06uA, the current leakage could have been reduced by using diodes. Moreover, this design was constrained by the available components. The MOSFETS provided in the components kit affected the current leakage as the gates of these MOSFETS are not isolated enough. To come out with the lowest possible current leakage an FGMOS (floating gate MOSFET) could be used, in comparison with the n-channel and p-channel MOSFET that we have, the FGMOS has a more isolated gate which will in return help reduce the current leakage.

# *References*

[1] F. Razaghian and S. Bonakdarpour, “Reducing the leakage current and PDP in the quasi-floating gate circuits,” in 2012 Spring Congress on Engineering and Technology, 2012, pp. 1–4.

[2] W. Storr, “MOSFET as a switch - using power MOSFET switching,” Basic Electronics Tutorials, https://www.electronics-tutorials.ws/transistor/tran_7.html (accessed Mar. 7, 2024).

[3] Mouser, https://www.mouser.com/datasheet/2/308/1/MC14007UB_D-2315408.pdf (accessed Mar. 8, 2024).