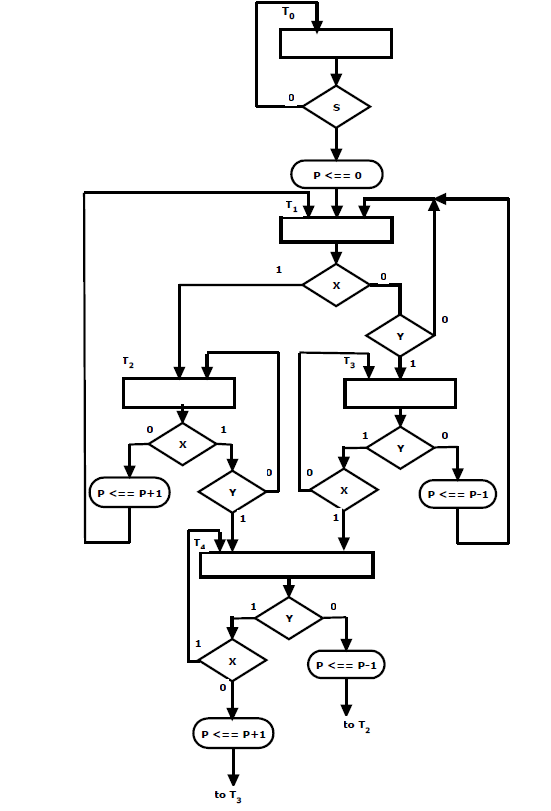
|  |  |  |
| --- | --- | --- |
| NAME | ID NUM | SEC |
| 1. أحمد عبد الله جبر القرم | 11819195 | 3/8:00-11:00 |
| - | - | - |

**Experiment 4**: Algorithmic State Machine (Car-Park)

**Introduction** :

In this lab , I will implement an algorithmic state machine (ASM) on the ZedBoard to implement a system that count the number of cars in a car-park.



**Tools used in Lap** :

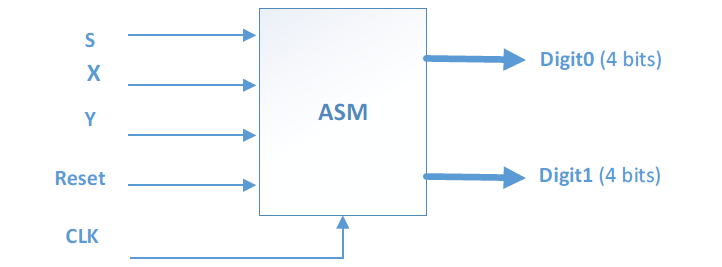
1. Computer lap.
2. Vivado software .
3. Zboard from Xilinx.
4. VHDL

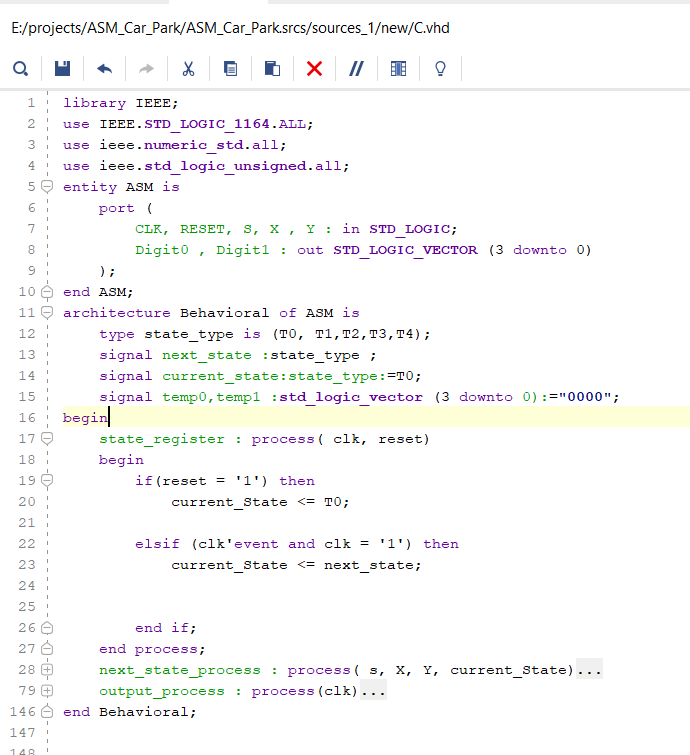
**Procedure :**

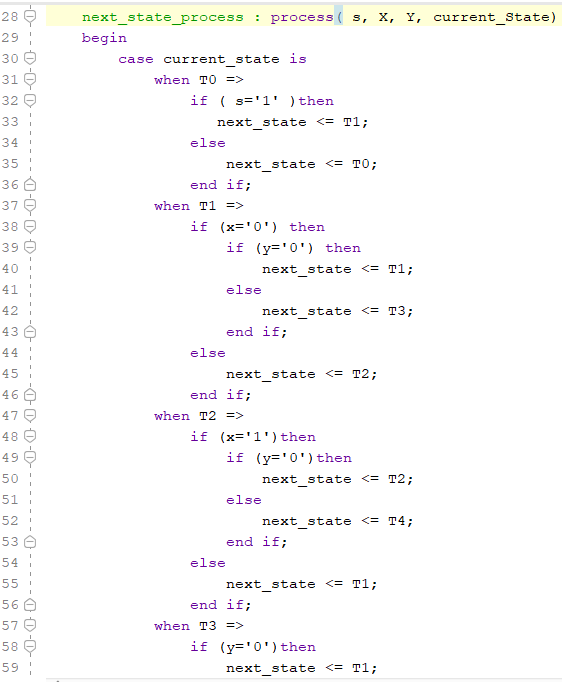
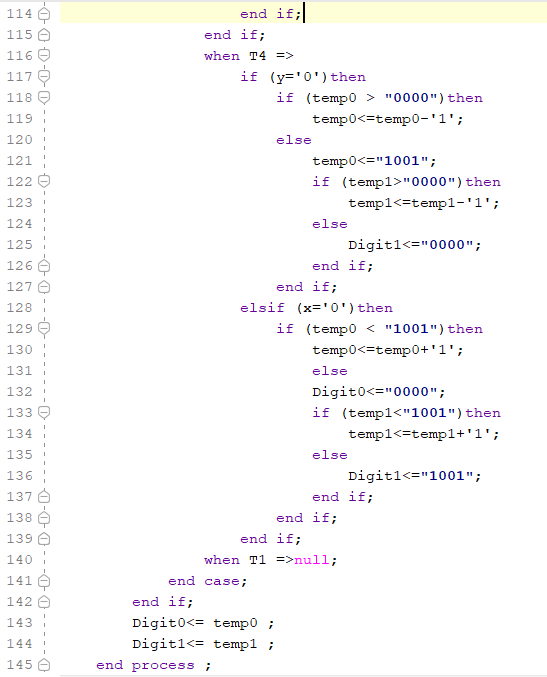
**Part 1** : ASM Simulation

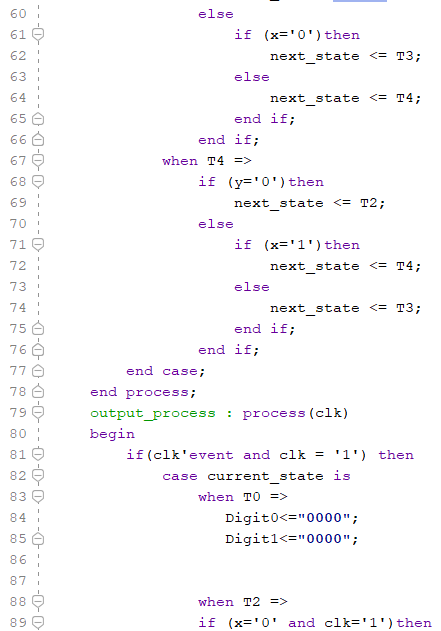
I implemented the given asm in vhdl

using 3 processe .

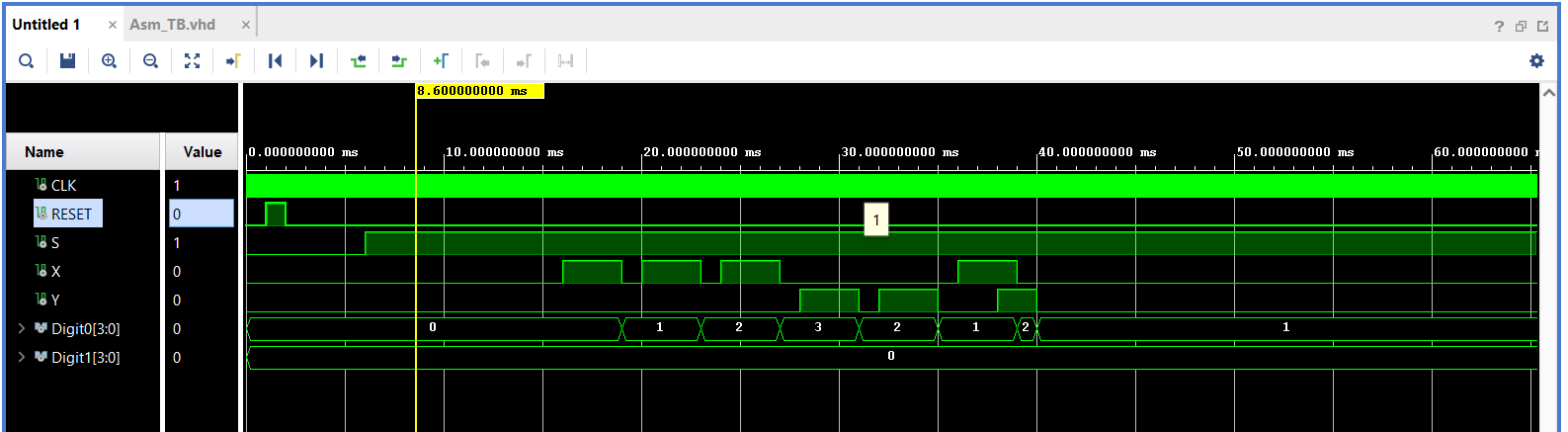


ASM Vhdl Code:



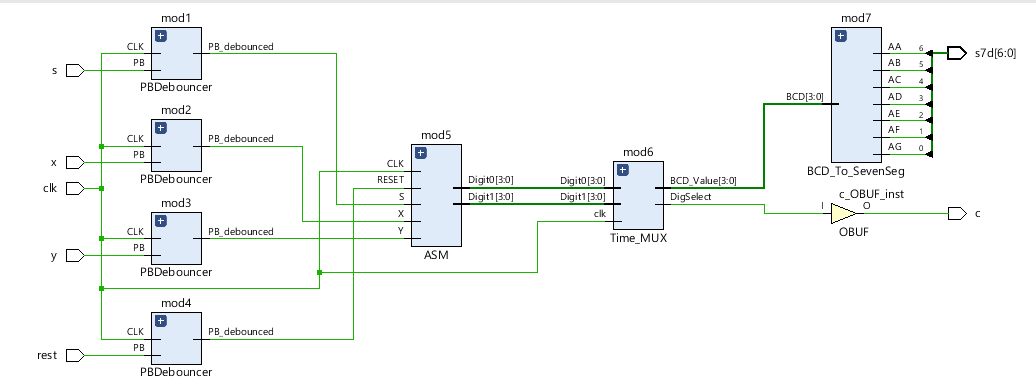


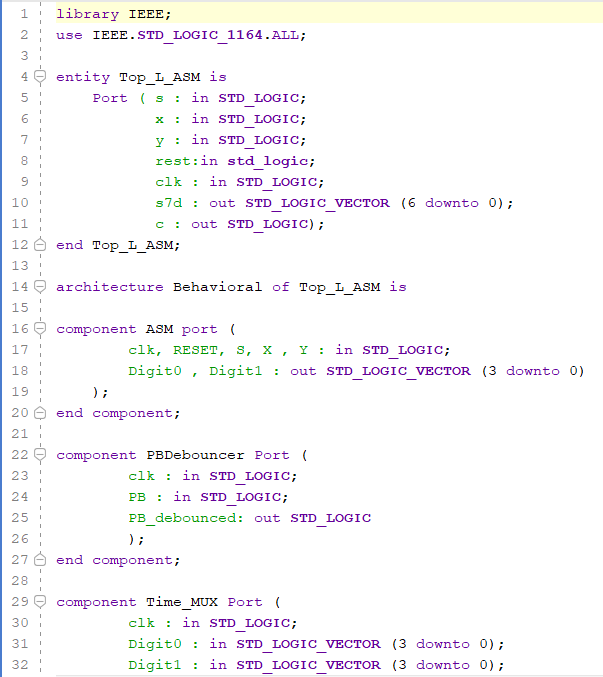
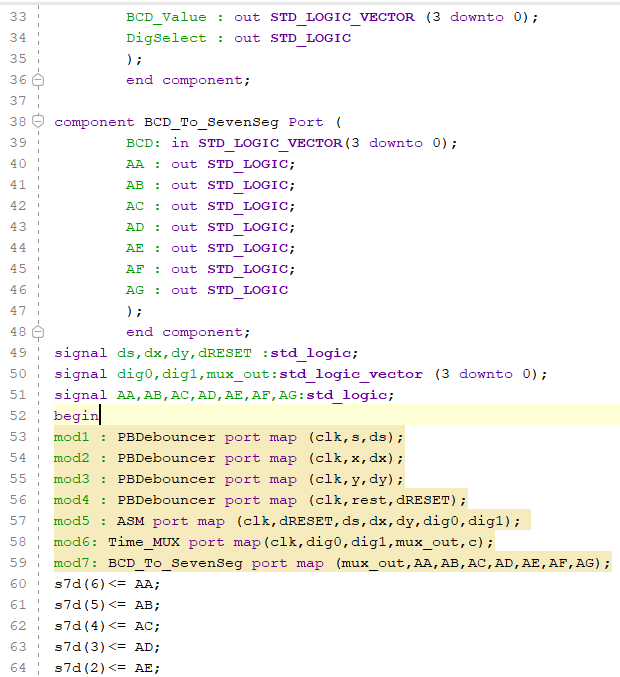


Asm Simulation :

**Part 2** : Top Level (ASM Car-Park )

I had created the Top level entity with four component :

1. PBDebouncer: to debounce the signals from the push buttons.
2. Time\_MUX: to select between the two digits (Tens and Ones) of the BCD counter.
3. BCD\_To\_SevenSeg:
4. The previous Asm component.

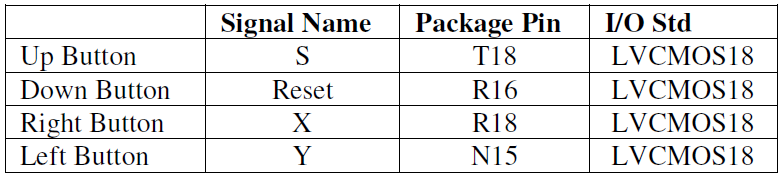
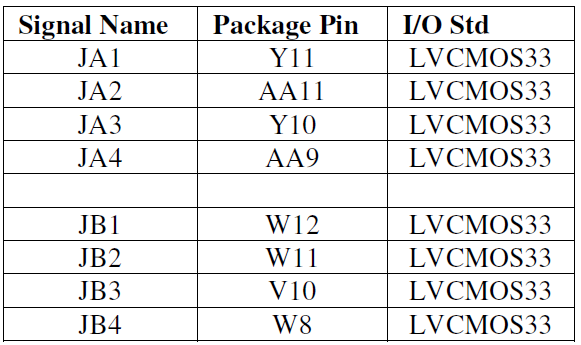
Top level Vhdl Code :

Top level simulation :



Synthesis, Implementation, and Bitstream Generation:

I had connected the Pins as shown :



**Conclusion:**

In this excrement I had learned how to create block that behave in a certain ASM chart (Algorithmic State Machine of Car-Park) .