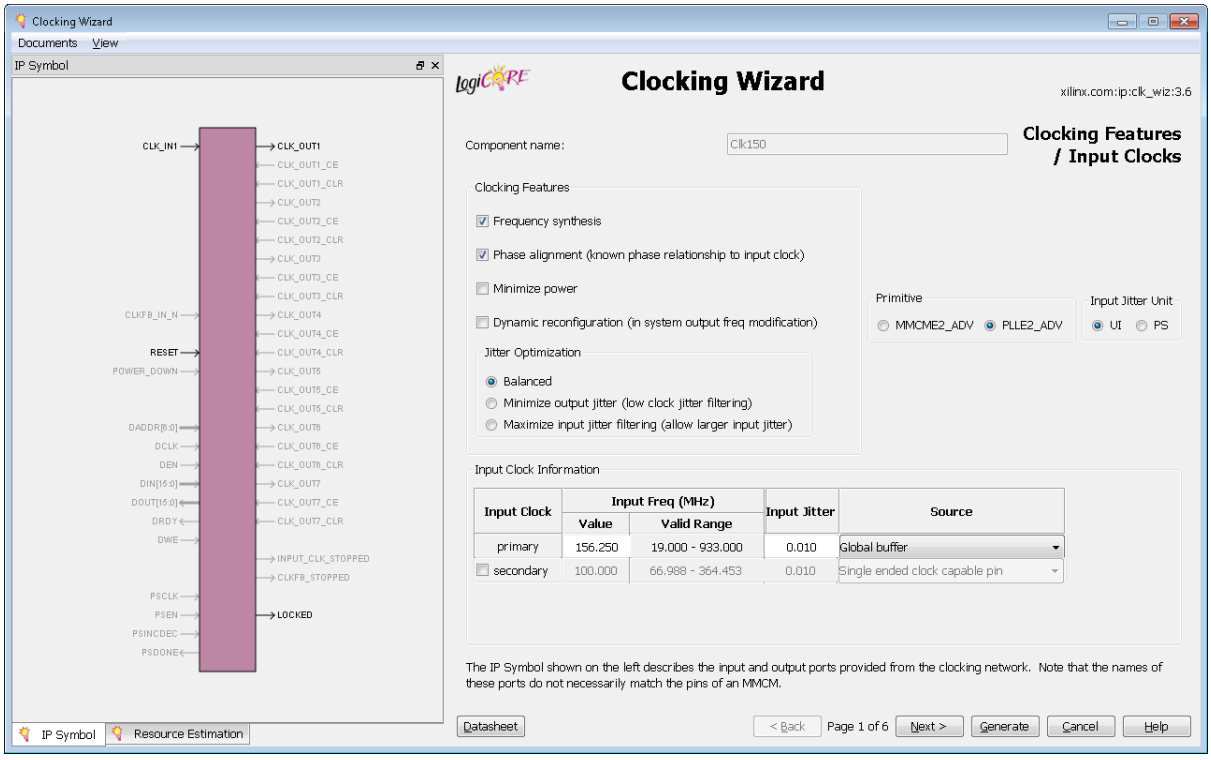
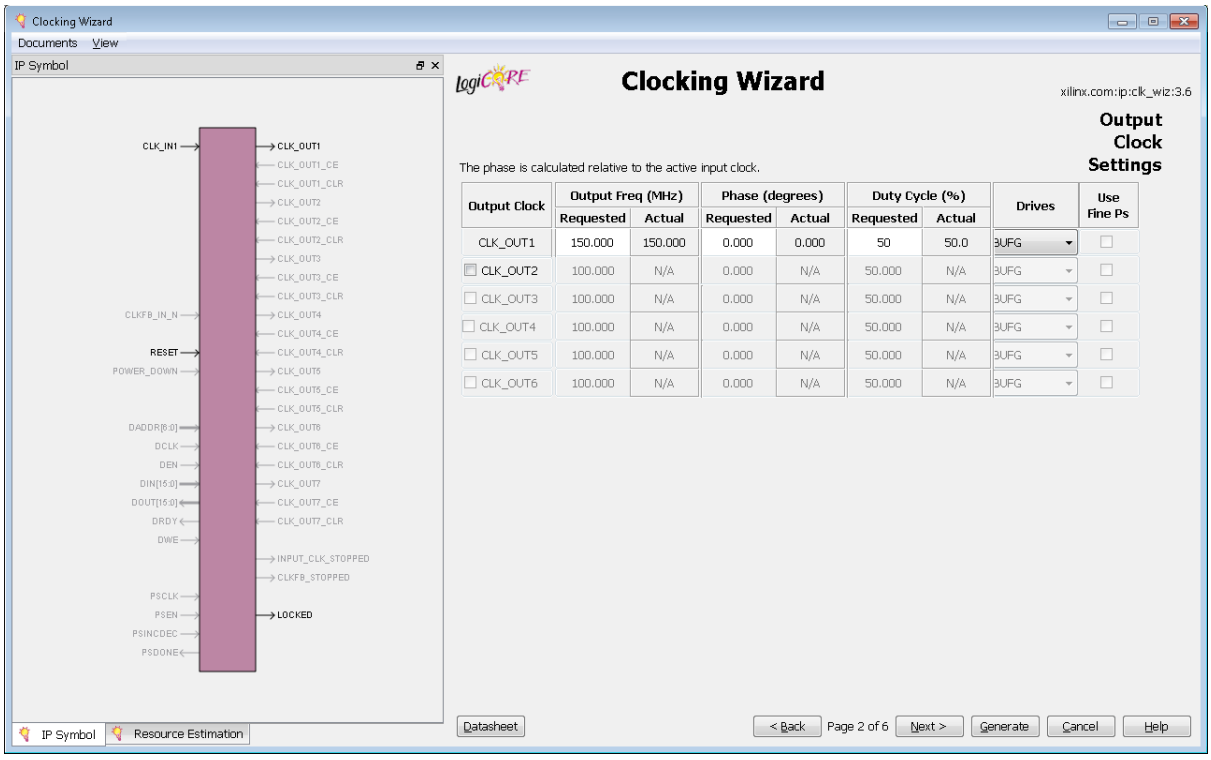
Steps to create Clk150 ip core:

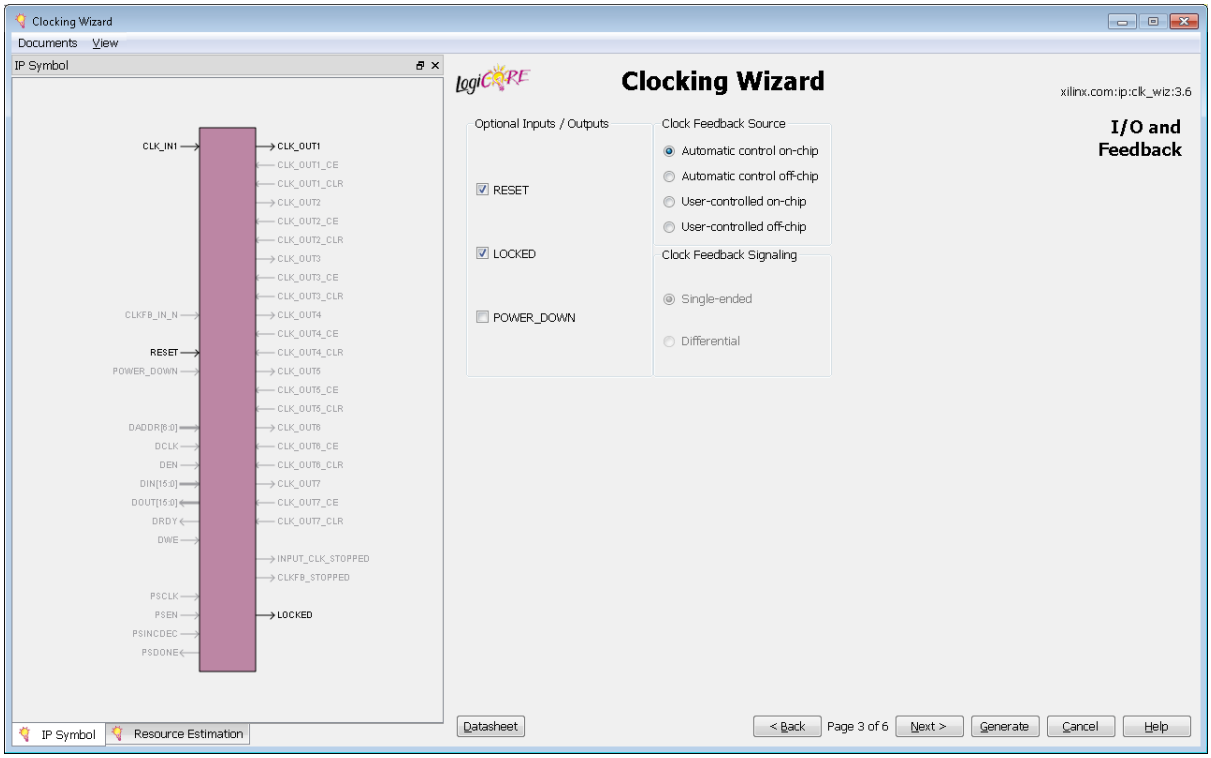
Step 1:



Step 2:



Step 3:


Clocking Wizard
Documents View
IP Symbol
CLK_IN1
CLK_OUT1
CLK_OUT1_CE
CLK_OUT1_CLR
CLK_OUT2
CLK_OUT2_CE
CLK_OUT2_CLR
CLK_OUT3
CLK_OUT3_CE
CLK_OUT3_CLR
CLKFB_IN_N
CLK_OUT4
CLK_OUT4_CE
RESET
CLK_OUT4_CLR
POWER_DOWN
CLK_OUT5
CLK_OUT5_CE
CLK_OUT5_CLR
DADDR[6:0]
CLK_OUT6
DCLK
CLK_OUT6_CE
DEN
CLK_OUT6_CLR
DIN[15:0]
CLK_OUT7
DOUT[15:0]
CLK_OUT7_CE
DRDY
CLK_OUT7_CLR
DWE
INPUT_CLK_STOPPED
CLKFB_STOPPED
PSCLK
PSEN
LOCKED
PSINCDEC
PSDONE
IP Symbol
Resource Estimation
LogiCORE
Clocking Wizard
xilinx.com:ip:clk_wiz:3.6
I/O and Feedback
Optional Inputs / Outputs
RESET
LOCKED
POWER_DOWN
Clock Feedback Source
Automatic control on-chip
Automatic control off-chip
User-controlled on-chip
User-controlled off-chip
Clock Feedback Signaling
Single-ended
Differential
Datasheet
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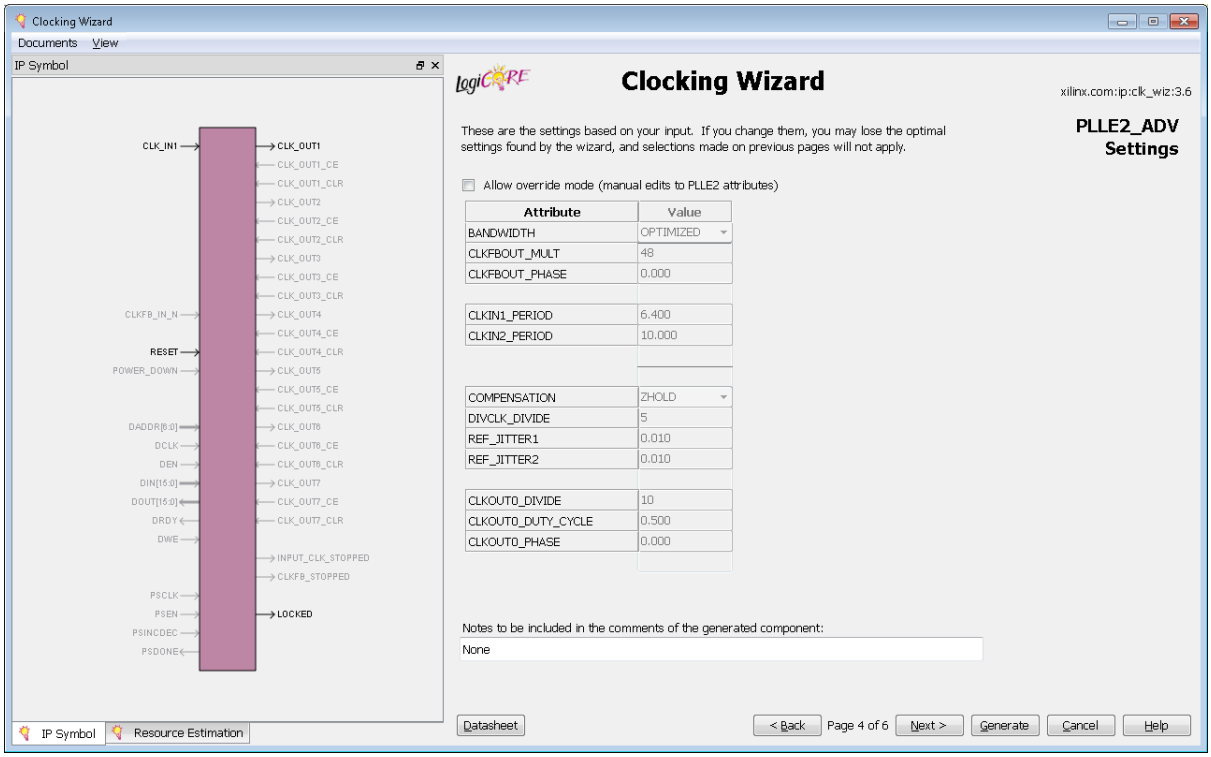
Generate
Cancel
Help

Step 4:


Clocking Wizard
Documents View
IP Symbol
CLK_IN1
CLK_OUT1
CLK_OUT1_CE
CLK_OUT1_CLR
CLK_OUT2
CLK_OUT2_CE
CLK_OUT2_CLR
CLK_OUT3
CLK_OUT3_CE
CLK_OUT3_CLR
CLKFB_IN_N
CLK_OUT4
CLK_OUT4_CE
RESET
CLK_OUT4_CLR
POWER_DOWN
CLK_OUT5
CLK_OUT5_CE
CLK_OUT5_CLR
DADDR[6:0]
CLK_OUT6
DCLK
CLK_OUT6_CE
DEN
CLK_OUT6_CLR
DIN[15:0]
CLK_OUT7
DOUT[15:0]
CLK_OUT7_CE
DRDY
CLK_OUT7_CLR
DWE
INPUT_CLK_STOPPED
CLKFB_STOPPED
PSCLK
PSEN
LOCKED
PSINCDEC
PSDONE
IP Symbol
Resource Estimation
LogiCORE
Clocking Wizard
xilinx.com:ip:clk_wiz:3.6
PLLE2_ADV Settings
These are the settings based on your input. If you change them, you may lose the optimal settings found by the wizard, and selections made on previous pages will not apply.
Allow override mode (manual edits to PLLE2 attributes)
Attribute
Value
BANDWIDTH
OPTIMIZED
CLKFBOUT_MULT
48
CLKFBOUT_PHASE
0.000
CLKIN1_PERIOD
6.400
CLKIN2_PERIOD
10.000
COMPENSATION
ZHOLD
DIVCLK_DIVIDE
5
REF_JITTER1
0.010
REF_JITTER2
0.010
CLKOUT0_DIVIDE
10
CLKOUT0_DUTY_CYCLE
0.500
CLKOUT0_PHASE
0.000
Notes to be included in the comments of the generated component:
None
Datasheet
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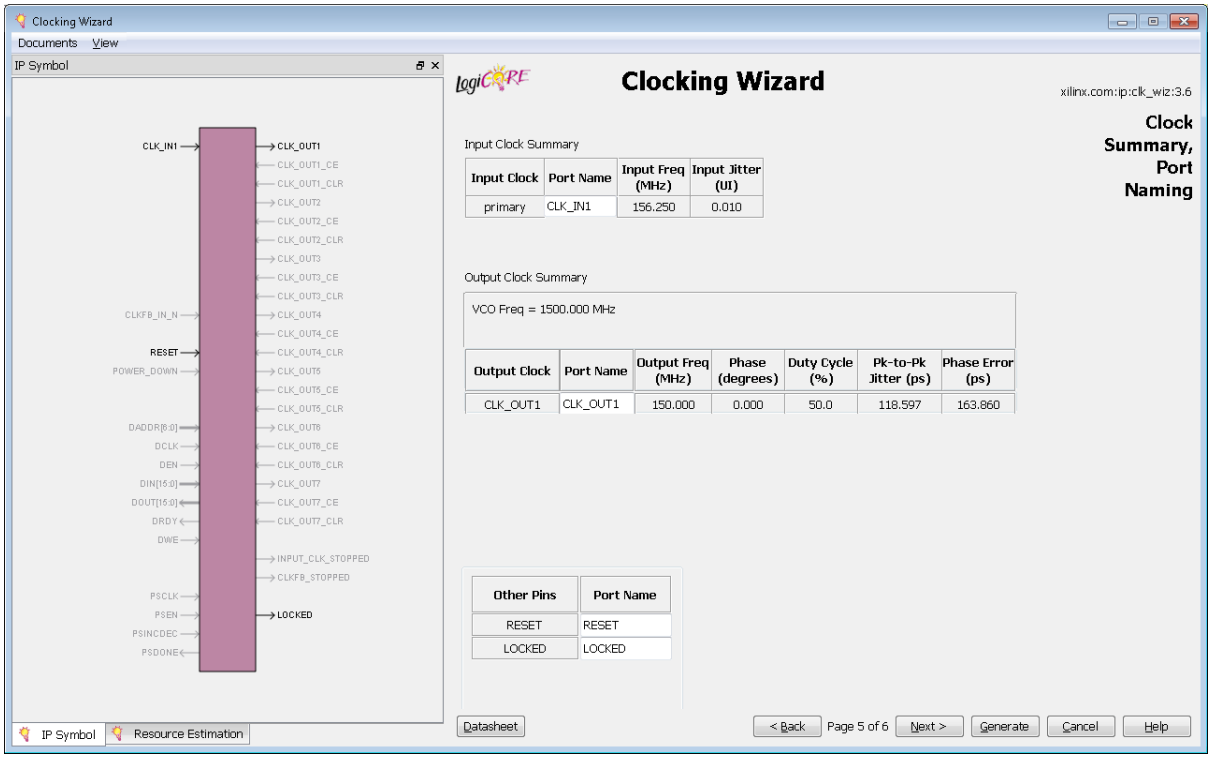
Step 5:


Clocking Wizard
Documents View
IP Symbol
Clocking Wizard
xilinx.com:ip:clk_wiz:3.6
Clock Summary, Port Naming
Input Clock Summary
Input Clock | Port Name | Input Freq (MHz) | Input Jitter (UI)
primary | CLK_IN1 | 156.250 | 0.010
Output Clock Summary
VCO Freq = 1500.000 MHz
Output Clock | Port Name | Output Freq (MHz) | Phase (degrees) | Duty Cycle (%) | Pk-to-Pk Jitter (ps) | Phase Error (ps)
CLK_OUT1 | CLK_OUT1 | 150.000 | 0.000 | 50.0 | 118.597 | 163.860
Other Pins | Port Name
RESET | RESET
LOCKED | LOCKED
Datasheet
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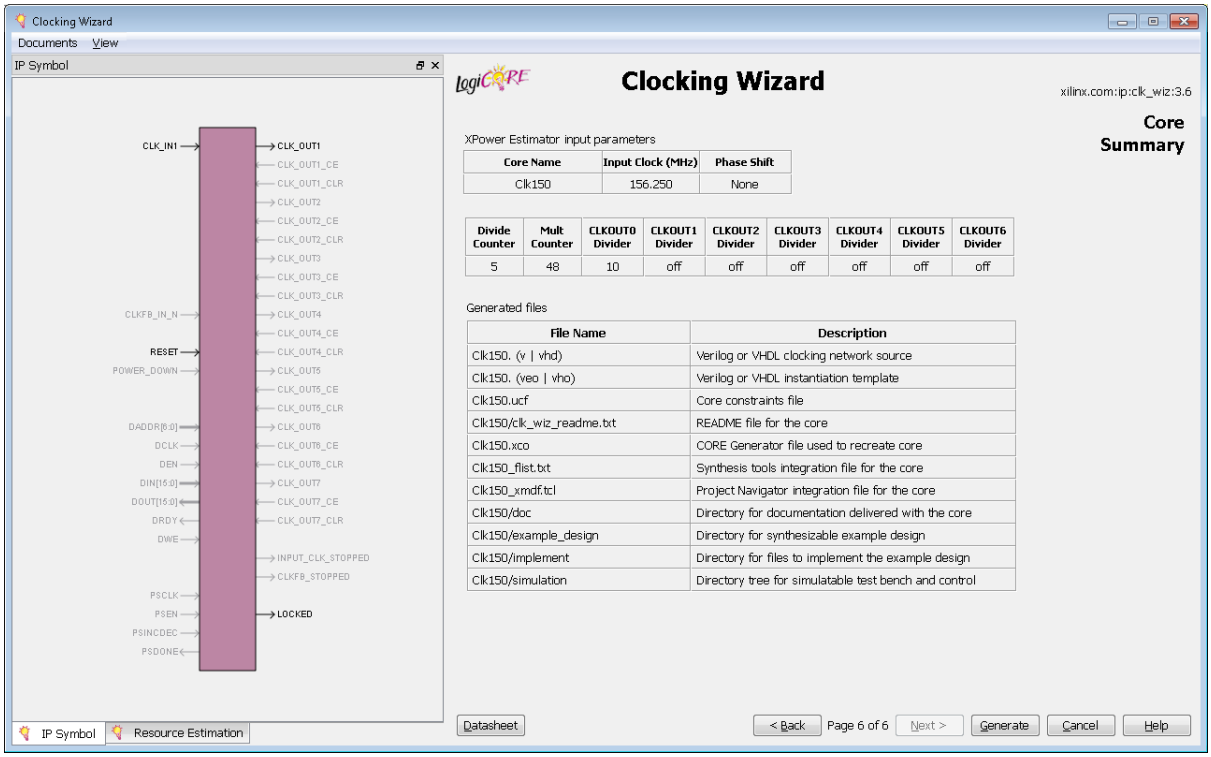
Help
IP Symbol
Resource Estimation

Step 6:


Clocking Wizard
Documents View
IP Symbol
Clocking Wizard
xilinx.com:ip:clk_wiz:3.6
Core Summary
XPower Estimator input parameters
Core Name | Input Clock (MHz) | Phase Shift
Clk150 | 156.250 | None
Divide Counter | Mult Counter | CLKOUT0 Divider | CLKOUT1 Divider | CLKOUT2 Divider | CLKOUT3 Divider | CLKOUT4 Divider | CLKOUT5 Divider | CLKOUT6 Divider
5 | 48 | 10 | off | off | off | off | off | off
Generated files
File Name | Description
Clk150. (v | vhd) | Verilog or VHDL clocking network source
Clk150. (veo | vho) | Verilog or VHDL instantiation template
Clk150.ucf | Core constraints file
Clk150/clk_wiz_readme.txt | README file for the core
Clk150.xco | CORE Generator file used to recreate core
Clk150_flist.txt | Synthesis tools integration file for the core
Clk150_xmdf.tcl | Project Navigator integration file for the core
Clk150/doc | Directory for documentation delivered with the core
Clk150/example_design | Directory for synthesizable example design
Clk150/implement | Directory for files to implement the example design
Clk150/simulation | Directory tree for simulatable test bench and control
Datasheet
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Resource Estimation