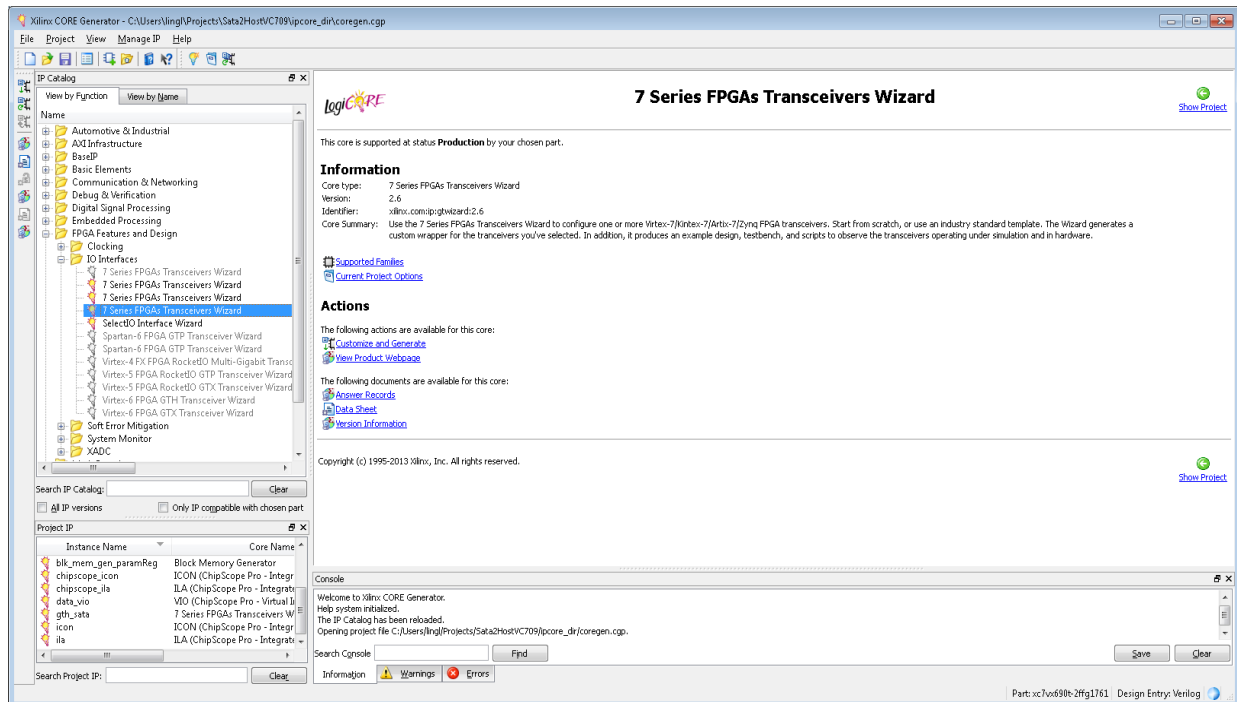


GTH instantiation process for SATA2 (3Gb/s)

Lisa Liu, Xilinx, 14.08.2013

Platform: VC709, FMC XM104, ISE14.6 (64 bit)

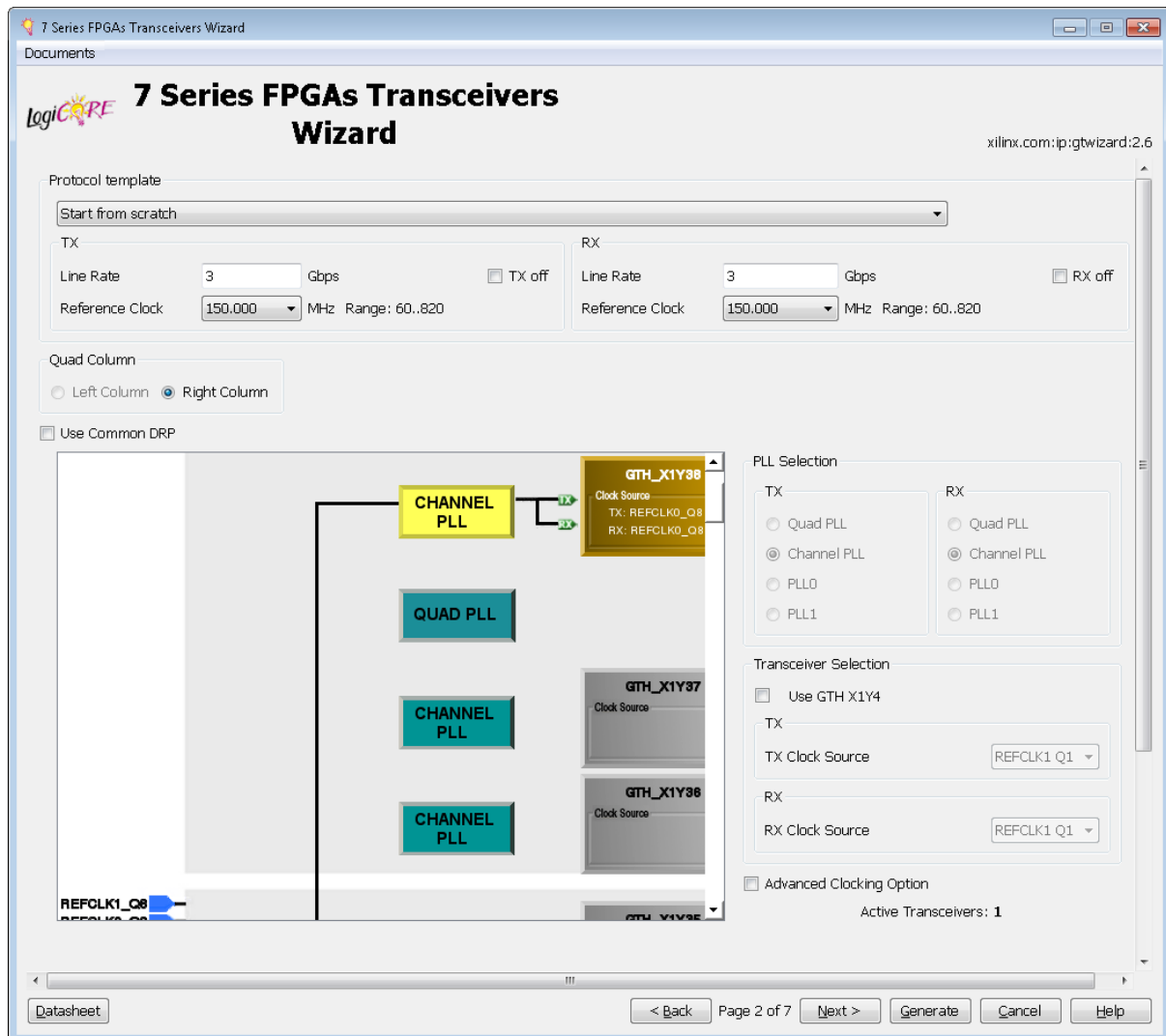
Step 1: Open core generator, select “7 Series FPGAs Transceiver Wizard” -> “Customize and Generate”



Step2: Give component name, gth_sata in my case and choose transceiver type.



Step3: Setup line rate, choose GTH tile and PLL, in this case “Channel PLL” is used.



To find out which GTH tile should be used, following steps are needed.

- For SATA1 port on XM104, on page 14 in ug536.pdf, table 1-5 gives the signal names of the corresponding sata pins.
- Track these signals names back to the schematic of the FPGA development board (VC709, in my case) and find out the FPGA pins that drive these signals (C2, C1, B8, B7 in my case).
- Find the GTH tile that drive these FPGA pins (in my case, on page 395 of UG476.pdf, it shows that these pins are driven by GTH_X1Y38).

Step 4: Setup 8B/10B encoding and decoding

7 Series FPGAs Transceivers Wizard

Documents

7 Series FPGAs Transceivers Wizard

xilinx.com:ip:gtwizard:2.6

TX

External Data Width: 16 Bits

Encoding: 8B/10B

Internal Data Width: 20 Bits

☒ Use DRP 60 MHz

Encoding Optional Ports

☐ TXBYPASS8B10B

☐ TXCHARDISPMODE

☐ TXCHARDISPPAL

☐ RXCHARISCOMMA

☒ RXCHARISK

☐ RXSTARTOFSEQ

Synchronization and Clocking

TX

☒ Enable TX Buffer

TXUSRCLK Source: TXOUTCLK

TXOUTCLK Source: ☐ Use TXPLLREFCLK

RX

☒ Enable RX Buffer

RX Buffer Bypass Mode: Auto

RXUSRCLK Source: TXOUTCLK

RXOUTCLK Source: ☐ Use RXPLLREFCLK

Optional Ports

☐ TXPCSRESET

☐ TXPMARESET

☐ TXSYSCLKSEL

☐ TXRATE

☐ TXBUFSTATUS

☐ RXPCSRESET

☐ RXPMARESET

☐ RXSYSCLKSEL

☐ RXRATE

☐ RXBUFSTATUS

☐ RXBUFRESET

☐ RXCDRHOLD

☐ CPLLDP

☐ QPLLDP

Used to dynamically change the RX rate

Datasheet

< Back Page 3 of 7 Next > Generate Cancel Help

Step 5: Alignment setting

7 Series FPGAs Transceivers Wizard

Documents

7 Series FPGAs Transceivers Wizard

xilinx.com:ip:gtwizard:2.6

RXCOMMA Alignment

RX COMMA detection

☒ Use comma detection

☐ Decode valid comma only

☐ Combine plus/minus commas (double-length comma)

Comma Value:

Plus Comma:

Minus Comma:

Comma Mask:

Align to:

Optional Ports

☐ ENPCOMMAALIGN (Enables positive Comma Alignment)

☐ ENMCOMMAALIGN (Enables negative Comma Alignment)

☐ RXSLIDE

☒ RXBYTEISALIGN

☐ RXBYTEREALIGN

☐ RXCOMMADET

Termination and Equalization

Differential Swing and Emphasis Mode:

RX Equalization

Equalization Mode:

Automatic Gain Control:

RX Termination

Termination Voltage:

☒ GND ☐ AVTT

☐ Floating ☐ Programmable

RX Termination Voltage: mV

Optional Ports

<input type="checkbox"/> TXPOLARITY	<input type="checkbox"/> TXQPISENN	<input type="checkbox"/> RXPOLARITY	<input type="checkbox"/> RXQPIEN
<input type="checkbox"/> TXINHIBIT	<input type="checkbox"/> TXQPISENP	<input type="checkbox"/> RXDFELPMRESET	<input type="checkbox"/> RXQPISENN
<input type="checkbox"/> TXDIFFCTRL	<input type="checkbox"/> TXQPIBIASEN	<input type="checkbox"/> RXDFEAGCOVRDEN	<input type="checkbox"/> RXQPISENP
<input type="checkbox"/> TXPOSTCURSOR	<input type="checkbox"/> TXQPIWEAKPUP	<input type="checkbox"/> RXLPMLFKLOVRDEN	<input type="checkbox"/> RXLPMEN
<input type="checkbox"/> TXPRECURSOR	<input type="checkbox"/> TXQPISTRONGPDOWN	<input type="checkbox"/> RXLPMHFOVRDEN	
<input type="checkbox"/> TXMAINCURSOR			

[Datasheet](#) [< Back](#) [Page 4 of 7](#) [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Step 6: OOB signalling

7 Series FPGAs Transceivers Wizard

Documents

7 Series FPGAs Transceivers Wizard

xilinx.com:ip:gtwizard:2.6

PCIe Express and SATA

☐ Enable PCI Express

SATA COM sequence

Bursts

Idles

PCI Express Parameters

Transition Time

To P2

From P2

To/From Non P2

Optional Ports

☐ LOOPBACK ☒ COMWAKEDET ☐ TXDETECTRX

☒ RXSTATUS ☒ TXCOMINIT ☒ TXELECIDLE

☐ RXVALID ☒ TXCOMSAS ☐ PHYSTATUS

☒ COMINITDET ☒ TXCOMWAKE ☐ TXPOWERDOWN

☒ COMSASDET ☒ COMFINISH ☐ RXPOWERDOWN

OOB signalling and PRBS

OOB Signal Detection

☒ Use RX OOB Signal Detection

PRBS

☐ Use PRBS Detector ☐ RXPRBS_LOOPBACK

☐ Use Port TXPRBSSEL

☐ Use Port TXPRBSFORCEERR

Channel Bonding

☐ Use Channel Bonding

☐ Use Two Channel Bonding Sequences

Sequence length

Sequence Max Skew

Clock correction

☐ Use Clock Correction

☐ Use Two Clock Correction Sequences

Sequence length

PPM Offset +/-

Periodicity of the CC sequence bytes

Datasheet

< Back Page 5 of 7 Next > Generate Cancel Help

Step 7: Channel bonding (use default)

7 Series FPGAs Transceivers Wizard

Documents

7 Series FPGAs Transceivers Wizard

xilinx.com:ip:gtwizard:2.6

Channel Bonding Sequence Definition

Sequence1, Byte1	Sequence1, Byte2	Sequence1, Byte3	Sequence1, Byte4
00000000	00000000	00000000	00000000
<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character
<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity
<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care

Sequence2, Byte1	Sequence2, Byte2	Sequence2, Byte3	Sequence2, Byte4
00000000	00000000	00000000	00000000
<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character
<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity
<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care

Clock Correction Sequence Definition

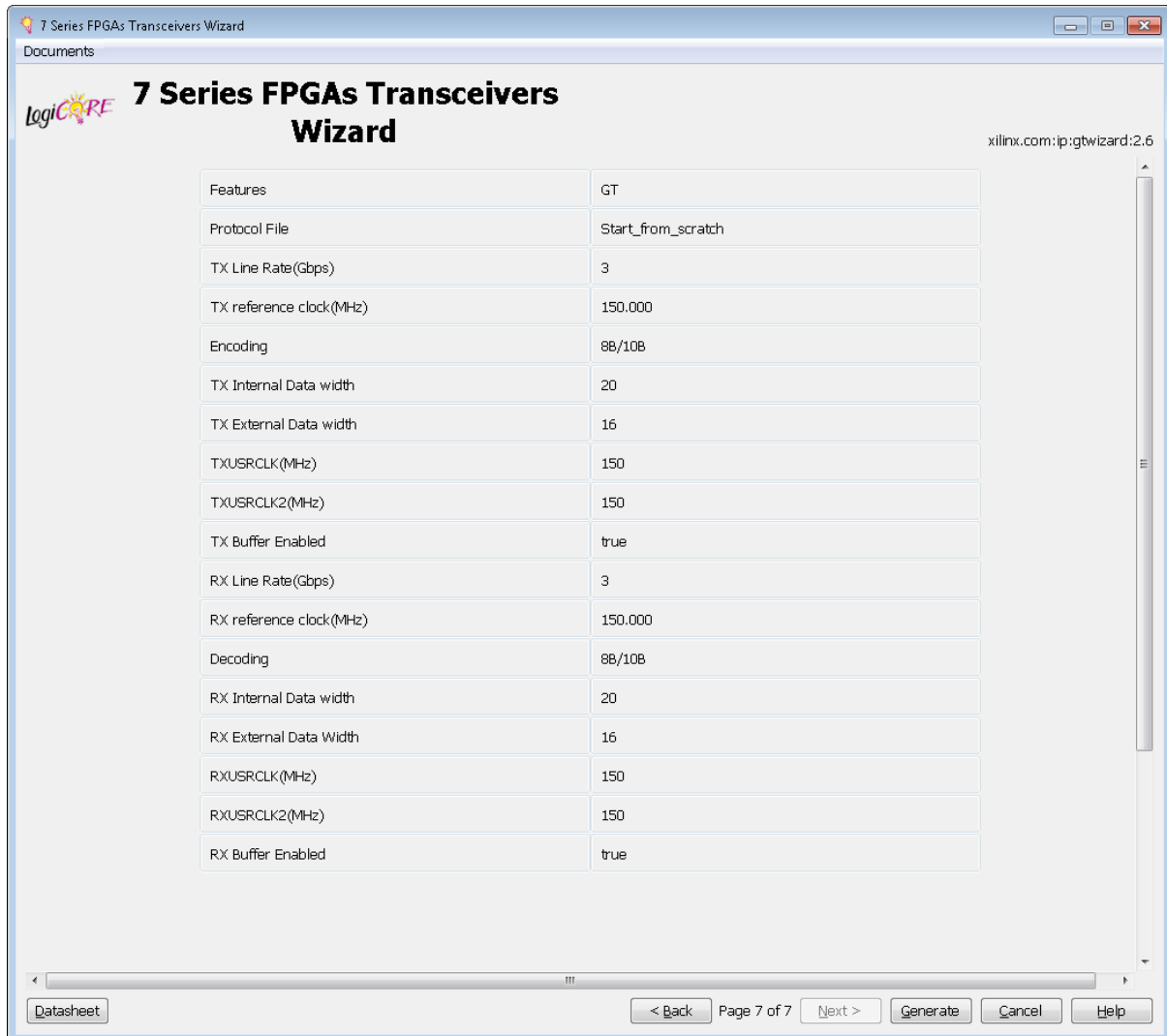
Sequence1, Byte1	Sequence1, Byte2	Sequence1, Byte3	Sequence1, Byte4
00000000	00000000	00000000	00000000
<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character
<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity
<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care

Sequence2, Byte1	Sequence2, Byte2	Sequence2, Byte3	Sequence2, Byte4
00000000	00000000	00000000	00000000
<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character	<input type="checkbox"/> K Character
<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity	<input type="checkbox"/> Inverted Disparity
<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care	<input type="checkbox"/> Don't Care

Datasheet

< Back Page 6 of 7 Next > Generate Cancel Help

Step 8: Summary



The screenshot shows the '7 Series FPGAs Transceivers Wizard' window. The title bar indicates 'Documents' and '7 Series FPGAs Transceivers Wizard'. The window contains a table with configuration parameters and their values. The parameters are organized into TX and RX sections. The TX section includes settings for Line Rate, reference clock, encoding, data width, and buffer enablement. The RX section includes similar settings for the receiver. The bottom of the window features a 'Datasheet' button and navigation controls: '< Back', 'Page 7 of 7', 'Next >', 'Generate', 'Cancel', and 'Help'.

Features	GT
Protocol File	Start_from_scratch
TX Line Rate(Gbps)	3
TX reference clock(MHz)	150.000
Encoding	8B/10B
TX Internal Data width	20
TX External Data width	16
TXUSRCLK(MHz)	150
TXUSRCLK2(MHz)	150
TX Buffer Enabled	true
RX Line Rate(Gbps)	3
RX reference clock(MHz)	150.000
Decoding	8B/10B
RX Internal Data width	20
RX External Data Width	16
RXUSRCLK(MHz)	150
RXUSRCLK2(MHz)	150
RX Buffer Enabled	true

When the core generator finish, add following files to the project (for the GTH instantiation process.

It might be different files for GTX):

- a) ipcore_dir\gth_sata\example_design\gth_sata_gt_usrclk_source.v
- b) ipcore_dir\gth_sata.v
- c) ipcore_dir\gth_sata_gt.v
- d) ipcore_dir\gth_sata\example_design\gth_sata_gtrxreset_seq.v
- e) ipcore_dir\gth_sata\example_design\gth_sata_sync_block.v

In above files, the gth_sata_gt_usrclk_source module takes the 150MHz reference clock inputs and generates input clocks, including DRP clock, for the GTH transceiver, which is defined in gth_sata module.

The gth_sata.v is the top module for GTH transceiver instantiation. It contains the GTH instance specified in gth_sata_gt module and the reset circuitry for GTH implemented in gth_sata_gtrxreset_seq and gth_sata_sync_block module.

Note: the DRP clock is also important. Because it is used to drive the GTH reset circuit. The DRP clock in my case is 60MHz generated from 200MHz system clock.

I have changed following attribute values of GTH instance.

.RX_CM_SEL (2'b11), //(2'b01), original value 01. This is used to choose 800mV termination voltage for RX.

.PCS_RSVD_ATTR (48'h000000000100), //original value was 0. This is used to enable OOB detection circuit in GTH.