GTH instantiation process for SATA2 (3Gb/s)

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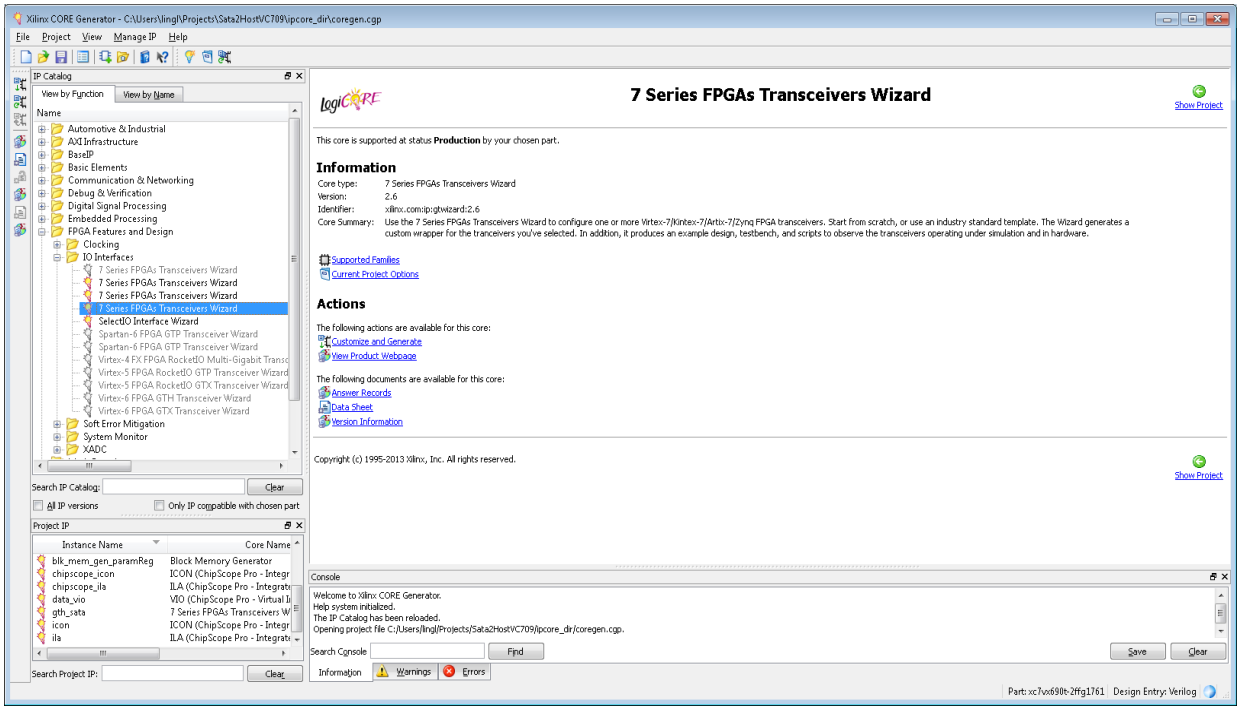
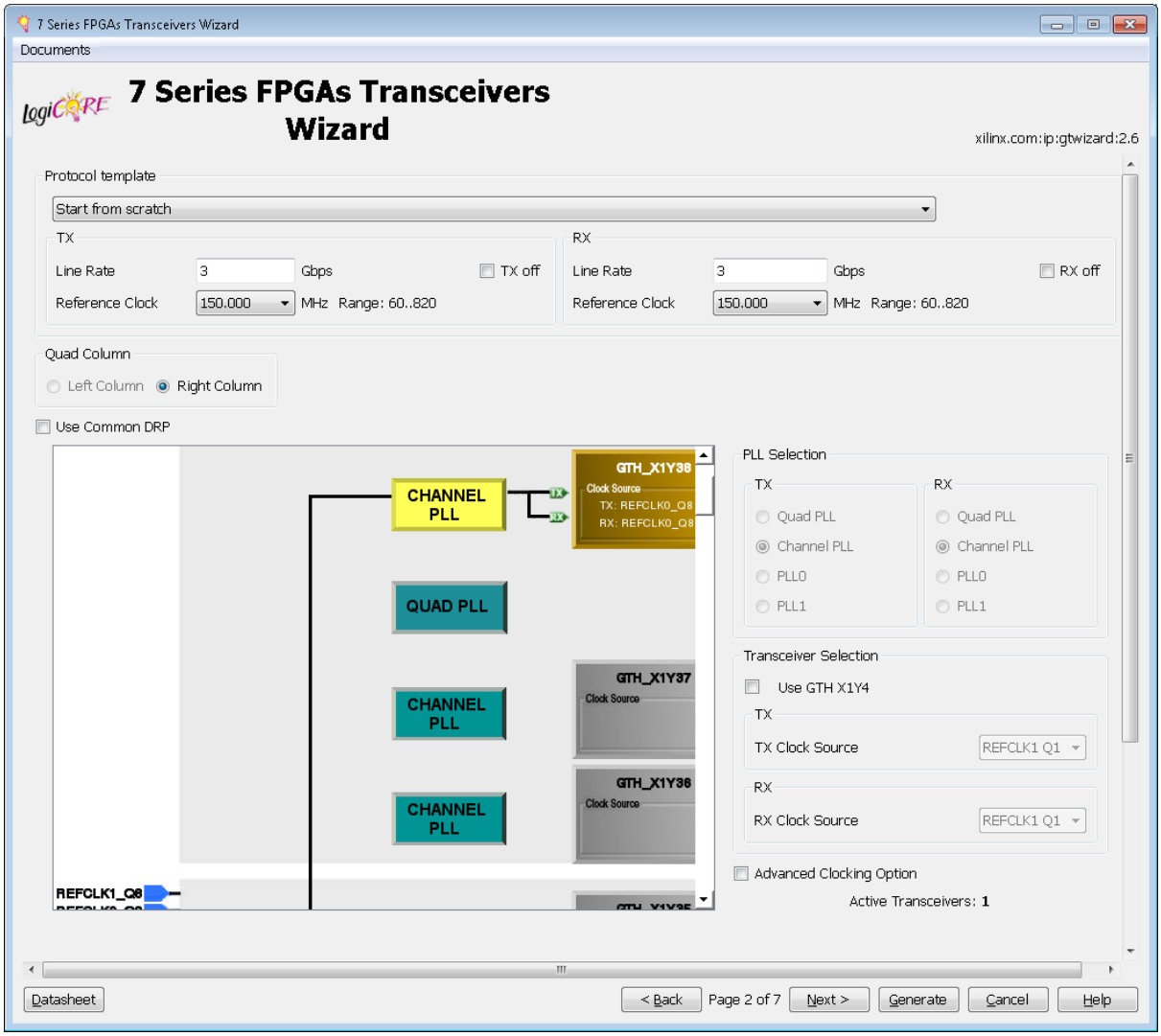
Platform: VC709, FMC XM104, ISE14.6 (64 bit)

Step 1: Open core generator, select “7 Series FPGAs Transceiver Wizard” -> “Customize and Generate”



Step2: Give component name, gth_sata in my case and choose transceiver type.

Step3: Setup line rate, choose GTH tile and PLL, in this case “Channel PLL” is used.



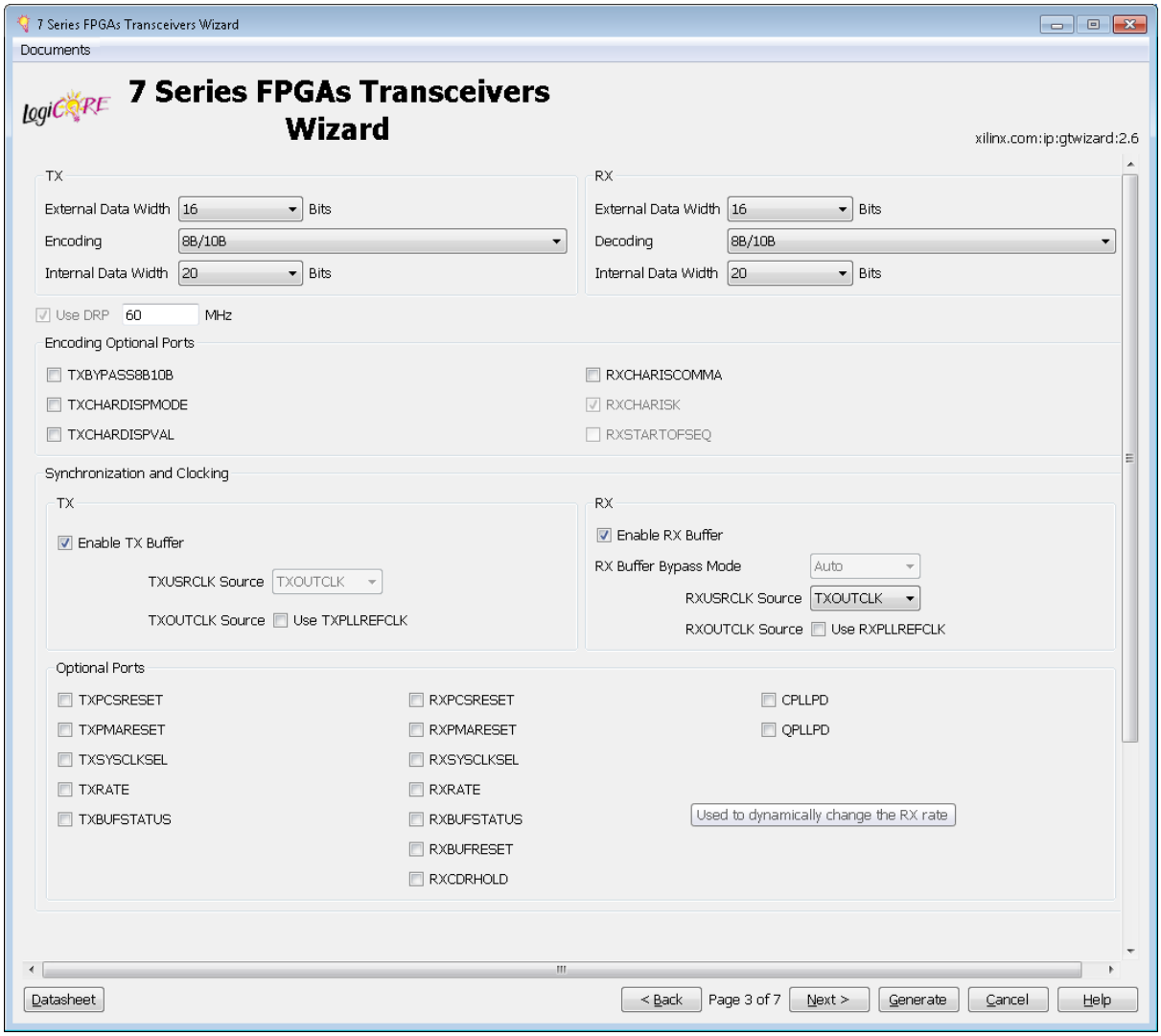
To find out which GTH tile should be used, following steps are needed.

a) For SATA1 port on XM104, on page 14 in ug536.pdf, table 1-5 gives the signal names of the corresponding sata pins.

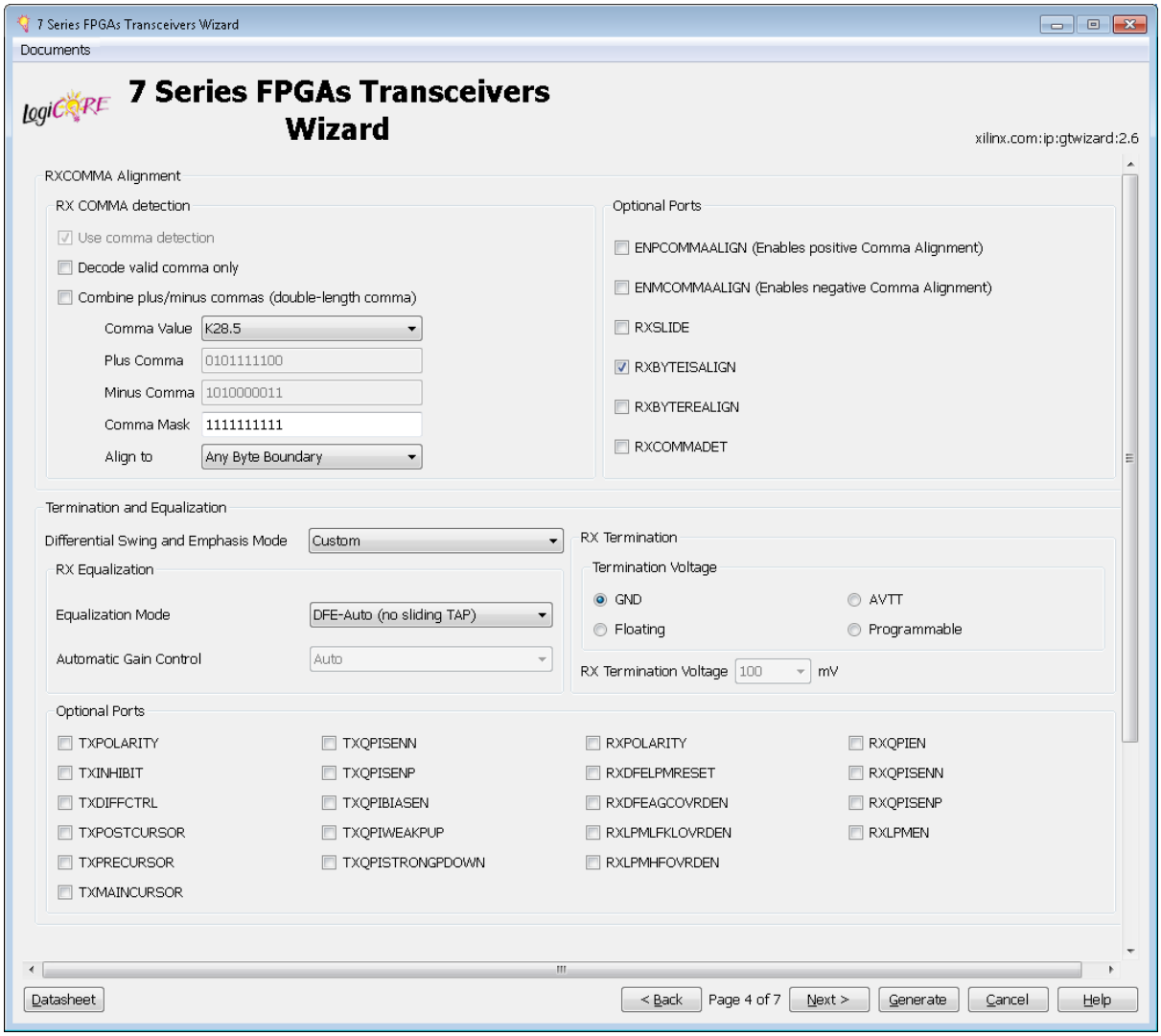
b) Track these signals names back to the schematic of the FPGA development board (VC709, in my case) and find out the FPGA pins that drive these signals (C2, C1, B8, B7 in my case).

c) Find the GTH tile that drive these FPGA pins (in my case, on page 395 of UG476.pdf, it shows that these pins are driven by GTH_X1Y38).

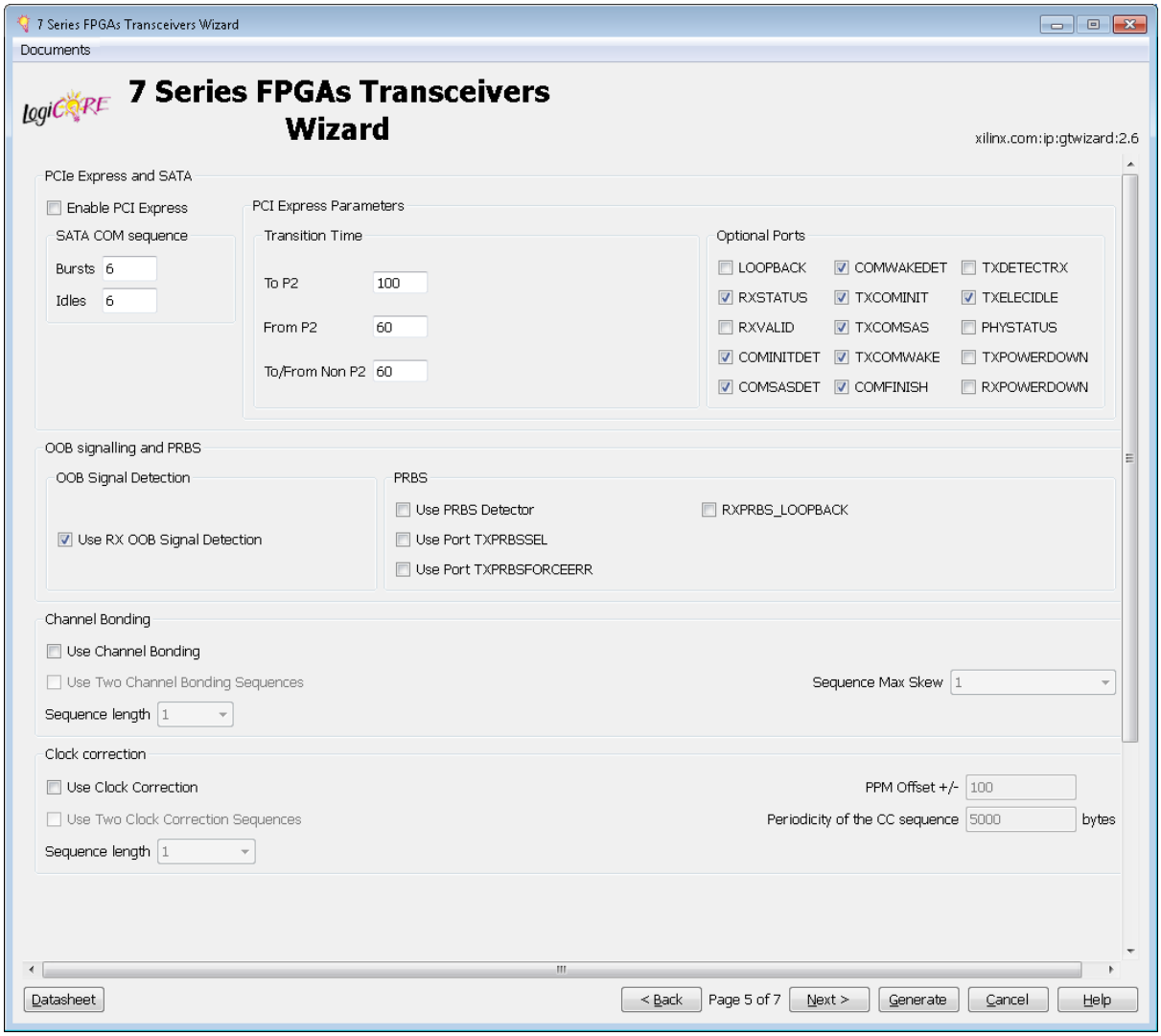
Step 4: Setup 8B/10B encoding and decoding



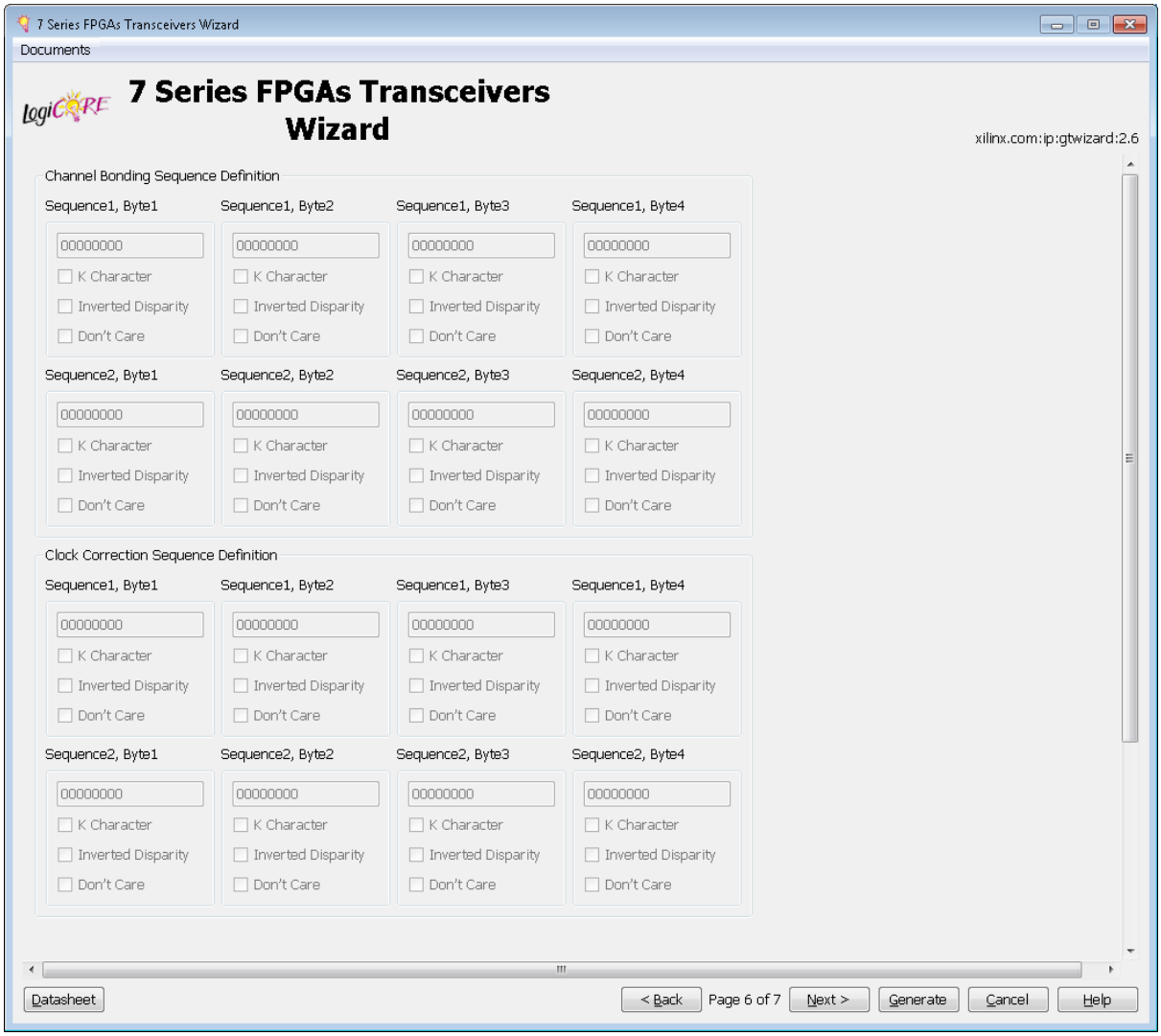
Step 5: Alignment setting



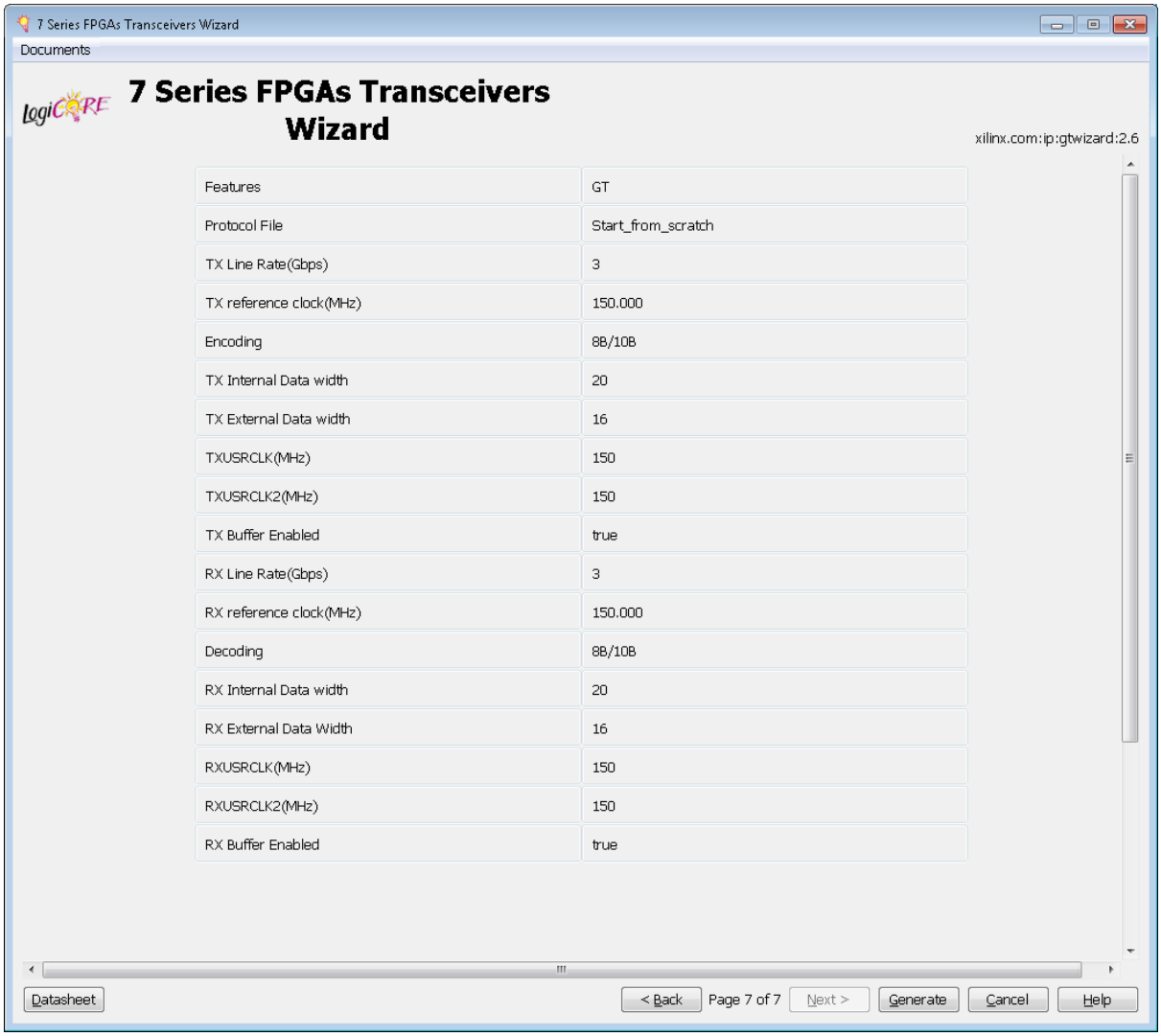
Step 6: OOB signalling



Step 7: Channel bonding (use default)



Step 8: Summary



When the core generator finish, add following files to the project (for the GTH instantiation process. It might be different files for GTX):

a) ipcore_dir\gth_sata\example_design\gth_sata_gt_usrclk_source.v

b) ipcore_dir\gth_sata.v

c) ipcore_dir\gth_sata_gt.v

d) ipcore_dir\gth_sata\example_design\gth_sata_gtrxreset_seq.v

e) ipcore_dir\gth_sata\example_design\gth_sata_sync_block.v

In above files, the gth_sata_gt_usrclk_source module takes the 150MHz reference clock inputs and generates input clocks, including DRP clock, for the GTH transceiver, which is defined in gth_sata module.

The gth_sata.v is the top module for GTH transceiver instantiation. It contains the GTH instance specified in gth_sata_gt module and the reset circuitry for GTH implemented in gth_sata_gtrxreset_seq and gth_sata_sync_block module.

Note: the DRP clock is also important. Because it is used to drive the GTH reset circuit. The DRP clock in my case is 60MHz generated from 200MHz system clock.

I have changed following attribute values of GTH instance.

.RX_CM_SEL (2'b11), //(2'b01), original value 01. This is used to choose 800mV termination voltage for RX.

.PCS_RSVD_ATTR (48'h000000000100), //original value was 0. This is used to enable OOB detection circuit in GTH.