## ODE Solver Design Report

Mahmoud Adas Evram Youssef

Section:2, BN:21 Section:1, BN:9

Remonda Talaat Mohamed Shawky
Section:1, BN:20 Section:2, BN:16

March 20, 2020

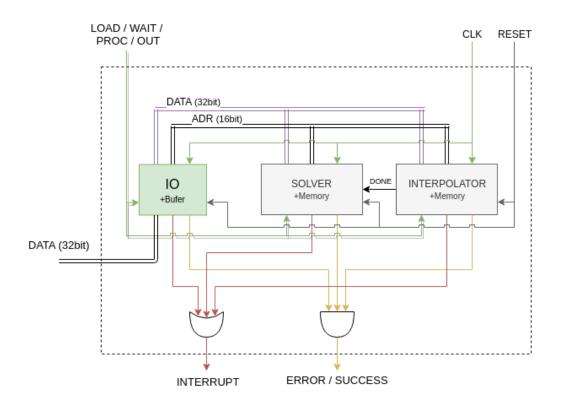


Figure 1: Overall Design

## 1 Interfaces and HW Summary

The hardware has the following interfaces that triggers some actions summarized below and detailed in the rest of the document.

- CLK: IN
- RESET: ASYNC IN
  - clears all internal states of all modules:
    - \* IO internal buffer.
    - \* ERROR/SUCCESS of all modules resets to SUCCESS.
    - \* INTERRUPT resets to zero.
  - Memory at solver and interpolator are NOT cleared.
  - at next clock, CPU is expected to turn the LOAD / WAIT / PROC / OUT into LOAD state and we will start loading input again.
- LOAD / WAIT / PROC / OUT (2bit): IN:
  - set the current major state of the machine
  - LOAD(0):
    - \* IO receives **compressed** data from the CPU.
    - \* IO decompresses data into buffer.
    - \* buffer is flushed into data bus with appropriate address.
    - \* ends when cpu finishes its data loading and switches to WAIT state.
  - WAIT(1):
    - \* Same state as LOAD, but IO doesn't receive anymore data from CPU.
    - \* ends when IO flushes all its buffer and raises *INTERRUP* with either *ERROR* or *SUCCESS*.
  - PROC(2):
    - \* SOLVER sends time step to calculate U at.
    - \* SOLVER and INTERPOLATOR work concurrently to calculate their outputs.

- \* INTERPOLATOR sends DONE signal to SOLVER when it finishes the interpolated U.
- \* SOLVER can request to copy the interpolated U.
- \* INTERPOLATOR waits for SOLVER to send next time step.
- \* ends when either SOLVER or INTERP raises INTERRUPT with either SUCCESS or ERROR.

## - OUT(3):

- \* IO just copies final outputs to cpu from SOLVER memory.
- \* ends when IO raises INTERRUPT with either SUCCESS or ERROR.
- DATA (32bit): INOUT
  - Data bus between cpu and io.
- INTERRUPT: OUT
  - raised from 0 to 1 when some internal module (IO / SOLVER / INTERPOLATOR) finishes its task.
  - if task finished with success the ERROR / SUCCESS is set to SUCCESS, otherwise it's ERROR.
- ERROR(0) / SUCCESS(1): OUT
  - CPU should operate on this value ONLY when INTERRUPT is
     1.
  - errors that could happen include: divide by zero, H \(\begin{aligned} 1\), incomplete input.