5-stage Pipelined Processor Design Report

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Part I

Introduction

0.1 System Overview

This document reports our design work of the 5-stage pipelined processor using Harvard architecture. We discuss the overall system blocks and connections, the functionalities of the different blocks and the hazard solutions.

0.2 Task Distribution

TODO: Task distribution table

Part II

Overall System

0.3 Overall System Design Schema

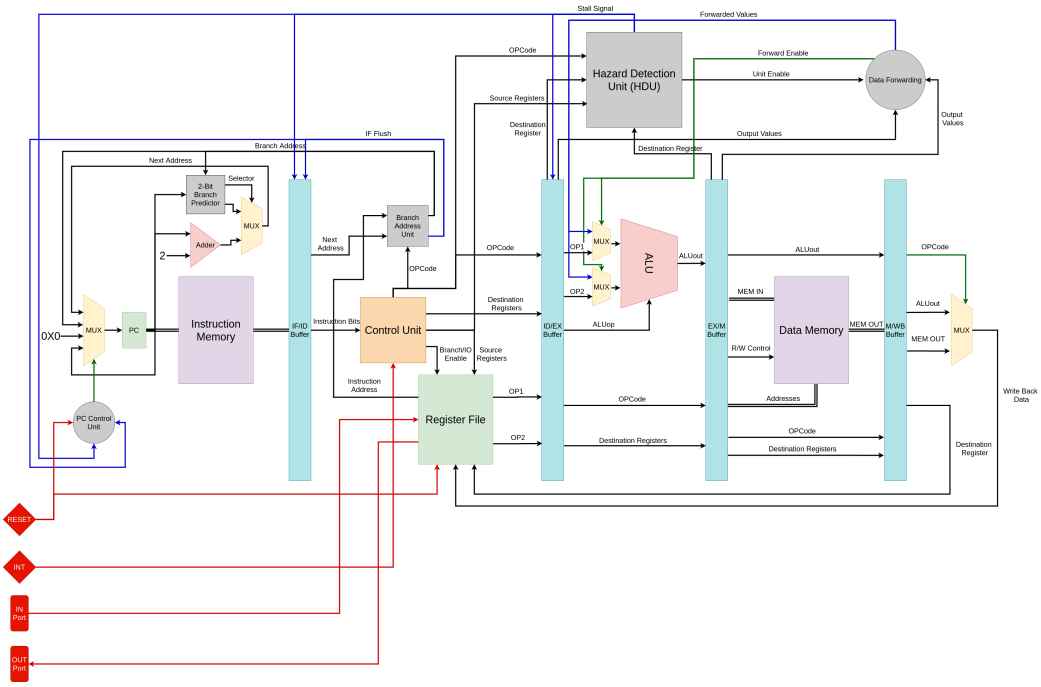

Figure 1: Overall System Design

0.4 Memory Specs

The following are the initial specs for both instruction and data memory.

0.4.1 Instruction Memory

- $4GB\ X\ 16BIT$
- BUS $= 16BIT$

0.4.2 Data Memory

- $4GB\ X\ 16BIT$

- BUS = $16BIT$
- SP $->$ 2^{31} *(at the middle of the memory).*

Part III

Instruction Format

0.5 One Operand Operations

- 4 bits (1111) for one operand instructions.
- 3 bits to define instruction.
- 3 bits for destination register.
- 1 bit to define the memory slots occupied by the instruction.
- Total of 11 bits, padded with 5 0's to fit 16 bits.

Table 1: One Operand Instruction Mapping

Operation	OpCode	Destination	16|32	Conditions
IN	1111000	000:111	0	————————
NOT	1111001	000:111	0	if !Rdst=0,Z=1 if !Rdst<0,N=1
INC	1111010	000:111	0	if Rdst+1=0,Z=1 if Rdst+1<0,N=1
DEC	1111011	000:111	0	if Rdst-1=0,Z=1 if Rdst-1<0,N=1
OUT	1111100	000:111	0	————————

0.6 Special Operations

- 16 0's to represent NOP (0000000000000000).

0.7 Two Operand Operations

- 4 bits to define instruction.
- 3 bits for each of Rsrc1, Rsrc2 and Rdst.
- 1 bit to define the memory slots occupied by the instruction.
- 16 bits for immediate values.
- Total of 14 bits in most cases with some exceptions mentioned below.

Table 2: Two Operand Instruction Mapping

Operation	OpCode	Rsrc1	Rsrc2	Rdst	imm	16|32	Conditions
SWAP	0001	000:111	—	000:111	—	0	———————— _
ADD	0010	000:111	000:111	000:111	—	0	if Result=0,Z=1 if Result<0,N=1
SUB	0011	000:111	000:111	000:111	—	0	if Result=0,Z=1 if Result<0,N=1
AND	0100	000:111	000:111	000:111	—	0	if Result=0,Z=1 if Result<0,N=1
OR	0101	000:111	000:111	000:111	—	0	if Result=0,Z=1 if Result<0,N=1
SHL	0110	000:111	—	—	16 bits	1	update carry flag
SHR	0111	000:111	—	—	16 bits	1	update carry flag
IADD	1000	000:111	—	000:111	16 bits	1	if Result=0,Z=1 if Result<0,N=1

0.8 Memory Operations

- 4 bits to define instruction.
- 3 bits for destination register.
- 1 bit to define the memory slots occupied by the instruction.
- 16 bits for immediate values.
- 20 bits for effective addresses.
- Total of 8 bits with no immediate values or effective addresses.
- Total of 24 bits with immediate values.
- Total of 28 bits with effective addresses.

Table 3: Memory Instruction Mapping

Operation	OpCode	Rdst	imm	EA	16|32	Conditions
PUSH	1001	000:111	—	—	0	————————
POP	1010	000:111	—	—	0	————————
LDM	1011	000:111	16 bits	—	1	————————
LDD	1100	000:111	—	20 bits	1	————————
STD	1101	000:111	—	20 bits	1	————————

0.9 Branch and Change Control Operations

- 4 bits (0000) for branching instructions.
- 3 bits to define instruction.
- 3 bits for destination register.
- 1 bit to define the memory slots occupied by the instruction.
- Total of 11 bits, padded with 5 0's to fit 16 bits.

Table 4: One Operand Instruction Mapping

Operation	OpCode	Destination	16|32	Conditions
JZ	0000001	000:111	0	————————
JMP	0000010	000:111	0	————————
CALL	0000011	000:111	0	————————
RET	0000100	—	0	————————
RTI	0000101	—	0	————————

Part IV

Control Unit

Part V

Pipeline Stages

Part VI

Pipeline Hazards and solutions

0.10 Hazards Detection

0.10.1 Structural Hazards

No detection required.

0.10.2 Data Hazards

Refer the *HDU* in 1

0.10.3 Control Hazards

- At Fetch stage, always check the branch predictor and calculate the next address accordingly.
- At Decode stage, check whether the OPCode is of a branch operation. If so, pass the address to the program counter and compare the correct address with the address of the counter to decide whether to flush the Fetch stage or not.

0.11 Hazards Handling

0.11.1 Structural Hazards

2 memory units, one for instructions and one for data. Both have the same specs *(mentioned below)*.
Also, to handle register file structural hazard, the write back will be in the first half of the clock cycle and the decode will be in the second half.

0.11.2 Data Hazards

Stall

Occurs only at Decode stage, due to load use case.

- Fetch same instruction (don't increment the program counter).
- Latch IF/ID buffer with the same values.
- Freeze Decode stage.

- Clear ID/EX buffer.

Data Forwarding

- EX/MEM buffer $->$ Execute / Decode.
- ID/EX buffer $->$ Decode.

0.11.3 Control Hazards

Flush

Occurs only at Fetch Stage, due to wrong branch prediction at Decode stage.

- Load new address in the program counter.
- Remove fetched instructions from IF/ID buffer.

Dynamic Branch Prediction

Hash table of some length containing Keys of branch addresses paired with 1-bit for branch prediction.