5-stage Pipelined Processor Design Report

Team #4

Mohamed Shawky
SEC:2, BN:16

Remonda Talaat
SEC:1, BN:20

Evram Youssef
SEC:1, BN:9

Mahmoud Adas
SEC:2, BN:21

March 29, 2020

Contents

List of Figures

List of Tables

Part I

Introduction

Part II

Overall System

0.1 Overall Design Schema

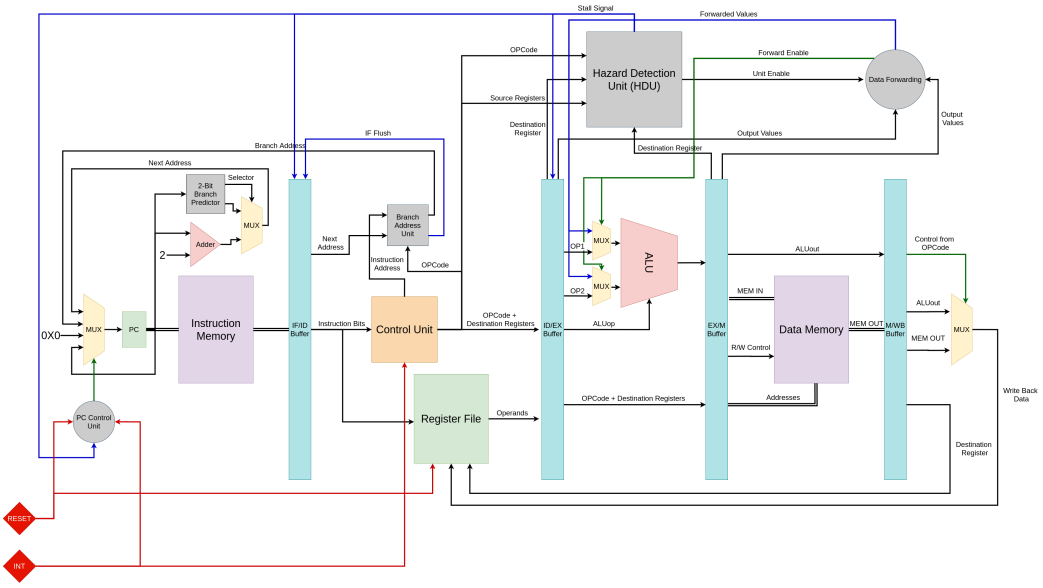

Figure 1: Overall System Design

0.2 Hazards Detection

0.2.1 Structural Hazards

No detection required.

0.2.2 Data Hazards

Refer the *HDU* in 1

0.2.3 Control Hazards

- At Fetch stage, always check the branch predictor and calculate the next address accordingly.

- At Decode stage, check whether the OPCode is of a branch operation. If so, pass the address to the program counter and compare the correct address with the address of the counter to decide whether to flush the Fetch stage or not.

0.3 Hazards Handling

0.3.1 Structural Hazards

2 memory units, one for instructions and one for data. Both have the same specs *(mentioned below)*.
Also, to handle register file structural hazard, the write back will be in the first half of the clock cycle and the decode will be in the second half.

0.3.2 Data Hazards

Stall

Occurs only at Decode stage, due to load use case.

- Fetch same instruction (don't increment the program counter).
- Latch IF/ID buffer with the same values.
- Freeze Decode stage.
- Clear ID/EX buffer.

Data Forwarding

- EX/MEM buffer $->$ Execute / Decode.
- ID/EX buffer $->$ Decode.

0.3.3 Control Hazards

Flush

Occurs only at Fetch Stage, due to wrong branch prediction at Decode stage.

- Load new address in the program counter.

- Remove fetched instructions from IF/ID buffer.

Dynamic Branch Prediction

Hash table of some length containing Keys of branch addresses paired with 2-bit FSM for branch prediction.

0.4 Memory Specs

The following are the initial specs for both instruction and data memory.

0.4.1 Instruction Memory

- $4GB\ X\ 16BIT$
- BUS = $16BIT$

0.4.2 Data Memory

- $4GB\ X\ 16BIT$
- BUS = $16BIT$
- SP $->$ 2^{31} *(at the middle of the memory).*

Part III

Instruction Format

Part IV

Control Unit

Part V

Pipeline Stages

Part VI

Pipeline Hazards and solutions