5-stage Pipelined Processor Design Report

Team #4

Mohamed Shawky
SEC:2, BN:16

Remonda Talaat
SEC:1, BN:20

Evram Youssef
SEC:1, BN:9

Mahmoud Adas
SEC:2, BN:21

March 28, 2020

Contents

List of Figures

List of Tables

Part I

Introduction

Part II

Overall System

0.1 Overall Design Diagram

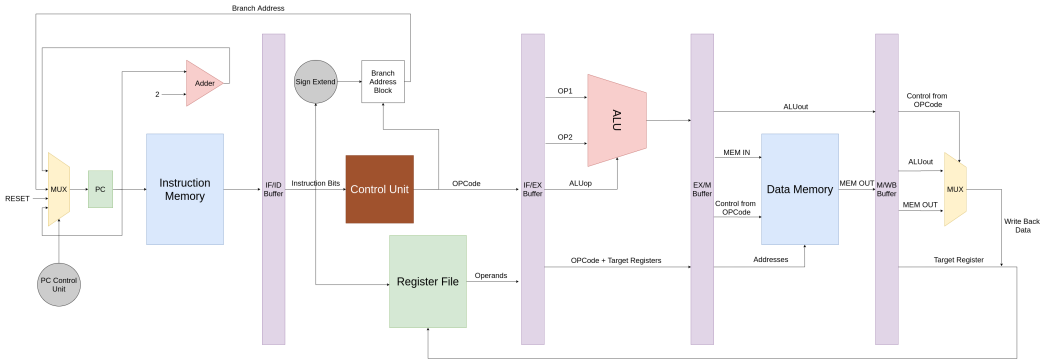

Figure 1: Overall System Design

0.2 Hazards Handling

0.2.1 Structural Hazards

2 memory units, one for instructions and one for data. Both have the same specs *(mentioned below)*.

0.2.2 Data Hazards

Stall

Occurs only at Decode stage, due to load use case.

- Fetch same instruction (don't increment the program counter).
- Latch IF/ID buffer with the same values.
- Freeze Decode stage.
- Clear ID/EX buffer.

Data Forwarding

- MEM/WB buffer $->$ Execute / Decode.
- EX/MEM buffer $->$ Execute / Decode.

0.2.3 Control Hazards

Flush

Occurs only at Fetch Stage, due to wrong branch prediction at Decode stage.

- Load new address in the program counter.
- Remove fetched instructions from IF/ID buffer.

Dynamic Branch Prediction

Hash table of some length containing Keys of branch addresses paired with 2-bit FSM for branch prediction.

0.3 Memory Specs

The following are the initial specs for both instruction and data memory.

0.3.1 Instruction Memory

- $4GB\ X\ 16BIT$
- BUS = $16BIT$

0.3.2 Data Memory

- $4GB\ X\ 16BIT$
- BUS = $16BIT$
- SP $->$ 2^{31} *(at the middle of the memory).*

Part III

Instruction Format

Part IV

Control Unit

Part V

Pipeline Stages

Part VI

Pipeline Hazards and solutions