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UVVM Tutorial

A brief introduction to UVVM.

UVVM Library

- Overview

bitvis
A COMPANY IN THE ACANDO GROUP

UVVM

- Universal VHDL Verification Methodology
- VHDL only
- Open Source

Utility Library

- logging
- alert handling
- result checking
- sufficient for simple testbenches

VVC Framework

- advanced features
- better overview
- readability and maintainability
- support for CRV and coverage

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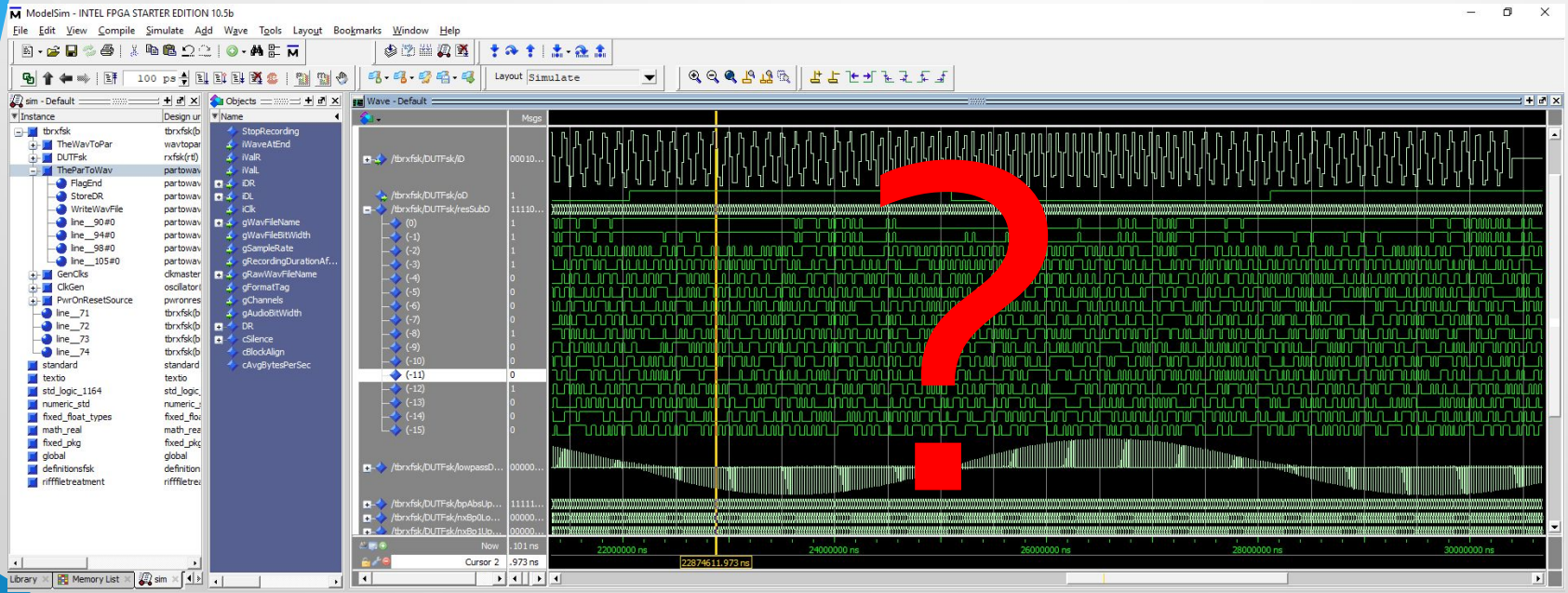
UVVM Library

- Motivation



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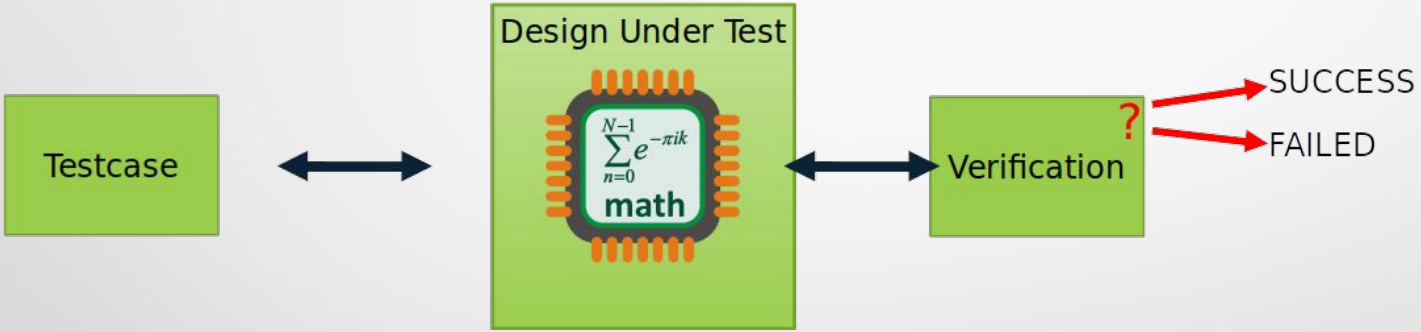
- Motivation



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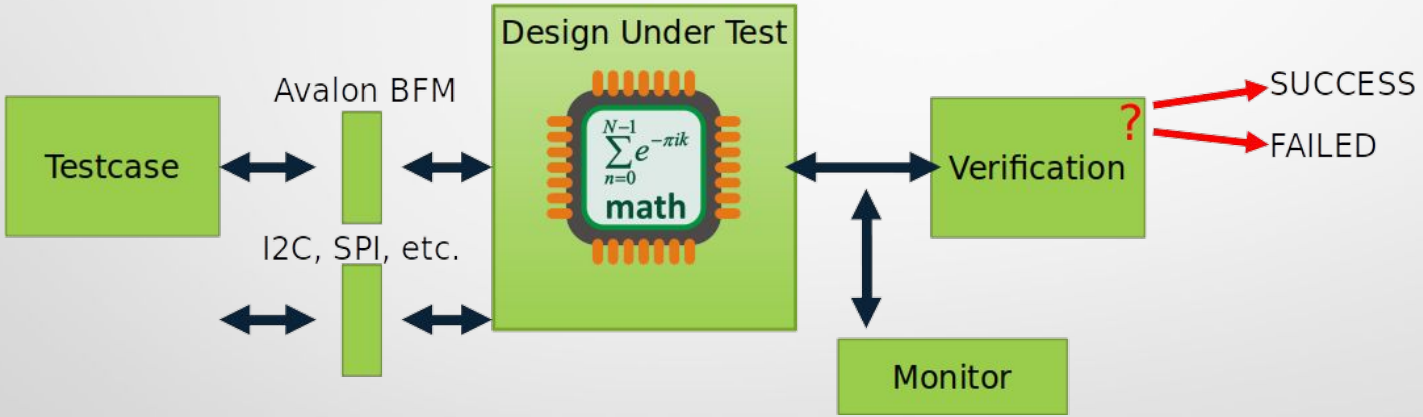
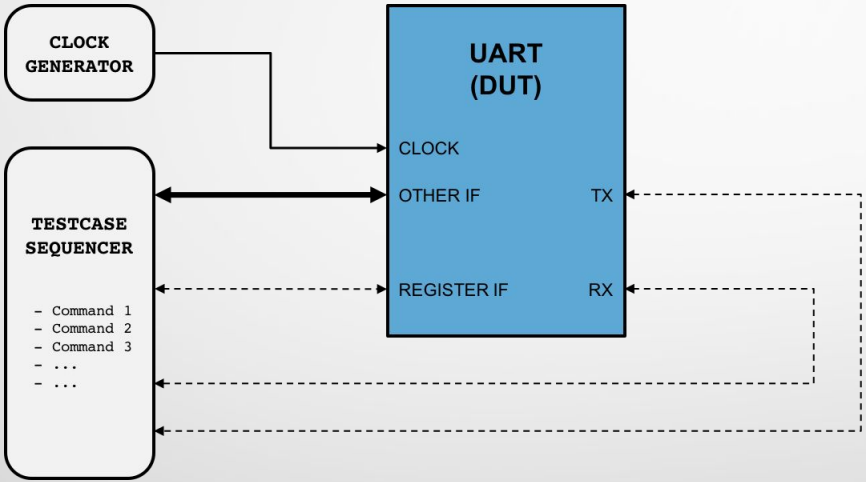


UVVM Library

- The UVVM way



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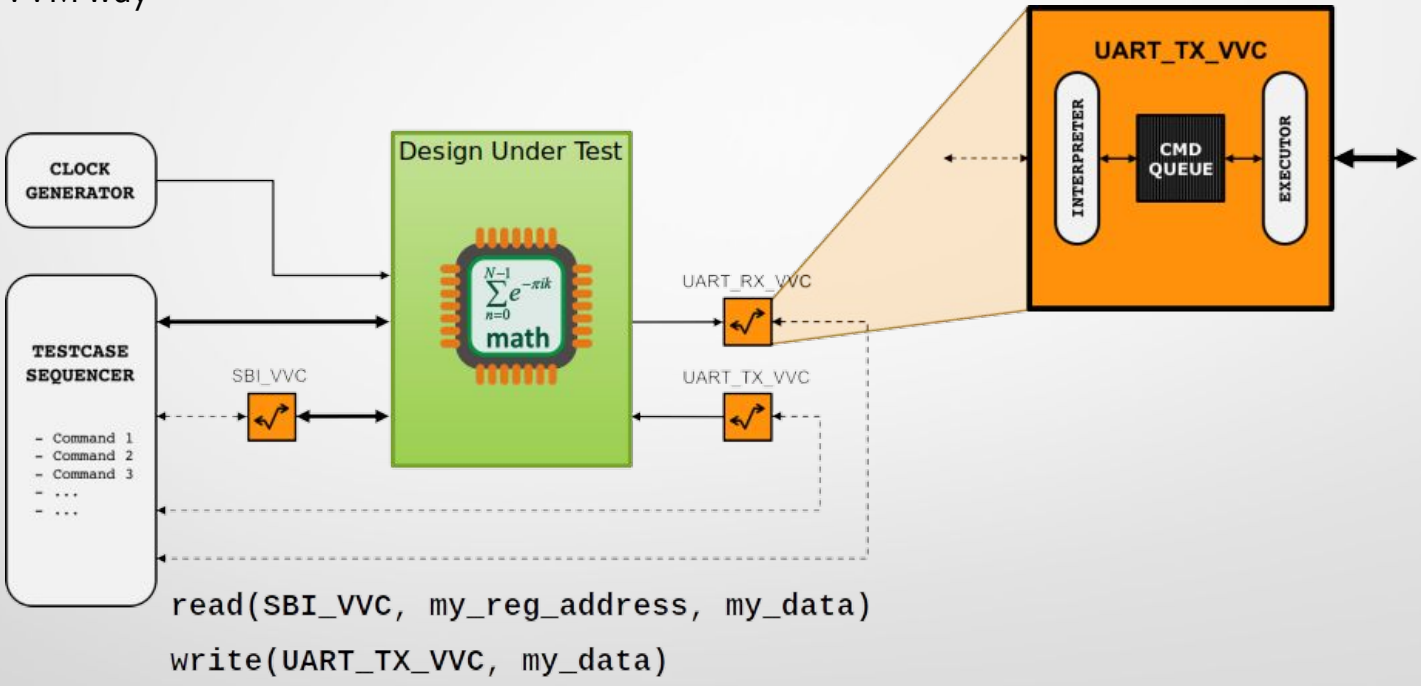
- The UVVM way



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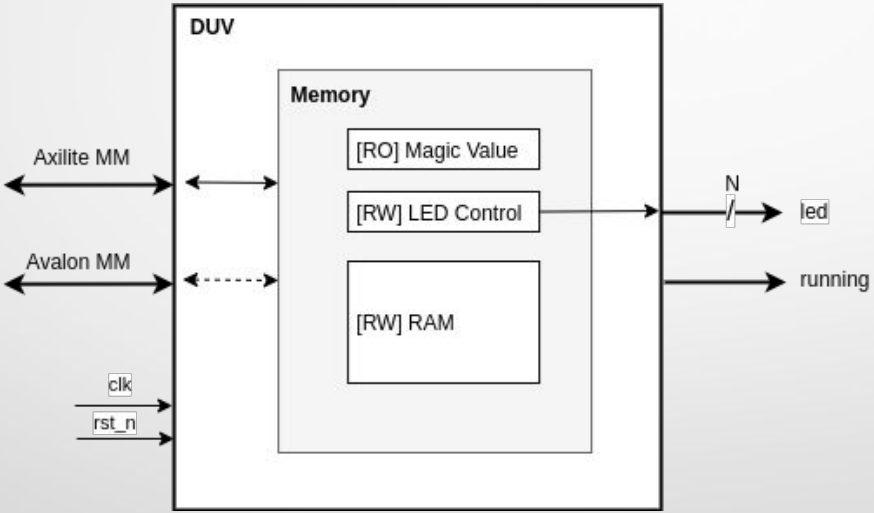
The Tutorial

- Device Under Verification



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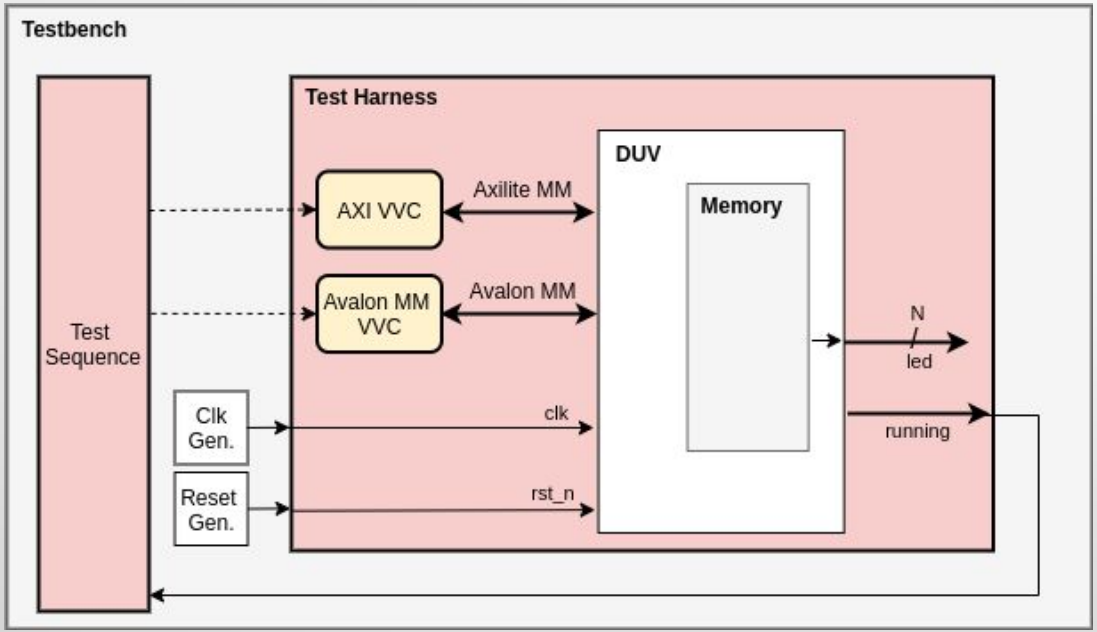
The Tutorial

- Testbench Architecture



The Tutorial

- Hands On !

Please now open the tutorial PDF.

You will find it in the repository* under doc/the-tutorial.pdf

* https://github.com/wurmmi/uvvm-tutorial

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