### Project diagrams and description

Digital Oscilloscope

### Top Level

Memory

CPU

ADC

VGA

Top Level Module

* **VGA driver.**
* **ADC driver.**
* **NIOS driver.**
* **Memory driver:**

1. **SDRAM**
2. **M9K SRAM**

VGA driver

Vsync/Hsync

Pixel Clock

H\_Pixel/V\_Pixel

Sync\_n/Blank\_n

Module exports

Clock/Reset

Module imports

This module imports Clock and reset signals from Top Level module, these signals are then used to generate the necessary Video Graphics Array signals such as Vertical synchronization signal (Vsync) and Horizontal synchronization signal (Hsync), this module also generates a 25MHz pixel clock for displaying 640\*480 resolution images at 60Hz refresh rate, no PLL used here since the base frequency of the used FPGA (DE2-115) is 50MHz and we can use a simple counter to generate the 25MHz signal.

The H\_Pixel and V\_Pixel signals are Horizontal and Vertical counters for scaning the entire monitor frame, these two signals use new terminology than the H\_counter/V\_counter signals used in the previous Digital Oscilloscope project uploaded on GitHub, the H\_Pixel has a range from 0-639 and the V\_Pixel has a range from 0-479.

Sync\_n/Blank\_n active low signals control the ADV7123 DAC to avoid sending data to the blanking area on the screen.

Assigned to Ahmad

### Top Level Description

ADC driver

ADC\_CLK

CS

Module exports

Clock/Reset

Module imports

The AD7352 is a differential input, dual ADC intergrated circuit, this dual-ADC has 3MSPS sampling rate with 12-bit accuarcy which is excellent accuarcy,

This ADC needs maximum power supply voltage of 2.75V which is considered low voltage, that means that the power consumption by this ADC is quite low.

The digital oscilloscope is built using based on this ADC

Assigned to Mustafa

Serial\_DATA

### Top Level Description

CPU driver

Module exports

Module imports

The NIOS CPU is a soft processor that can be included in any FPGA project, this RISC(Reduced Instruction Set) CPU can be added as an IP Core through Qsys System Integration Tool in Quartus software.

The CPU comes with different cores such as F core and E core for different targets, the E core for example is the economic core drivative of the processor which consume less logic elements and resources but at speed cost.

The NIOS is used in this project as a way to communicate with external PC host to transfer saved data in SDRAM to hard drive, the data stored in SDRAM is screen shot pixel data.

Assigned to Ahmad

### Top Level Description

Memory driver

The memory driver is divided into two main parts, the first one is used to manage the memory within the scope, storing analog data, frequency, images and others, while the second part (the SDRAM part) is specially used to store screen shots, the screen shots should be divided into two parts, the colormap of the image and pixel index for each screen shot or we could just save it as 24-bit data structure which will cost us more memory but in return will make things easier to read by NIOS.

This module has alot of input and output ports with high data trafficing, since every clock pulse plays a major role in controlling data paths that is linked to other modules, we can say that the scope heart is in this module.

No exports and imports are drawn since there are alot of them.

Assigned to Mustafa

Assigned to Ahmad

### Top Level Description

To/From SDRAM

Screen shot order

Incoming data, memory mapped reached

To host PC

Controls ADC chip and recieves serial data form the chip

General Storage

Controls

To Screen

I/O

I/O

ADC

VGA

M9K

Avalon Switch Fabric

SDRAM

NIOS

### General Diagram