Verification Plan of AHB-Lite

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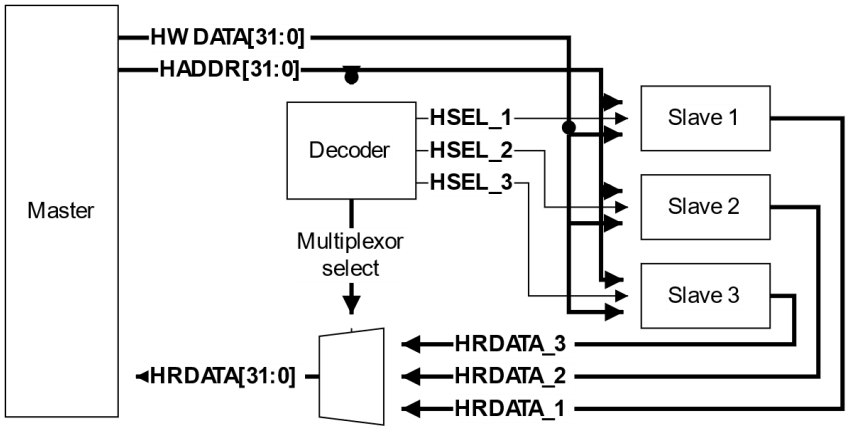
Introduction of AHB-Lite:

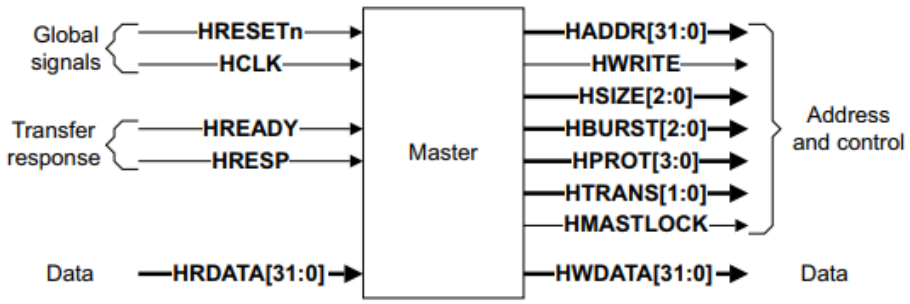
AHB LITE is the subset of AMBA 2. AHB used in such a SOC design where only one master, one slave or multiple slaves are required. AMBA AHB-Lite addresses the requirements of high-performance synthesizable designs. It is a bus interface that supports a single bus master and provides high-bandwidth operation.
AHB-Lite implements the features required for high-performance, high clock frequency systems including burst transfers, single-clock edge operation, non-tristate implementation and wide data bus configurations.



The main component types of an AHB-LITE system are Master, Slave, Decoder and Multiplexor.

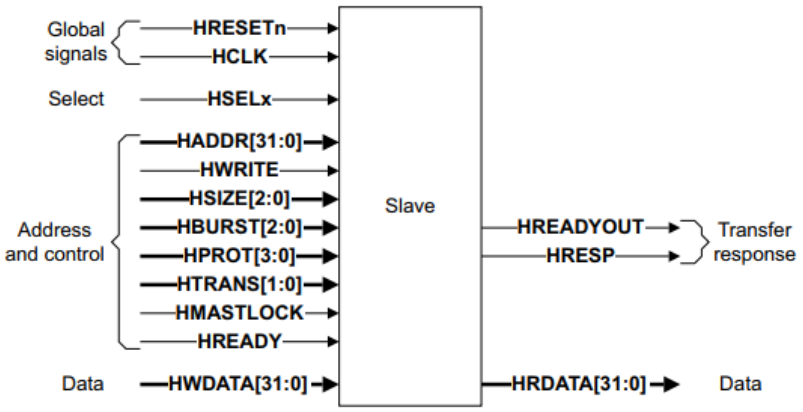
Master:

An AHB-Lite master provides address and control information to initiate read and write operations.



Slave:

An AHB-Lite slave responds to transfers initiated by masters in the system. The slave uses the HSELx select signal from the decoder to control when it responds to a bus transfer. The slave signals back to the master the success, failure and waiting of the data transfer.



Decoder:

This component decodes the address of each transfer and provides a select signal for the slave that is involved in the transfer. It also provides a control signal to the multiplexor. A single centralized decoder is required in all AHB-Lite implementations that use two or more slaves.

Multiplexor:

A slave-to-master multiplexor is required to multiplex the read data bus and response signals from the slaves to the master. The decoder provides control for the multiplexor. A single centralized multiplexor is required in all AHB-Lite implementations that use two or more slaves.

Verification Plan

No.	Feature	Test Description	Ref.	Type	Result	Expected outcome	Comments
1	Direction of Data Transfer (HWRITE)	Write transfer from Master to slave.	3.1	TR		The Data must be written at the address B and a completed transfer is signalled i.e. HRESP should be low and HREADY should be high.	HWRITE is high indicating a write transfer.
2	Direction of Data Transfer (HWRITE)	Read transfer from Slave to Master.	3.1	TR		The Data must be read from the address and completed transfer is signalled. HRESP should be low and HREADY should be High.	When HWRITE is Low a read transfer is performed and the slave must generate the data on the read data bus HRDATA [31:0].
3	Read or Write transfer with wait states	When HREADY is low it shows a read or write transfer with wait states.	3.1/Fig 3-3	TR		During HREADY is low (waited state) the slave adding latency in the write and read transfer.	In this state the master cannot cancel the transfer. After wait slave perform read or write operation.
4	Transfer with HSEL is low	Generate a transfer while HSEL is low.		TR		Slave is not selected so no output.	
5	Send 00 value of HTRANS	Set 00 to HTRANS and send a transfer.	3.2	A		Slave should ignore transfer and set HRESP is 0.	
6	Writing multiple words	Multiple words is written after the other clock edges on same address (read from same address on next active clock edge).	3.1	TR		Last written word must be the output.	

7	Master Signal: IDLE HTRANS [1:0] =b00	An Address A is driven onto the bus. An idle transfer is inserted to this address.	3.2	A		Slave provides a zero wait Okay response. The transfer must be ignored by the slave.	
8	Master Signal: BUSY HTRANS [1:0] =b01	Address A and B are driven onto the bus. When a BUSY transfer is inserted on address A then the address and control signals must reflect the next burst transfer.	3.2	A		After the complete transfer signal from the slave for address A; address B is sampled during the sequential transfer	
9	Address changes during wait States (During an IDLE transfer)	During a waited transfer, the master is permitted to change the address for IDLE transfers. When HTRANS transfer type changes to NONSEQ the master must keep the address constant until HREADY is High.	3.6.2/ Fig 3-16	A		During the address phases of address A and address B the slave samples the addresses at the rising edge of the clock cycle. The slave will signal a completed transfer after the transfer to address A. The IDLE transfers are ignored by the slave between addresses A and B. Then, the slave will signal a completer transfer after the transfer to address B	Address change Successfully.

10	Address changes during wait States (After an ERROR response)	During a waited transfer if the slave responds with an ERROR response then the master is permitted to change the address when HREADY is low.	3.6.2/ Fig 3-17	A		The addresses are sampled at the rising edge of the clock cycle in their address phases During the first cycle of the data phase of address A, the slave provides an OKAY response. During the first cycle of the data phase of address B, the slave provides an OKAY response. Since the address phase was extended therefor in the next cycle slave will generate an ERROR response. During this cycle, the transfer type changed successfully. In the next cycle, the slave responds with an OKAY signal	Address change during awaited transfer after an ERROR
11	Slave response: Transfer done	The transfer is completed successfully.	5.1.1	A		Slave must give HREADY HIGH and HRESP OKAY	HREADY high indicates transfer complete and response is OKAY.
12	Slave response: Transfer pending	The Transfer is pending	5.1.2	A		Slave must give HREADY low and HRESP OKAY.	HREADY Low indicates the transfer is not completed yet and is pending

13	Slave response: Transfer failed	The transfer is not completed successfully.	5.1.3	A		HRESP must be HIGH. Two cycle response is required for an error condition.	When the transaction is failed, the response, HRESP is HIGH, indicating an error.
14	Clock (HCLK)	Each AHB-Lite component uses a single clock signal.	7.1.1	A		All inputs are sampled at rising edge of HCLK	All Output signal changes must occur after the rising edge of HCLK.
15	Reset (HRESETn)	During Reset all masters must ensure the address and control signals are at valid levels and that HTRANS [1:0] indicates IDLE. During reset all slaves must ensure that HREADYOUT is High.	7.1.2	TR		All previous binary information in the bust elements will be lost	
16	Send sequential transfer to a non-existent address	Generate an address that is not present in the memory. Send seq. transfer to that address. HRESP should become high for such transfer.	4	A		HRESP should become high for such transfer within next 2 cycles	
17	Send single burst to the memory	Generate a single burst and send to random address in the memory.	5	A		HRESP should be zero and HREADY should be 1 in next cycle which signals a successful transfer	

Explanation of Different Fields

No.	The serial number of the test.
Feature	The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.
Test Description	A detailed description of the test case being performed. You can be as verbose as you want.
Ref.	Reference to the section in the related standard document. The section number as well as page numbers should be described here.
Type	Type of the test. Whether the test is an assertion (A) or a transaction (T) type.
Result	Pass (P) or Fail (F).
Comments	Any other comments about the test or its results that you want to mention.