Verification Plan of AHB-Lite

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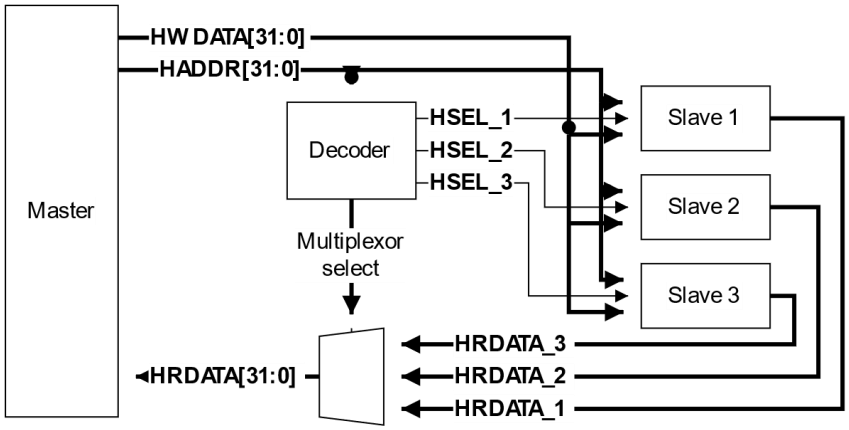
Introduction of AHB-Lite:

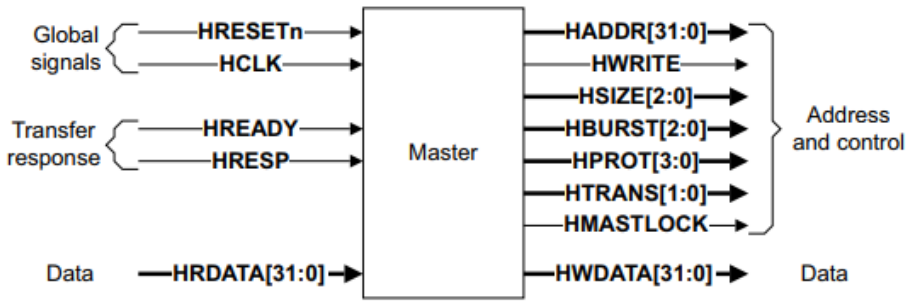
AHB LITE is the subset of AMBA 2. AHB used in such a SOC design where only one master, one slave or multiple slaves are required. AMBA AHB-Lite addresses the requirements of high-performance synthesizable designs. It is a bus interface that supports a single bus master and provides high-bandwidth operation.
AHB-Lite implements the features required for high-performance, high clock frequency systems including burst transfers, single-clock edge operation, non-tristate implementation and wide data bus configurations.



The main component types of an AHB-LITE system are Master, Slave, Decoder and Multiplexor.

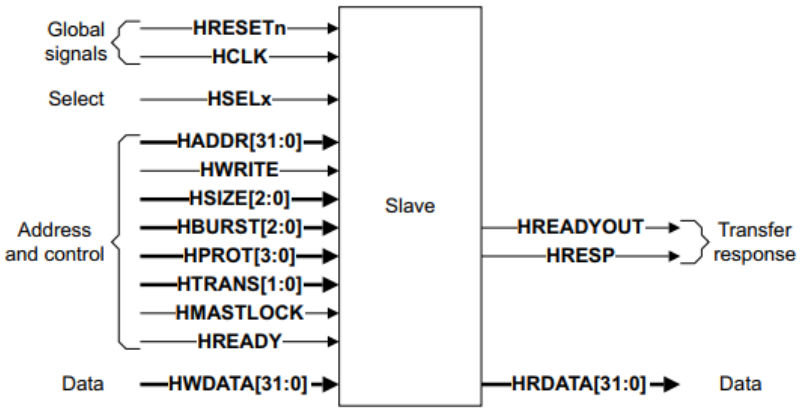
Master:

An AHB-Lite master provides address and control information to initiate read and write operations.



Slave:

An AHB-Lite slave responds to transfers initiated by masters in the system. The slave uses the HSELx select signal from the decoder to control when it responds to a bus transfer. The slave signals back to the master the success, failure and waiting of the data transfer.



Decoder:

This component decodes the address of each transfer and provides a select signal for the slave that is involved in the transfer. It also provides a control signal to the multiplexor. A single centralized decoder is required in all AHB-Lite implementations that use two or more slaves.

Multiplexor:

A slave-to-master multiplexor is required to multiplex the read data bus and response signals from the slaves to the master. The decoder provides control for the multiplexor. A single centralized multiplexor is required in all AHB-Lite implementations that use two or more slaves.

Verification Plan

No.	Feature	Test Description	Ref.	Type	Result	Comments
1	Direction of Data Transfer (HWRITE)	When HWRITE is High it indicate a write transfer and the master broadcasts data on the write data bus HWDATA [31:0].	3.1	TR		Write Transfer from Master to Slave.
2	Direction of Data Transfer (HWRITE)	When HWRITE is Low a read transfer is performed and the slave must generate the data on the read data bus HRDATA [31:0].	3.1	TR		Read transfer from Slave to Master.
3	Read transfer with wait states	When HREADY is low it shows a read transfer with wait states.	3.1/Fig 3-3	TR		
4	Transfer Type IDLE HTRANS[1:0] b00	When IDLE transfer is inserted to an address. Slaves must always provide a zero wait state OKAY response.	3.2	TR		The transfer must be ignored by the Slave.
5	Slave Error Response	If a slave provides an error response then the master can cancel the remaining transfers in the burst.	3.5.2			
6	Waited Transfer Type changes (IDLE to NONSEQ)	During a waited transfer the master is permitted to change the transfer type from IDLE to NONSEQ and must keep HTRANS constant until HREADY is high.	3.6.1/ Fig 3-13	A		
7	Waited Transfer Type changes (BUSY to SEQ)	During a waited transfer for a fixed length burst, transfer type change from BUSY to SEQ and the master must keep HTRANS constant until HREADY is high.	3.6.1/ Fig 3-14	TR		
8	Waited Transfer Type changes (BUSY to NONSEQ)	During a waited transfer for an undefined length burst, INCR, the transfer type change from BUSY to any other transfer type, when HREADY is low. The burst continues if a SEQ transfer is performed but terminates if an IDLE or NONSEQ transfer is performed.	3.6.1/ Fig 3-15	A		

9	Address changes during wait States (During an IDLE transfer)	During a waited transfer, the master is permitted to change the address for IDLE transfers. When HTRANS transfer type changes to NONSEQ the master must keep the address constant until HREADY is High.	3.6.2/ Fig 3-16	A		
10	Address changes during wait States (After an ERROR response)	During a waited transfer if the slave responds with an ERROR response then the master is permitted to change the address when HREADY is low.	3.6.2/ Fig 3-17	A		
11	Locked Transfers (HMASTLOCK)	This signal indicates to any slave that the current transfer sequence is indivisible and must therefore be processed before any other transaction are processed.	3.3	A		
12	Default Slave (NONSEQ or SEQ)	If a NONSEQ or SEQ transfer is attempted to a non-existent address location then the default slave provides an ERROR response.	4.1.1	TR		
13	Default Slave (IDLE or BUSY)	IDLE or BUSY transfers to non-existent locations result in a zero wait state OKAY response.	4.1.1	TR		
14	Clock (HCLK)	Each AHB-Lite component uses a single clock signal. All Output signal changes must occur after the rising edge of HCLK.	7.1.1	A		
15	Reset (HRESETn)	During Reset all masters must ensure the address and control signals are at valid levels and that HTRANS[1:0] indicates IDLE. During reset all slaves must ensure that HREADYOUT is High.	7.1.2			

Explanation of Different Fields

No.	The serial number of the test.
Feature	The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.
Test Description	A detailed description of the test case being performed. You can be as verbose as you want.
Ref.	Reference to the section in the related standard document. The section number as well as page numbers should be described here.
Type	Type of the test. Whether the test is an assertion (A) or a transaction (T) type.
Result	Pass (P) or Fail (F).
Comments	Any other comments about the test or its results that you want to mention.