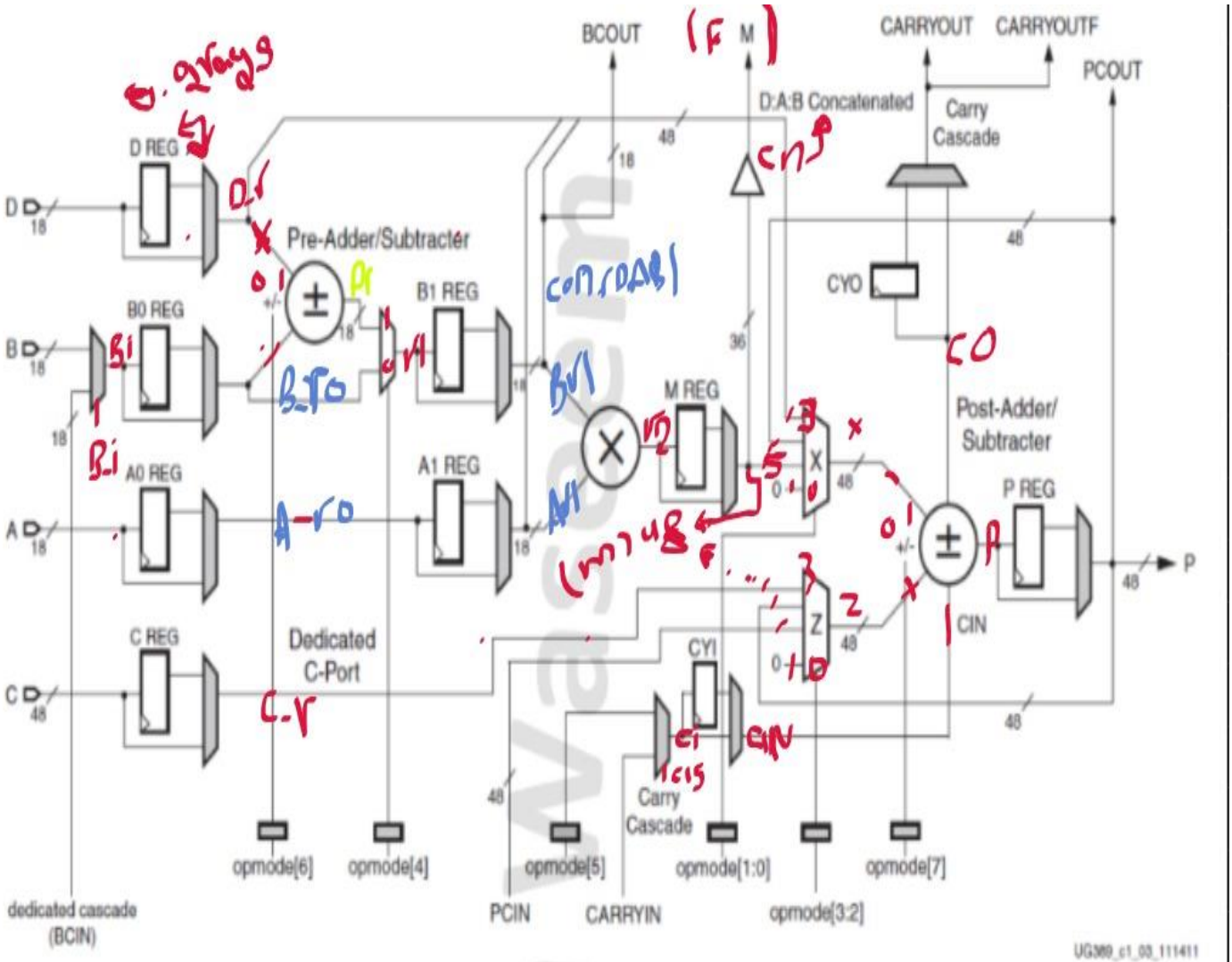
// data flow



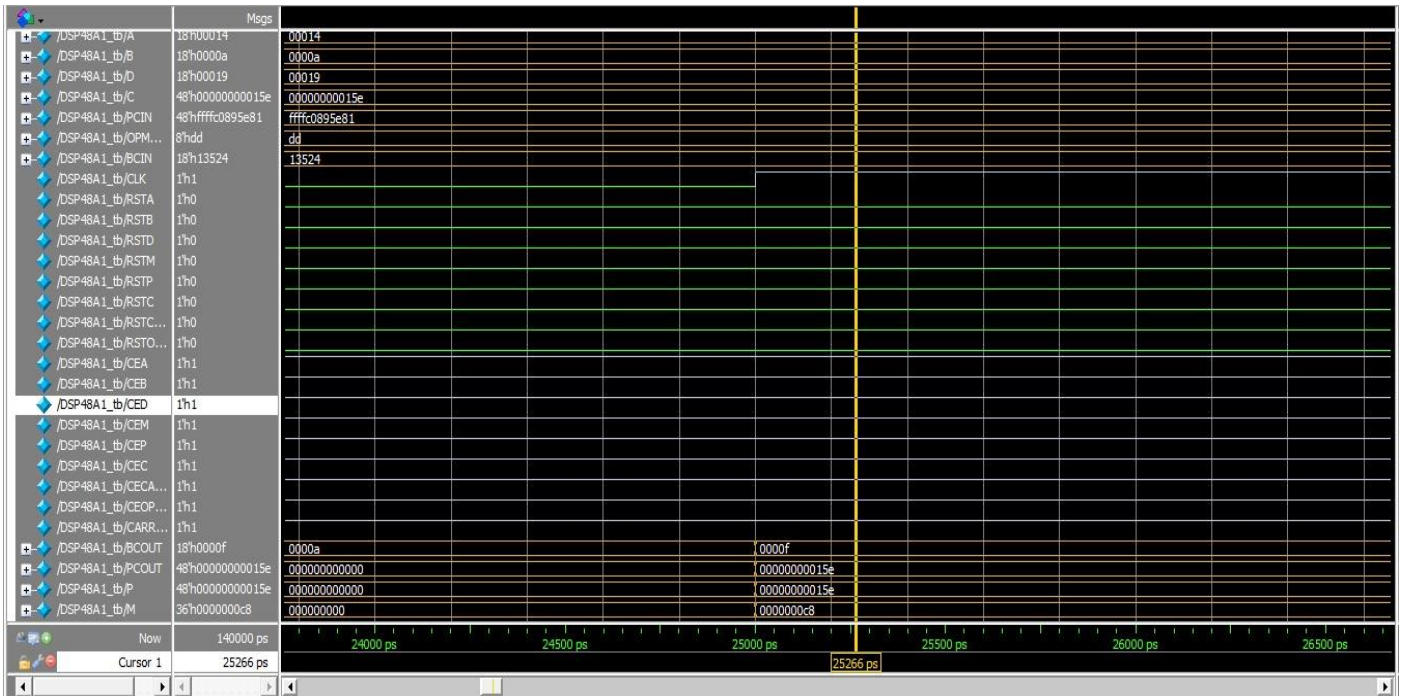
Note: opmode input has a register and mux pair in the design entry the same way as the input A, D, or C

// results

```
# [RESET correct] Outputs  zero after reset
# [correct test] Inputs: A=    20 B=    10 D=    25 C=           350 PCIN=281473911971457
# Expected -> BCOUT: 0000f, M: 00000012c, P: 000000000032, CARRYOUT: 0
# Got -> BCOUT: 0000f, M: 00000012c, P: 000000000032, CARRYOUT: 0
# [correct test] Inputs: A=    20 B=    10 D=    25 C=           350 PCIN=      112818957
# Expected -> BCOUT: 00023, M: 0000002bc, P: 000000000000, CARRYOUT: 0
# Got -> BCOUT: 00023, M: 0000002bc, P: 000000000000, CARRYOUT: 0
# [correct test] Inputs: A=    20 B=    10 D=    25 C=           350 PCIN=281472983847442
# Expected -> BCOUT: 0000a, M: 0000000c8, P: 000000000000, CARRYOUT: 0
# Got -> BCOUT: 0000a, M: 0000000c8, P: 000000000000, CARRYOUT: 0
# [correct test] Inputs: A=     5 B=     6 D=    25 C=           350 PCIN=          3000
# Expected -> BCOUT: 00006, M: 00000001e, P: fe6fffec0bb1, CARRYOUT: 1
# Got -> BCOUT: 00006, M: 00000001e, P: fe6fffec0bb1, CARRYOUT: 1
# All tests passed successfully!
# ** Note: $stop    : TB_DSP_48_A1.v(130)
#    Time: 140 ns  Iteration: 1  Instance: /DSP48A1_tb
# Break in Module DSP48A1_tb at TB_DSP_48_A1.v line 130
```

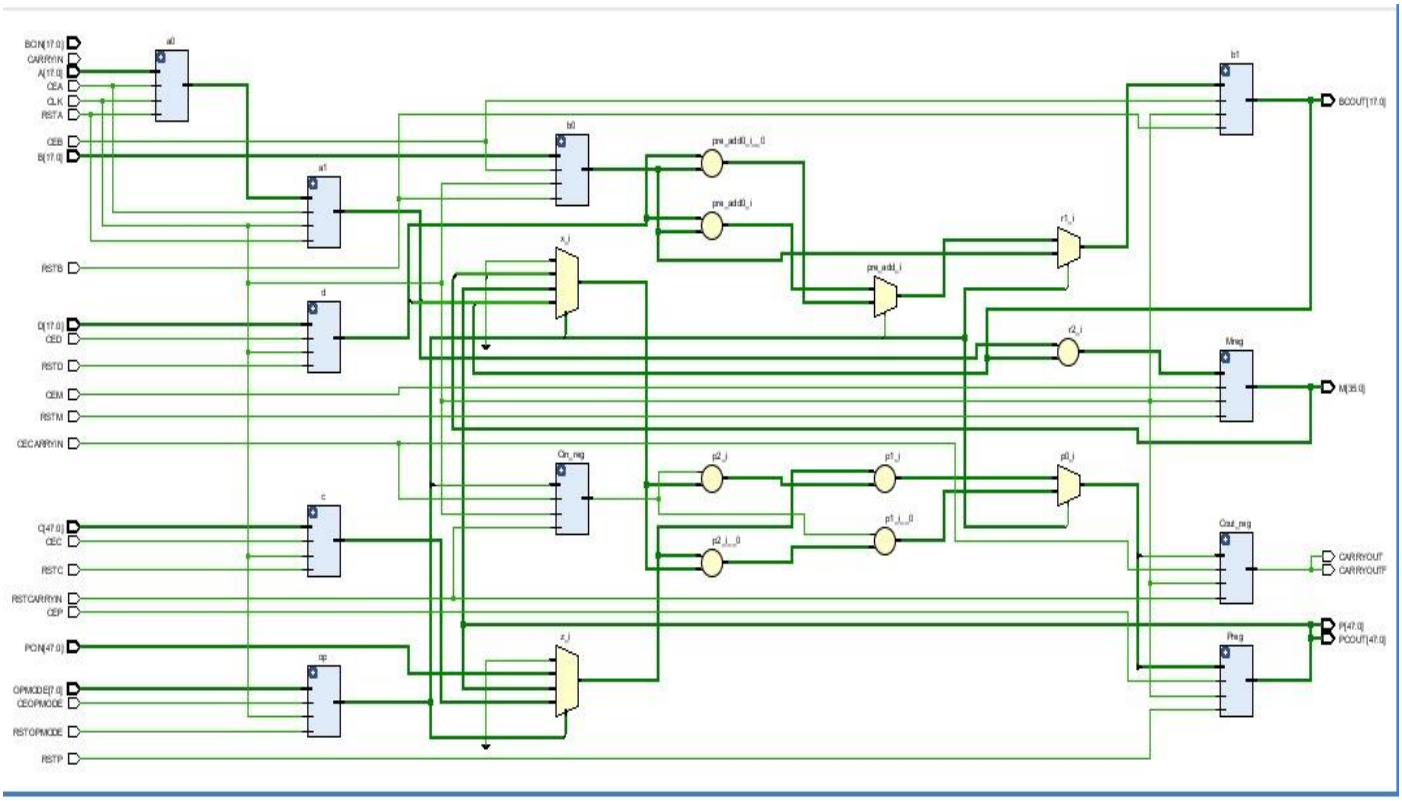
All outputs are correct

// simulation



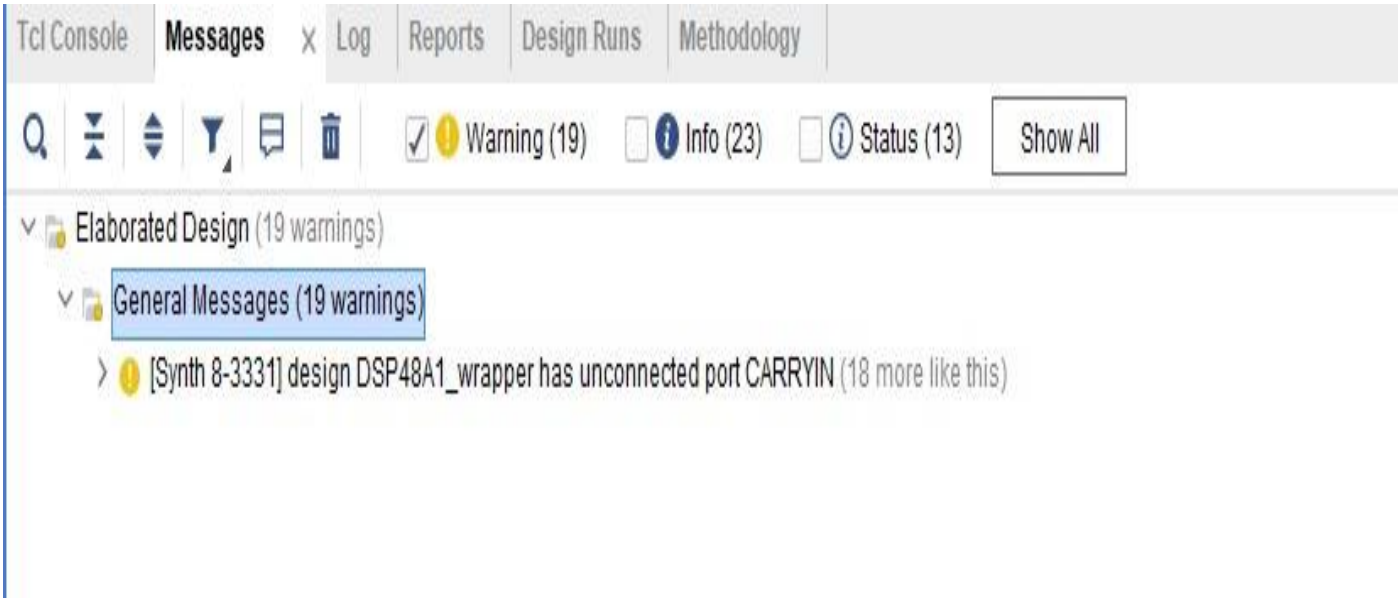
// correct wave form

// Schematic (RTL)

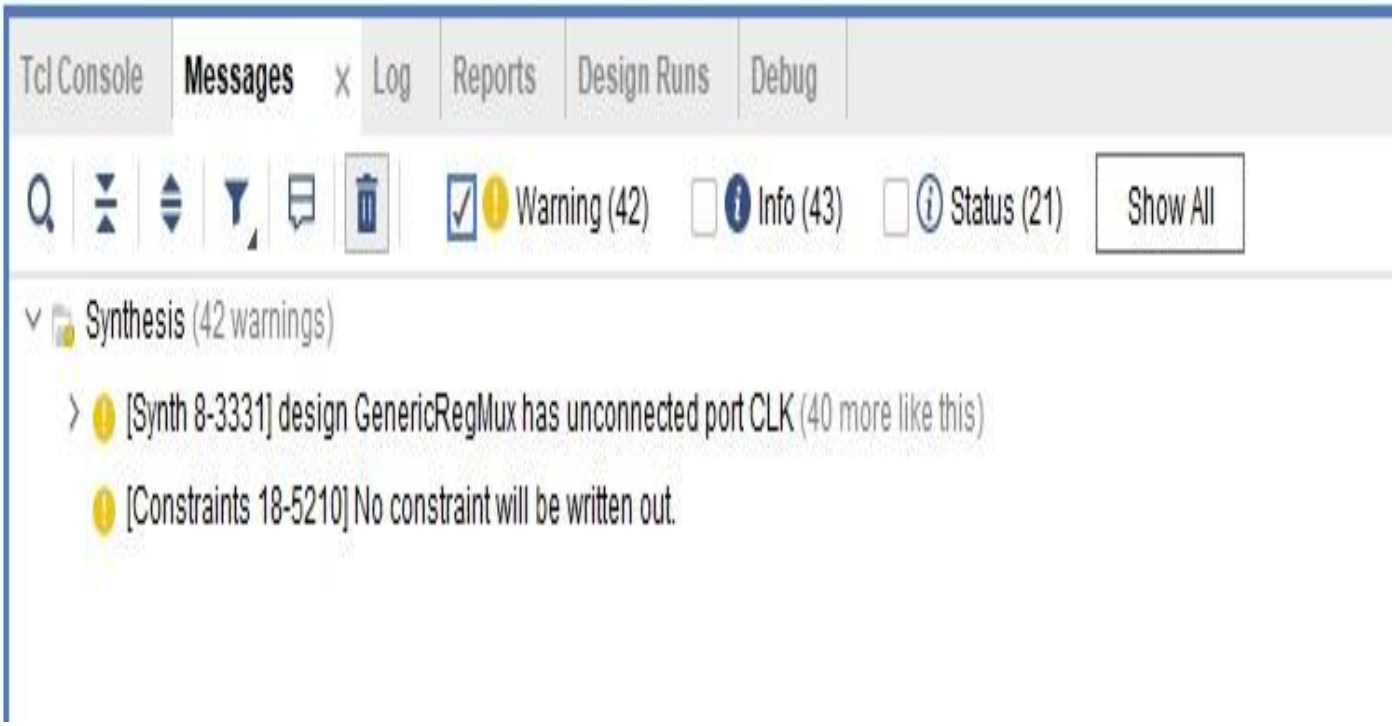


// blue block : in file (reg_or_wire.v)

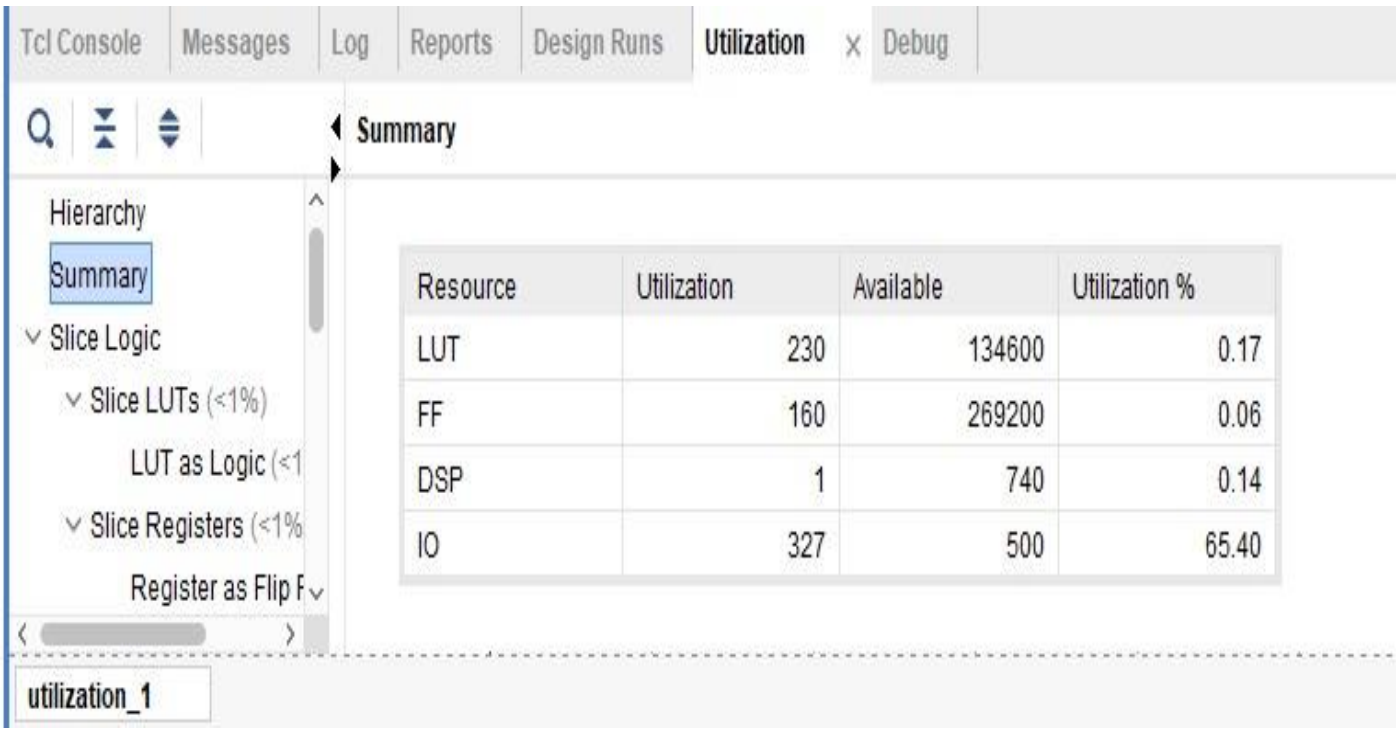
// messages(RTL)



// message(synt.)

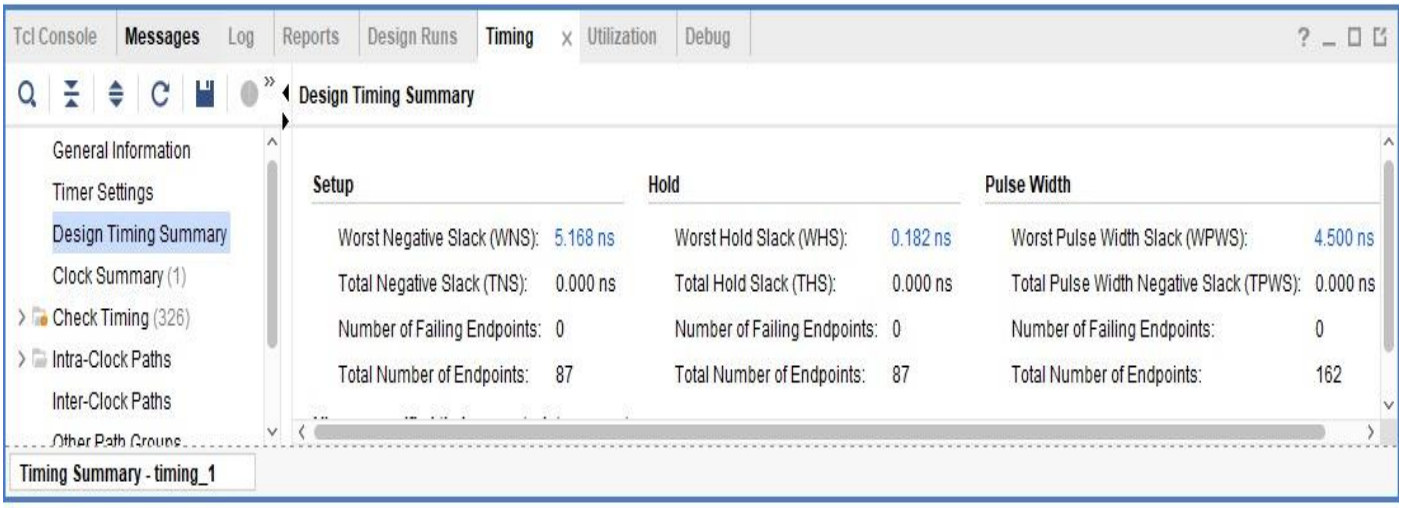


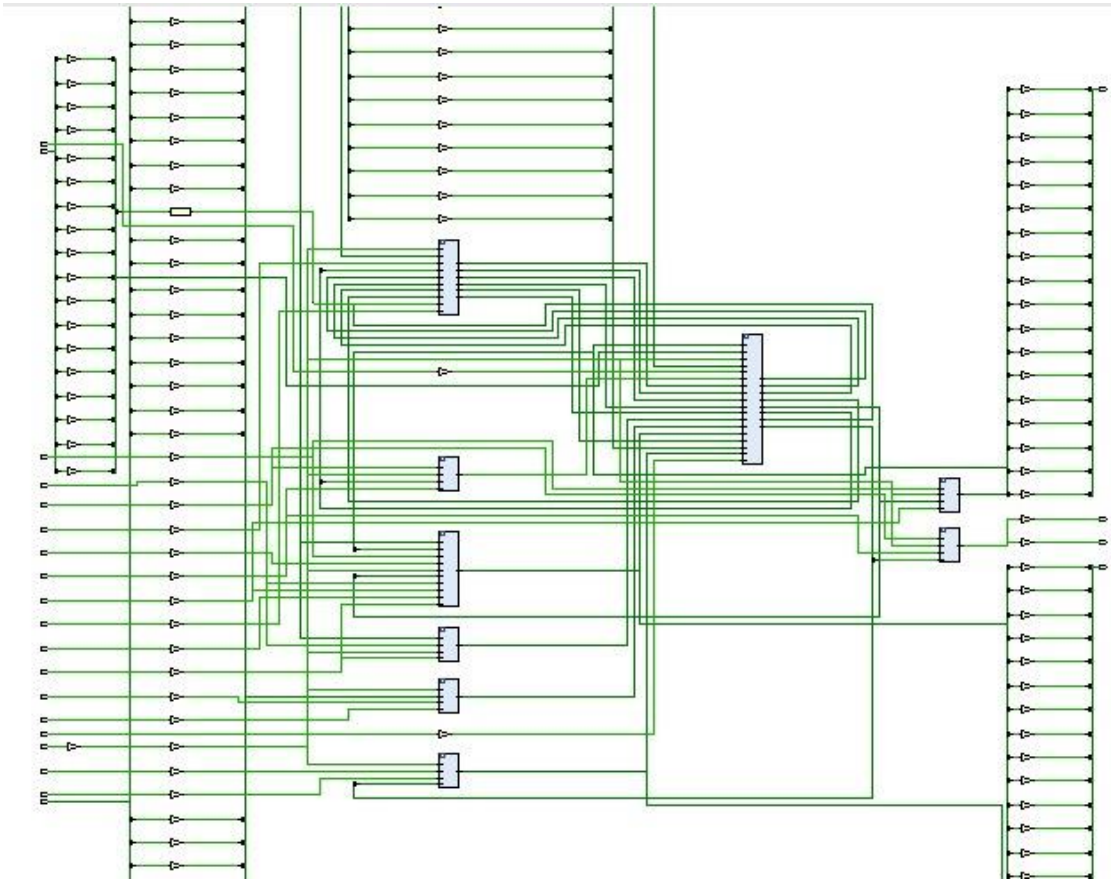
// Utilization report (synt.)

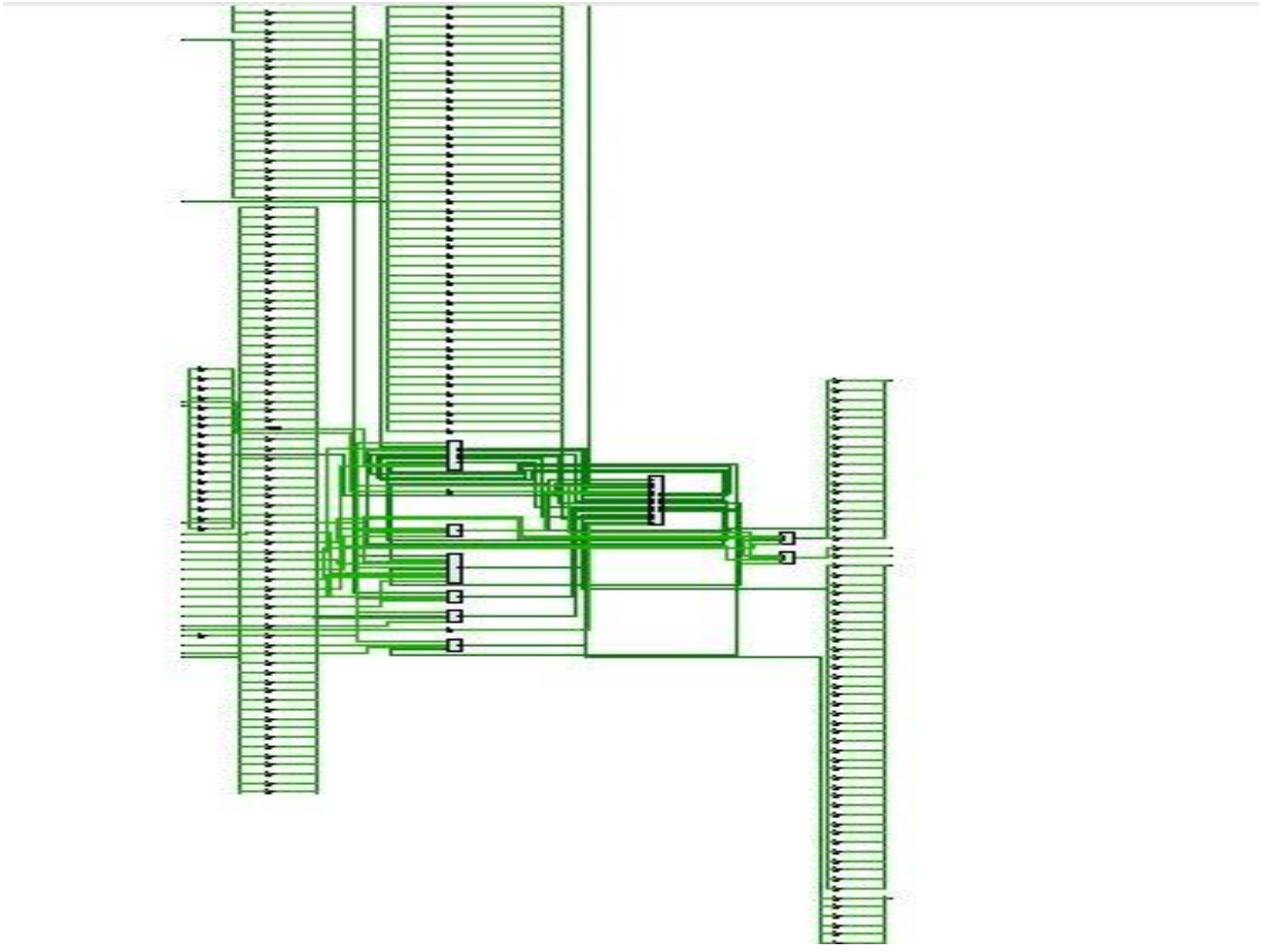


Resource	Utilization	Available	Utilization %
LUT	230	134600	0.17
FF	160	269200	0.06
DSP	1	740	0.14
IO	327	500	65.40

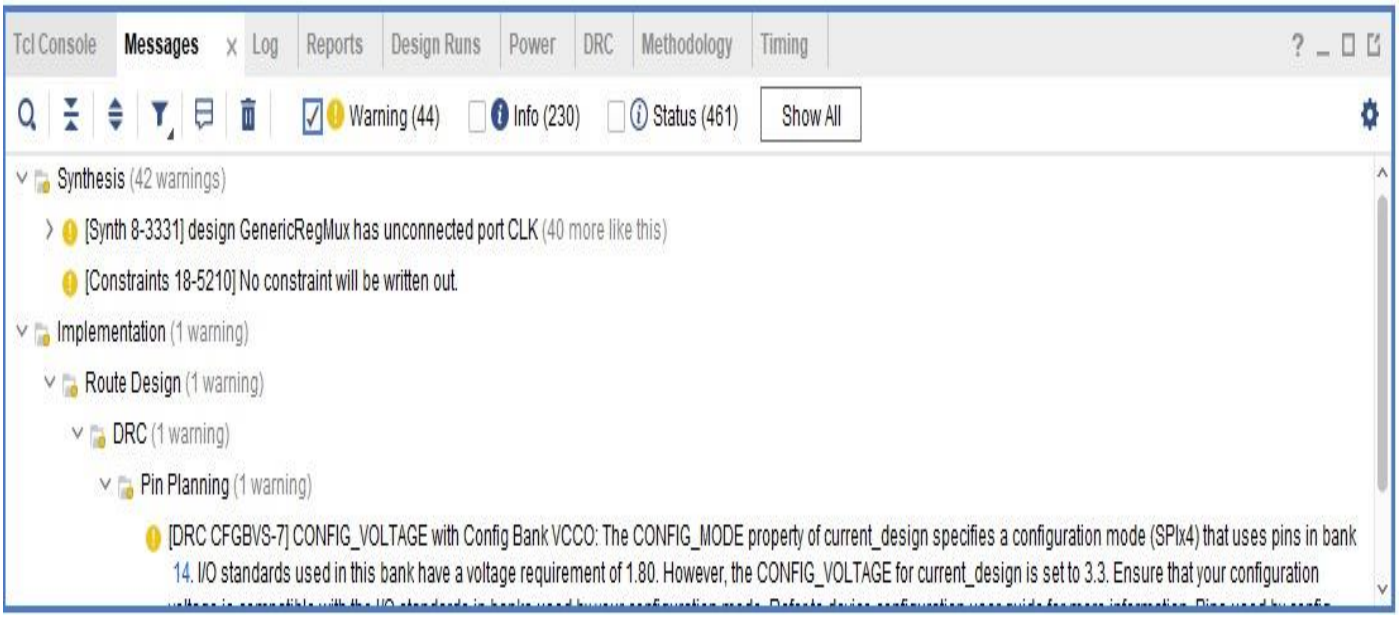
//timing report and tech. schmatic



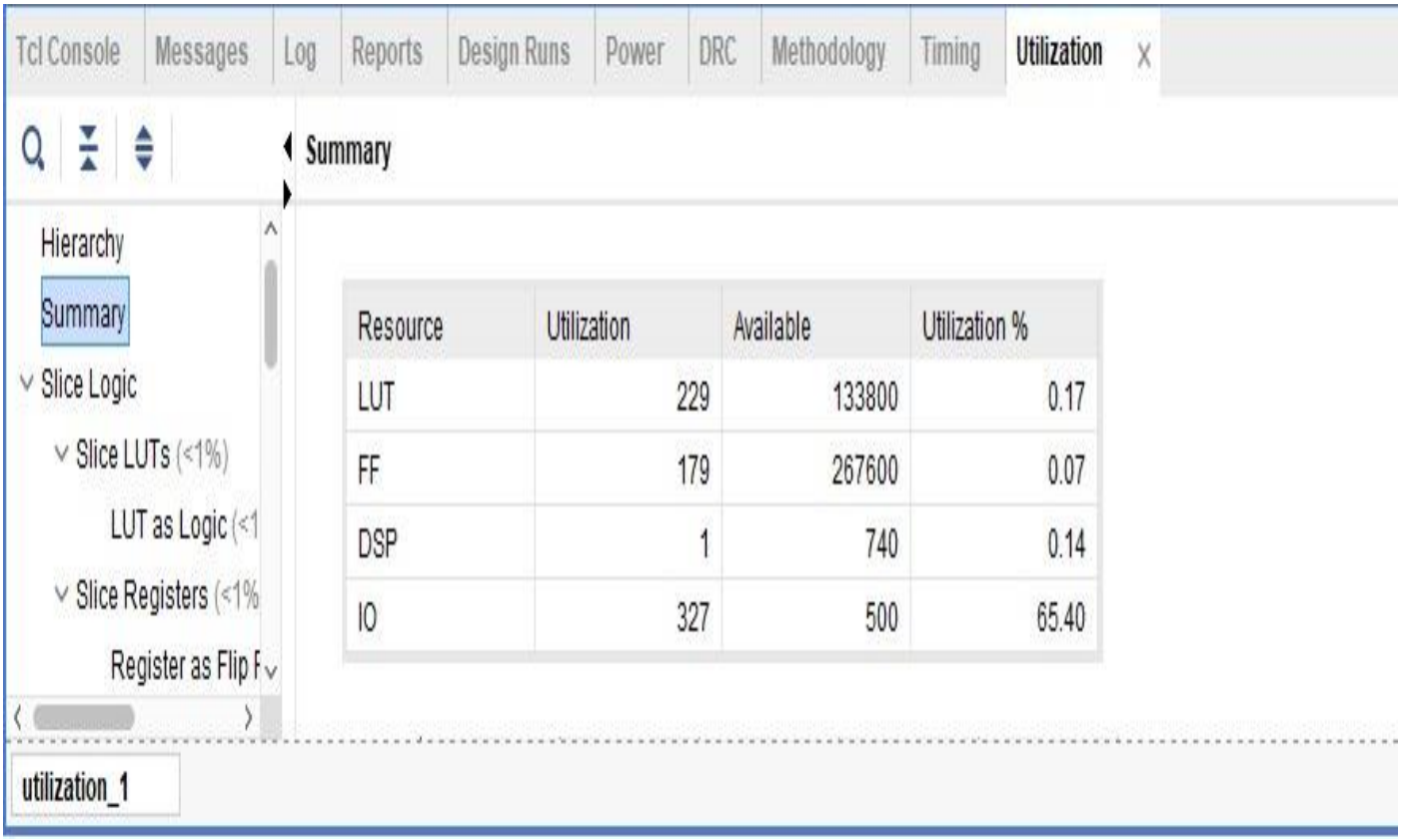




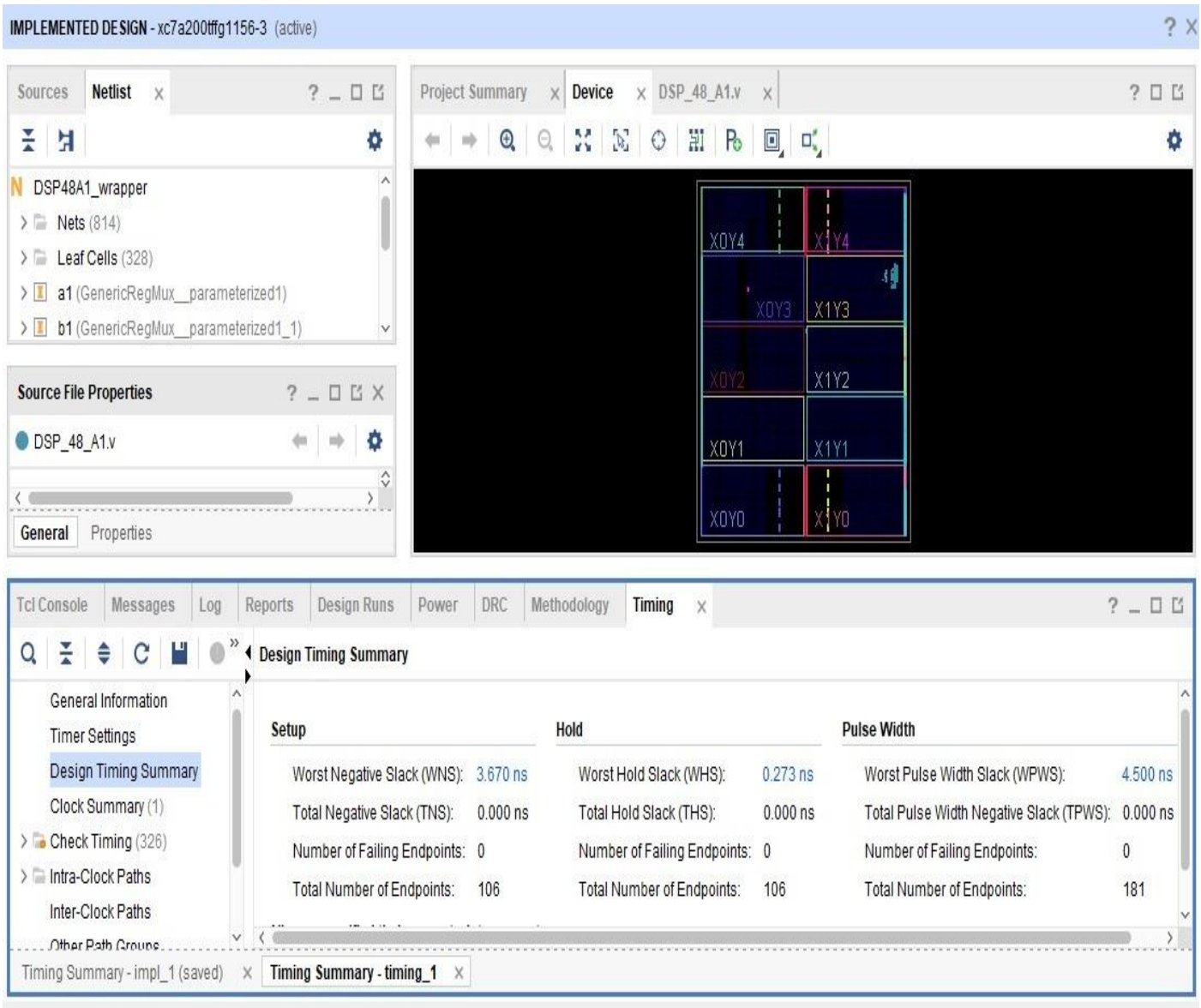
// message(impl.)



// Utilization report (impl.)



//timing report and device snippets



Note : Linting tool not working yet .