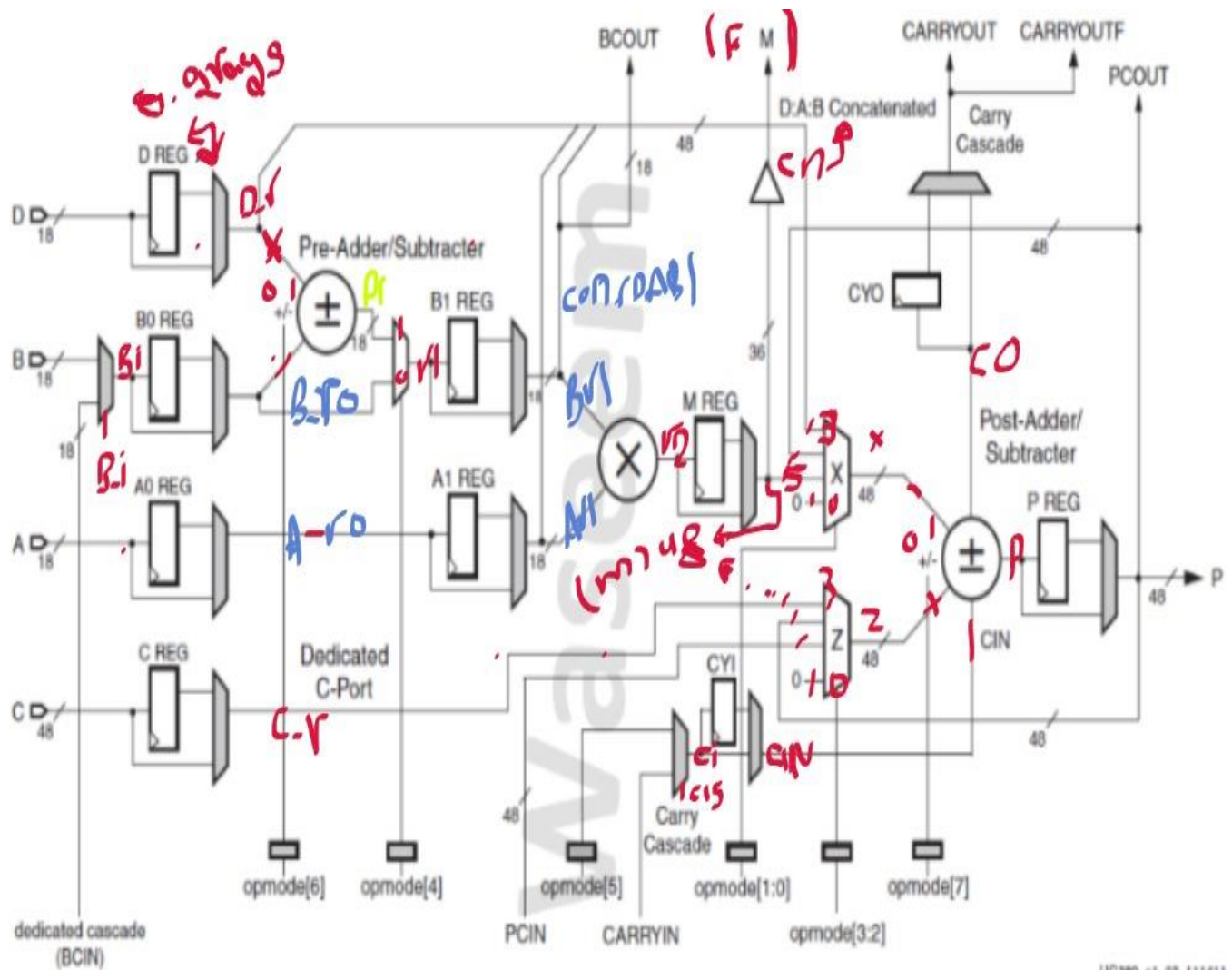


// data flow



UG389_61_03_111411

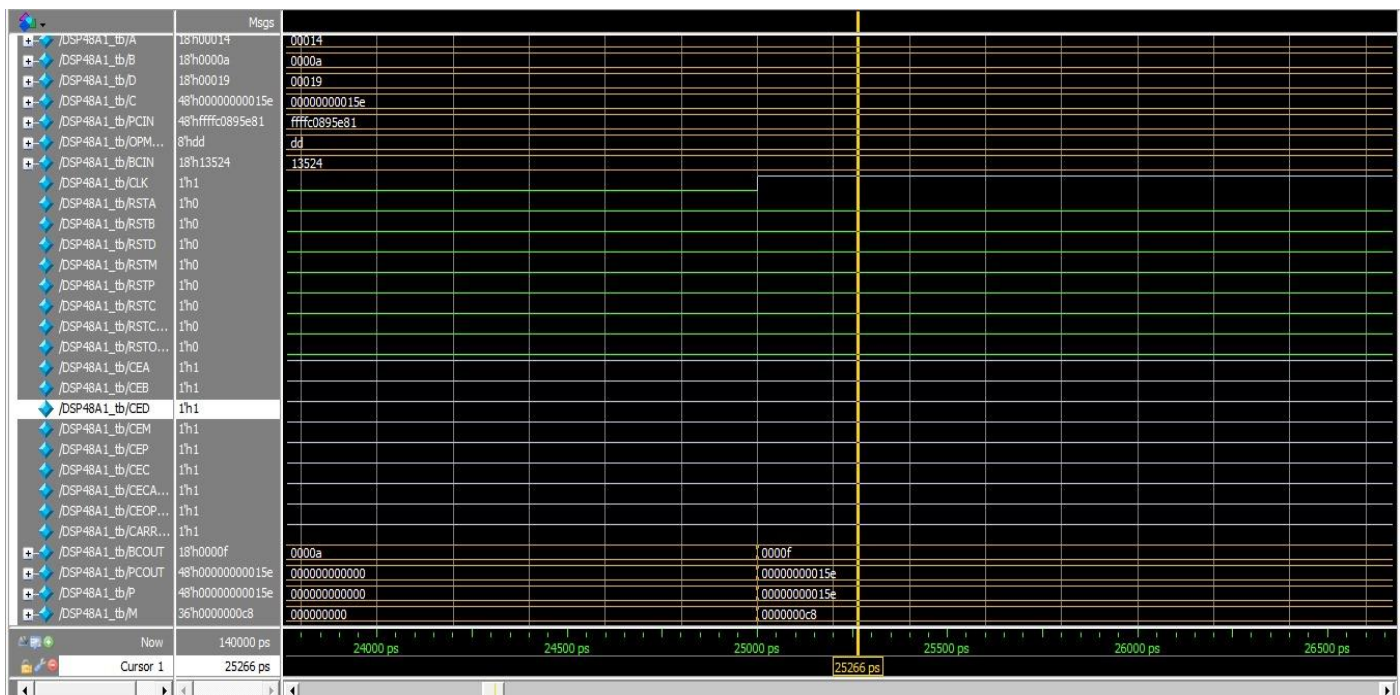
Note: opmode input has a register and mux pair in the design entry the same way as the input A, D, or C

// results

```
# [RESET correct] Outputs zero after reset
# [correct test] Inputs: A= 20 B= 10 D= 25 C= 350 PCIN=281473911971457
# Expected -> BCOUT: 0000f, M: 00000012c, P: 000000000032, CARRYOUT: 0
# Got -> BCOUT: 0000f, M: 00000012c, P: 000000000032, CARRYOUT: 0
# [correct test] Inputs: A= 20 B= 10 D= 25 C= 350 PCIN= 112818957
# Expected -> BCOUT: 00023, M: 0000002bc, P: 000000000000, CARRYOUT: 0
# Got -> BCOUT: 00023, M: 0000002bc, P: 000000000000, CARRYOUT: 0
# [correct test] Inputs: A= 20 B= 10 D= 25 C= 350 PCIN=281472983847442
# Expected -> BCOUT: 0000a, M: 0000000c8, P: 000000000000, CARRYOUT: 0
# Got -> BCOUT: 0000a, M: 0000000c8, P: 000000000000, CARRYOUT: 0
# [correct test] Inputs: A= 5 B= 6 D= 25 C= 350 PCIN= 3000
# Expected -> BCOUT: 00006, M: 00000001e, P: fe6fffec0bb1, CARRYOUT: 1
# Got -> BCOUT: 00006, M: 00000001e, P: fe6fffec0bb1, CARRYOUT: 1
# All tests passed successfully!
# ** Note: $stop : TB_DSP_48_A1.v(130)
# Time: 140 ns Iteration: 1 Instance: /DSP48A1_tb
# Break in Module DSP48A1_tb at TB_DSP_48_A1.v line 130
```

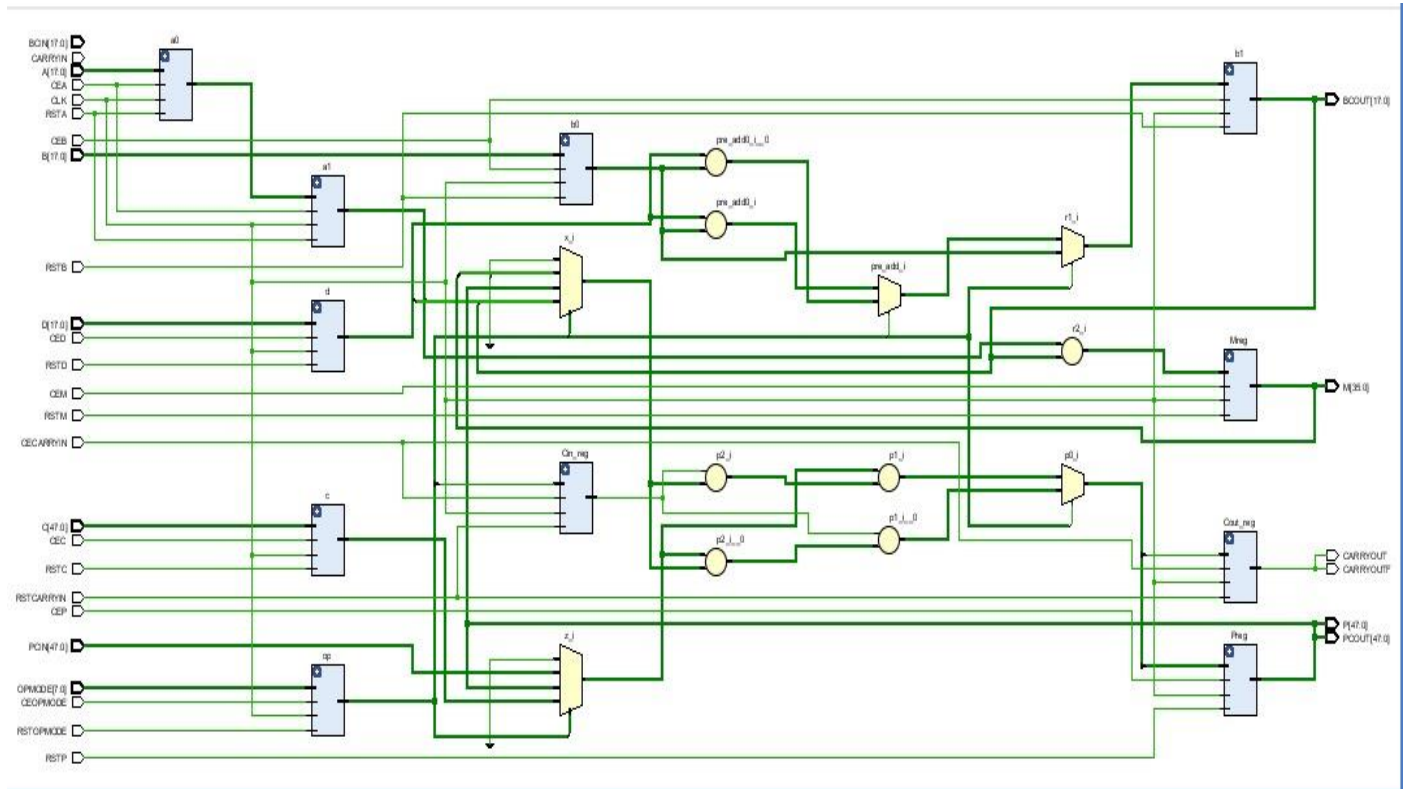
All outputs are correct

// simulation



// correct wave form

// Schematic (RTL)



// blue block : in file (reg_or_wire.v)

// messages(RTL)



// message(synt.)

The screenshot shows the 'Messages' window with tabs for 'Tcl Console', 'Messages', 'Log', 'Reports', 'Design Runs', and 'Debug'. The 'Messages' tab is active, displaying a search bar and filters for 'Warning (42)', 'Info (43)', and 'Status (21)', along with a 'Show All' button. A tree view on the left shows 'Synthesis (42 warnings)' expanded, listing two warnings: '[Synth 8-3331] design GenericRegMux has unconnected port CLK (40 more like this)' and '[Constraints 18-5210] No constraint will be written out.'

// Utilization report (synt.)

The screenshot shows the 'Utilization' window with tabs for 'Tcl Console', 'Messages', 'Log', 'Reports', 'Design Runs', 'Utilization', and 'Debug'. The 'Utilization' tab is active, displaying a 'Summary' section. On the left, a 'Hierarchy' tree shows 'Summary' selected under 'Slice Logic'. The main area contains a table with resource utilization data.

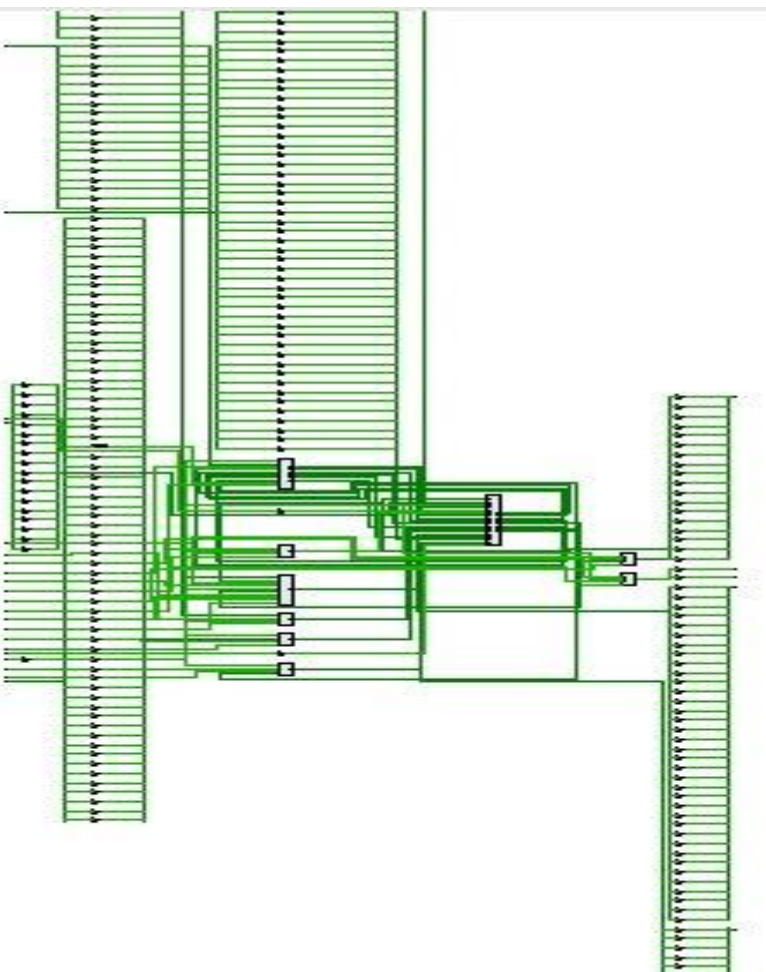
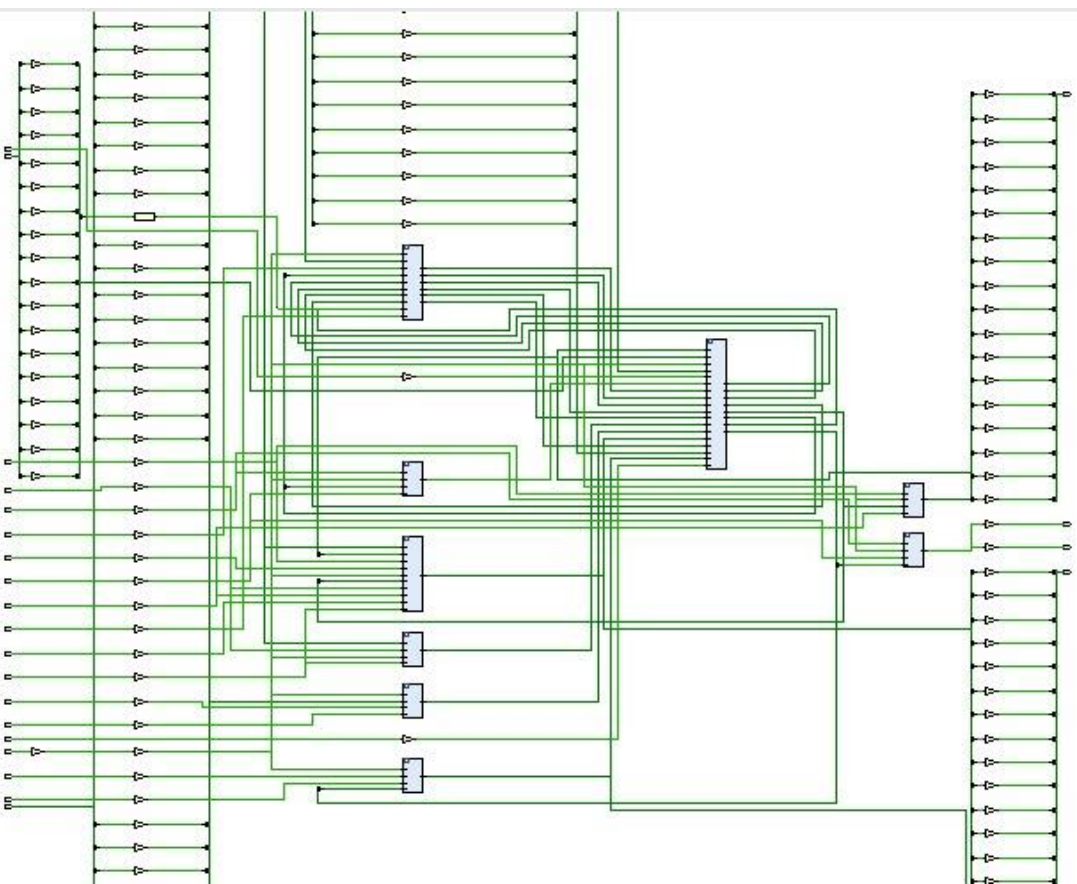
Resource	Utilization	Available	Utilization %
LUT	230	134600	0.17
FF	160	269200	0.06
DSP	1	740	0.14
IO	327	500	65.40

At the bottom left, a tab labeled 'utilization_1' is visible.

//timing report and tech. schmatic

Tcl Console	Messages	Log	Reports	Design Runs	Timing x	Utilization	Debug	?	_	□	↗
Design Timing Summary											
General Information											
Timer Settings											
Design Timing Summary											
Clock Summary (1)											
> Check Timing (326)											
> Intra-Clock Paths											
Inter-Clock Paths											
Other Path Groups											
Timing Summary - timing_1											

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.168 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 87	Total Number of Endpoints: 87	Total Number of Endpoints: 162



// message(impl.)

The Messages window displays a list of warnings. The categories and their counts are: Synthesis (42 warnings), Implementation (1 warning), Route Design (1 warning), DRC (1 warning), and Pin Planning (1 warning). The first warning under Synthesis is: [Synth 8-3331] design GenericRegMux has unconnected port CLK (40 more like this). The second warning is: [Constraints 18-5210] No constraint will be written out. The warning under Pin Planning is: [DRC CFGBVS-7] CONFIG_VOLTAGE with Config Bank VCC0: The CONFIG_MODE property of current_design specifies a configuration mode (SPIx4) that uses pins in bank 14. I/O standards used in this bank have a voltage requirement of 1.80. However, the CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in bank used by your configuration mode. Defects during configuration use guide for more information. Pins used by user6.

// Utilization report (impl.)

The Utilization report window shows a summary table of resource utilization. The table has four columns: Resource, Utilization, Available, and Utilization %. The data is as follows:

Resource	Utilization	Available	Utilization %
LUT	229	133800	0.17
FF	179	267600	0.07
DSP	1	740	0.14
IO	327	500	65.40

The left sidebar shows a hierarchy of reports: Hierarchy, Summary (selected), Slice Logic, Slice LUTs (<1%), LUT as Logic (<1%), Slice Registers (<1%), and Register as Flip F.

//timing report and device snippets

IMPLEMENTED DESIGN - xc7a200tfg1156-3 (active)

Sources Netlist x ? _ □

DSP48A1_wrapper

- > Nets (814)
- > Leaf Cells (328)
- > a1 (GenericRegMux__parameterized1)
- > b1 (GenericRegMux__parameterized1_1)

Source File Properties ? _ □ X

DSP_48_A1.v

General Properties

Project Summary x Device x DSP_48_A1.v x ? _ □

X0Y4 X1Y4

X0Y3 X1Y3

X0Y2 X1Y2

X0Y1 X1Y1

X0Y0 X1Y0

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing x ? _ □

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (326)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.670 ns	Worst Hold Slack (WHS): 0.273 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 106	Total Number of Endpoints: 106	Total Number of Endpoints: 181

Timing Summary - impl_1 (saved) x Timing Summary - timing_1 x

Note : Linting tool not working yet .