ICPEDIA

PnR Internship

Internship Project

Submitted by: Ahmed Abd-Elmotagly Ahmed

Running synthesis:

```
icpedia@icpedia-virtual-machine:/home/opentools/OpenLane$ ./flow.tcl -design wbqspiflash -tag icpedia_project_1 to synthesis
OpenLane a633b1fd2529851b284d7704c7f45cad5222f031
All rights reserved. (c) 2020-2022 Efabless Corporation and contributors.
Available under the Apache License, version 2.0. See the LICENSE file for more details.

[INFO]: Using design configuration at /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: PDKs root directory: /home/opentools/OpenLane/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/opentools/OpenLane/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library is set to: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: Run Directory: /home/opentools/OpenLane/designs/wbqspiflash/runs/icpedia_project_1
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[STEP 1]
[INFO]: Running Synthesis...
[STEP 2]
[INFO]: Running Single-Corner Static Timing Analysis...
[STEP 3]
[INFO]: Running Initial Floorplanning...
[INFO]: Extracting core dimensions...
[INFO]: Set CORE_WIDTH to 245.18, CORE_HEIGHT to 244.8.
[STEP 4]
[INFO]: Running IO Placement...
[STEP 5]
[INFO]: Running Tap/Decap Insertion...
[INFO]: Power planning with power {VPWR} and ground {VGND}...
[STEP 6]
[INFO]: Generating PDN...
[STEP 7]
[INFO]: Running Global Placement...
[STEP 8]
[INFO]: Running Placement Resizer Design Optimizations...
[STEP 9]
[INFO]: Writing Verilog...
[STEP 10]
[INFO]: Running Detailed Placement...
[STEP 11]
[INFO]: Running Clock Tree Synthesis...
[STEP 12]
[INFO]: Writing Verilog...
[STEP 13]
[INFO]: Running Placement Resizer Timing Optimizations...
[STEP 14]
[INFO]: Writing Verilog...
[INFO]: Routing...
[STEP 15]
[INFO]: Running Global Routing Resizer Timing Optimizations...
[STEP 16]
[INFO]: Writing Verilog...
[STEP 17]
[INFO]: Running Detailed Placement...
[STEP 18]
[INFO]: Running Global Routing...
[INFO]: Starting FastRoute Antenna Repair Iterations...
[STEP 19]
[INFO]: Running Fill Insertion...
[STEP 20]
[INFO]: Writing Verilog...
[STEP 21]
[INFO]: Running Detailed Routing...
[INFO]: No DRC violations after detailed routing.
[STEP 22]
[INFO]: Writing Verilog...
[INFO]: Running parasitics-based static timing analysis...
[STEP 23]
[INFO]: Running SPEF Extraction at the min process corner...
[STEP 24]
[INFO]: Running Multi-Corner Static Timing Analysis at the min process corner...
[STEP 25]
[INFO]: Running SPEF Extraction at the max process corner...
[STEP 26]
[INFO]: Running Multi-Corner Static Timing Analysis at the max process corner...
[STEP 27]
[INFO]: Running SPEF Extraction at the nom process corner...
[STEP 28]
[INFO]: Running Single-Corner Static Timing Analysis at the nom process corner...
[STEP 29]
[INFO]: Running Multi-Corner Static Timing Analysis at the nom process corner...
[STEP 30]
```

```
[STEP 30]
[INFO]: Running Magic to generate various views...
[INFO]: Streaming out GDS-II with Magic...
[INFO]: Generating MAGLEF views...
[STEP 31]
[INFO]: Streaming out GDS-II with Klayout...
[STEP 32]
[INFO]: Running XOR on the layouts using Klayout...
[STEP 33]
[INFO]: Running Magic Spice Export from LEF...
[STEP 34]
[INFO]: Writing Powered Verilog...
[STEP 35]
[INFO]: Writing Verilog...
[STEP 36]
[INFO]: Running LEF LVS...
[STEP 37]
[INFO]: Running Magic DRC...
[INFO]: Converting Magic DRC Violations to Magic Readable Format...
[INFO]: Converting Magic DRC Violations to Klayout XML Database...
[INFO]: No DRC violations after GDS streaming out.
[STEP 38]
[INFO]: Running OpenROAD Antenna Rule Checker...
[INFO]: Saving current set of views in 'designs/wbqspiflash/runs/icpedia_project_1/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/wbqspiflash/runs/icpedia_project_1/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/wbqspiflash/runs/icpedia_project_1/reports/metrics.csv'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/wbqspiflash/runs/icpedia_project_1/reports/signoff/28-rcx_sta.slew.rpt'.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
[INFO]: Note that the following warnings have been generated:
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/wbqspiflash/runs/icpedia_project_1/reports/signoff/28-rcx_sta.slew.rpt'.
```


Synthesis is completed with no errors.

Modifying config.tcl to change the pins order depending on the given file:

The file "pins_order.cfg" based on the required order:

Open

pins_order.cfg
/home/opentools/OpenLane/designs/wbqspiflash

pin_order.cfg | pins_order.cfg | wbqspiflash.v | floorplan.tcl | config.tcl

```
1 #N
2 o_wb_ack
3 o_wb_stall
4 o_qspi_sck
5 o_qspi_cs_n
6 o_qspi_mod.*
7 o_qspi_dat
8 o_interrupt
9
10 #S
11 o_wb_data\[\d{2}\]
12
13 #E
14 i_clk
15 i_wb_cyc
16 i_wb_data_stb
17 i_wb_ctrl_stb
18 i_wb_we
19 i_wb_addr.*
20 i_qspi_dat.*
21
22
23 #W
24 i_wb_data\[\d{2}\]
```

Changing the thickness to x1

```
39 set ::env(FP_IO_VTHICKNESS_MULT) 1
40 set ::env(FP_IO_HTHICKNESS_MULT) 1
```

Changing length to 2 um

```
35 set ::env(FP_IO_HLENGTH) 2
36 set ::env(FP_IO_VLENGTH) 2
```

Editing the power structure to have metal straps in met2 to met5:

```
44 set ::env(FP_PDN_LOWER_LAYER) met2
45 set ::env(FP_PDN_UPPER_LAYER) met5
```

Changing the required values

```
21 set ::env(FP_PDN_VOFFSET) 5.32
22 set ::env(FP_PDN_VPITCH) 30.94
23 set ::env(FP_PDN_HOFFSET) 5.65
24 set ::env(FP_PDN_HPITCH) 30.80
25
```

Running floorplan

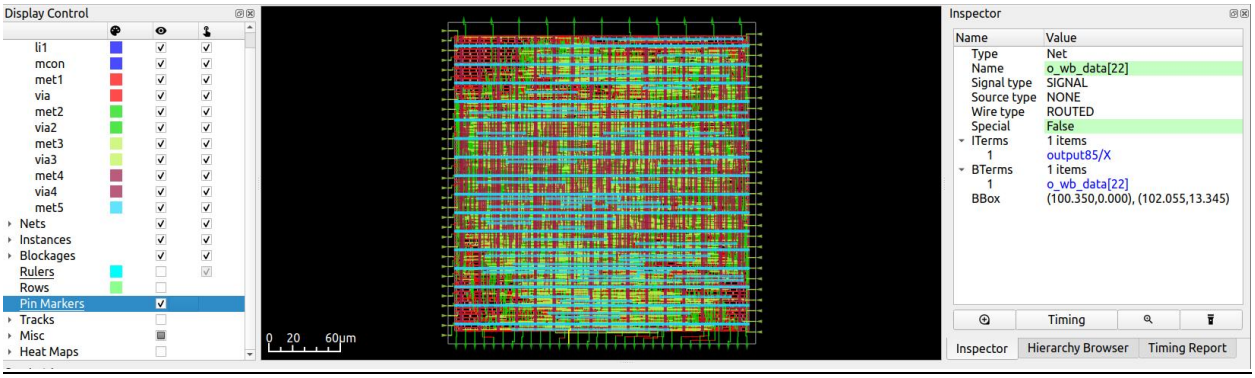
```
icpedia-virtual-machine:/home/opentools/OpenLane$ ./flow.tcl -design wbqspiflash -tag icpedia_project_1____ to floorplan
e a633b1fd2529851b284d7704c7f45cad5222f031
ts reserved. (c) 2020-2022 Efabless Corporation and contributors.
e under the Apache License, version 2.0. See the LICENSE file for more details.

Using design configuration at /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
PDKs root directory: /home/opentools/OpenLane/pdks
PDK: sky130A
Setting PDKPATH to /home/opentools/OpenLane/pdks/sky130A
Standard Cell Library: sky130_fd_sc_hd
Optimization Standard Cell Library is set to: sky130_fd_sc_hd
Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
Run Directory: /home/opentools/OpenLane/designs/wbqspiflash/runs/icpedia_project_1____
Preparing LEF files for the nom corner...
Preparing LEF files for the min corner...
Preparing LEF files for the max corner...
]
Running Synthesis...
]
Running Single-Corner Static Timing Analysis...
]
Running Initial Floorplanning...
Extracting core dimensions...
Set CORE_WIDTH to 245.18, CORE_HEIGHT to 244.8.
]
Running IO Placement...

Running Tap/Decap Insertion...
Power planning with power {VPWR} and ground {VGND}...
]
Generating PDN...
]
Running Global Placement...
]
Running Placement Resizer Design Optimizations...
]
Writing Verilog...
]
Running Detailed Placement...
]
Running Clock Tree Synthesis...
]
```

.

.

```
icpedia@icpedia-virtual-machine: /home/opentools/OpenLane
Running SPEF Extraction at the max process corner...
]
Running Multi-Corner Static Timing Analysis at the max process corner...
]
Running SPEF Extraction at the nom process corner...
]
Running Single-Corner Static Timing Analysis at the nom process corner...
]
Running Multi-Corner Static Timing Analysis at the nom process corner...
]
Running Magic to generate various views...
Streaming out GDS-II with Magic...
Generating MAGLEF views...
]
Streaming out GDS-II with Klayout...
]
Running XOR on the layouts using Klayout...
]
Running Magic Spice Export from LEF...
]
Writing Powered Verilog...
]
Writing Verilog...
]
Running LEF LVS...
]
Running Magic DRC...
Converting Magic DRC Violations to Magic Readable Format...
Converting Magic DRC Violations to Klayout XML Database...
No DRC violations after GDS streaming out.
]
Running OpenROAD Antenna Rule Checker...
Saving current set of views in 'designs/wbqspiflash/runs/icpedia_project_1____/results/final'...
Saving runtime environment...
Generating final set of reports...
Created manufacturability report at 'designs/wbqspiflash/runs/icpedia_project_1____/reports/manufacturability.rpt'.
Created metrics report at 'designs/wbqspiflash/runs/icpedia_project_1____/reports/metrics.csv'.
]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/wbqspiflash/runs/icpedia_project_1____/reports/signoff/28-rcx_sta.slew.rpt'.
There are no hold violations in the design at the typical corner.
There are no setup violations in the design at the typical corner.
]: Flow complete.
Note that the following warnings have been generated:
]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/wbqspiflash/runs/icpedia_project_1____/reports/signoff/28-rcx_sta.slew.rpt'.
```

Checking the floorplan in interactive:



The required pin order is achieved.

Initial die area and core area:

```
56 [INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
57 [INFO] Floorplanned on a die area of 0.0 0.0 256.315 267.035 (microns). Saving to /home/opentools/OpenLane/designs/wbqspiflash/runs/icpedia_project_1____/reports/floorplan/3-
   initial_fp_die_area.rpt.
58 [INFO] Floorplanned on a core area of 5.52 10.88 250.7 255.68 (microns). Saving to /home/opentools/OpenLane/designs/wbqspiflash/runs/icpedia_project_1____/reports/floorplan/3-
   initial_fp_core_area.rpt.
```



```
1157 ===========================================================================
1158  report_design_area
1159 ===========================================================================
1160 Design area 28261 u^2 47% utilization.
1161 area_report_end
```

Clock period:

```
21 ###############################################################################
22 # Timing Constraints
23 ###############################################################################
24 create_clock -name i_clk -period 20.0000 [get_ports {i_clk}]
```

Changing clock period to 15 and using time driven placement

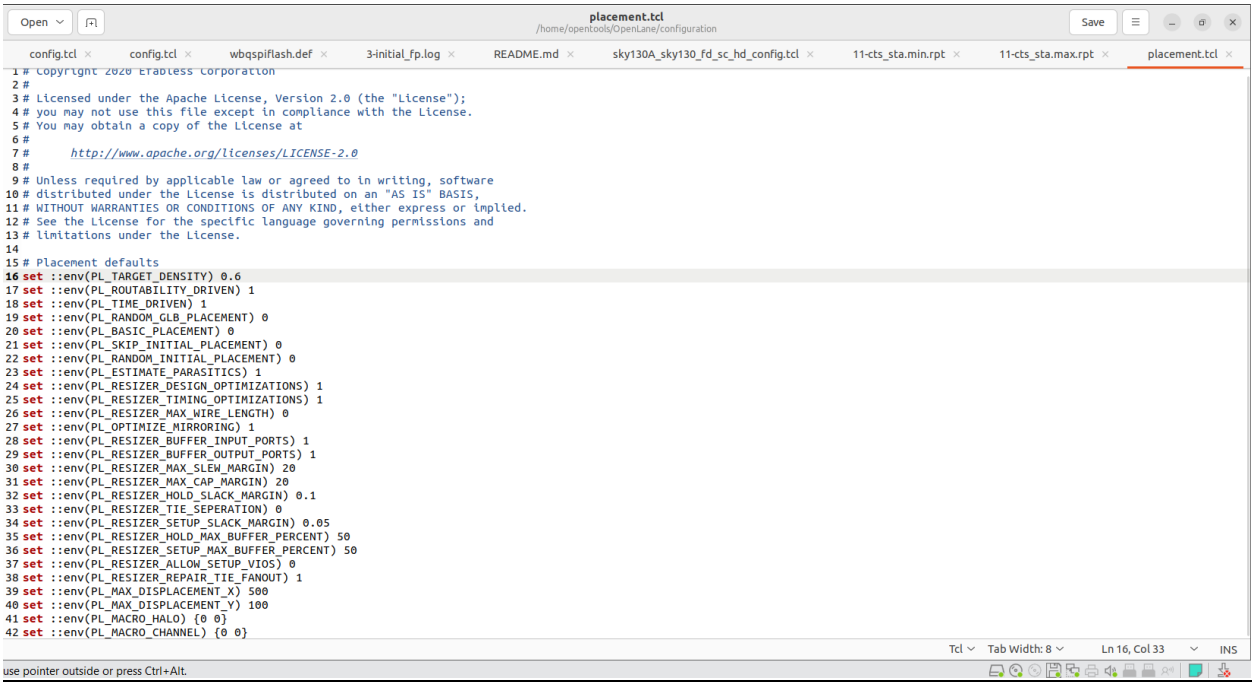
Open

sky130A_sky130_fd_sc_hd_config.tcl
/home/opentools/OpenLane/designs/wbqspiflash

config.tcl | config.tcl | wbqspiflash.def | 3-initial_fp.log | README.md | sky130A_sky130_fd_sc_hd_config.tcl

```
1 # SCL Configs
2 set ::env(CLOCK_PERIOD) "15"
3 set ::env(SYNTH_STRATEGY) "DELAY 0"
4 set ::env(SYNTH_MAX_FANOUT) 4
5 set ::env(FP_CORE_UTIL) 40
6 set ::env(PL_TARGET_DENSITY) [ expr ($::env(FP_CORE_UTIL)+5) / 100.0 ]
7 set ::env(PL_TIME_DRIVEN) 1
```

Changing target density to 0.6



Enabling fill insertion:

Running to cts:

```
icpedia@icpedia-virtual-machine:/home/opentools/OpenLane$ ./flow.tcl -design wbqspiflash -tag icpedia_project_2 -to cts
OpenLane a633b1fd2529851b284d7704c7f45cad5222f031
All rights reserved. (c) 2020-2022 Efabless Corporation and contributors.
Available under the Apache License, version 2.0. See the LICENSE file for more details.

[INFO]: Using design configuration at /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: PDKs root directory: /home/opentools/OpenLane/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/opentools/OpenLane/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library is set to: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: Run Directory: /home/opentools/OpenLane/designs/wbqspiflash/runs/icpedia_project_2
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[STEP 1]
[INFO]: Running Synthesis...
[STEP 2]
[INFO]: Running Single-Corner Static Timing Analysis...
[STEP 3]
[INFO]: Running Initial Floorplanning...
[INFO]: Extracting core dimensions...
[INFO]: Set CORE_WIDTH to 245.18, CORE_HEIGHT to 244.8.
[STEP 4]
[INFO]: Running IO Placement...
[STEP 5]
[INFO]: Running Tap/Decap Insertion...
[INFO]: Power planning with power {VPWR} and ground {VGND}...
[STEP 6]
[INFO]: Generating PDN...
[STEP 7]
[INFO]: Running Global Placement...
[STEP 8]
[INFO]: Running Placement Resizer Design Optimizations...
[STEP 9]
[INFO]: Writing Verilog...
[STEP 10]
[INFO]: Running Detailed Placement...
[STEP 11]
[INFO]: Running Clock Tree Synthesis...
[STEP 12]
[INFO]: Writing Verilog...
[STEP 13]
[INFO]: Running Placement Resizer Timing Optimizations...
[STEP 14]
[INFO]: Writing Verilog...
[INFO]: Saving current set of views in 'designs/wbqspiflash/runs/icpedia_project_2/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/wbqspiflash/runs/icpedia_project_2/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/wbqspiflash/runs/icpedia_project_2/reports/metrics.csv'.
[INFO]: There are no max slew, max fanout or max capacitance violations in the design at the typical corner.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
```

- ➔ Reduced the area clock frequency with no violations.
- ➔ Next table illustrates differences between the two configurations:

	1st config	**2nd config**
Core Area	245.7*245.68	245.18 * 244.8
Clock period	20 ns	15 ns
Placement target density	0.55	0.6
Die Area	256.315 * 267.035	256.315 * 267.035

Setting : DRT_OPT_ITERS to 64

```
40
41 set ::env(DRT_OPT_ITERS) 64
42
```

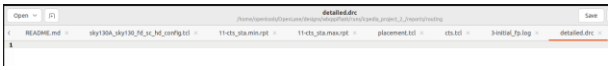
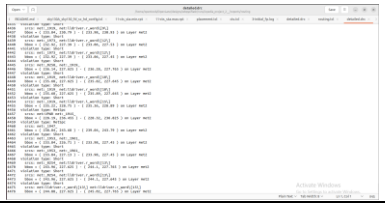
Running to routing:

```
icpedia@icpedia-virtual-machine:/home/opentools/OpenLane$ ./flow.tcl -design wbqspiflash -tag icpedia_project_2_ -to routing
OpenLane a633b1fd2529851b284d7704c7f45cad5222f031
All rights reserved. (c) 2020-2022 Efabless Corporation and contributors.
Available under the Apache License, version 2.0. See the LICENSE file for more details.

[INFO]: Using design configuration at /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: PDKs root directory: /home/opentools/OpenLane/pdks
[INFO]: PDK: sky130A
[INFO]: Setting PDKPATH to /home/opentools/OpenLane/pdks/sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library is set to: sky130_fd_sc_hd
[INFO]: Sourcing Configurations from /home/opentools/OpenLane/designs/wbqspiflash/config.tcl
[INFO]: Run Directory: /home/opentools/OpenLane/designs/wbqspiflash/runs/icpedia_project_2_
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[STEP 1]
[INFO]: Running Synthesis...
[STEP 2]
[INFO]: Running Single-Corner Static Timing Analysis...
[STEP 3]
[INFO]: Running Initial Floorplanning...
[INFO]: Extracting core dimensions...
[INFO]: Set CORE_WIDTH to 245.18, CORE_HEIGHT to 244.8.
[STEP 4]
[INFO]: Running IO Placement...
[STEP 5]
[INFO]: Running Tap/Decap Insertion...
[INFO]: Power planning with power {VPWR} and ground {VGND}...
[STEP 6]
[INFO]: Generating PDN...
[STEP 7]
[INFO]: Running Global Placement...
[STEP 8]
[INFO]: Running Placement Resizer Design Optimizations...
[STEP 9]
[INFO]: Writing Verilog...
[STEP 10]
[INFO]: Running Detailed Placement...
[STEP 11]
[INFO]: Running Clock Tree Synthesis...
[STEP 11]
[INFO]: Running Clock Tree Synthesis...
[STEP 12]
[INFO]: Writing Verilog...
[STEP 13]
[INFO]: Running Placement Resizer Timing Optimizations...
[STEP 14]
[INFO]: Writing Verilog...
[INFO]: Routing...
[STEP 15]
[INFO]: Running Global Routing Resizer Timing Optimizations...
[STEP 16]
[INFO]: Writing Verilog...
[STEP 17]
[INFO]: Running Detailed Placement...
[STEP 18]
[INFO]: Running Global Routing...
[INFO]: Starting FastRoute Antenna Repair Iterations...
[STEP 19]
[INFO]: Running Fill Insertion...
[STEP 20]
[INFO]: Writing Verilog...
[STEP 21]
[INFO]: Running Detailed Routing...
[INFO]: No DRC violations after detailed routing.
[STEP 22]
[INFO]: Writing Verilog...
[INFO]: Saving current set of views in 'designs/wbqspiflash/runs/icpedia_project_2_/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/wbqspiflash/runs/icpedia_project_2_/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/wbqspiflash/runs/icpedia_project_2_/reports/metrics.csv'.
[INFO]: There are no max slew, max fanout or max capacitance violations in the design at the typical corner.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
icpedia@icpedia-virtual-machine:/home/opentools/OpenLane$
```

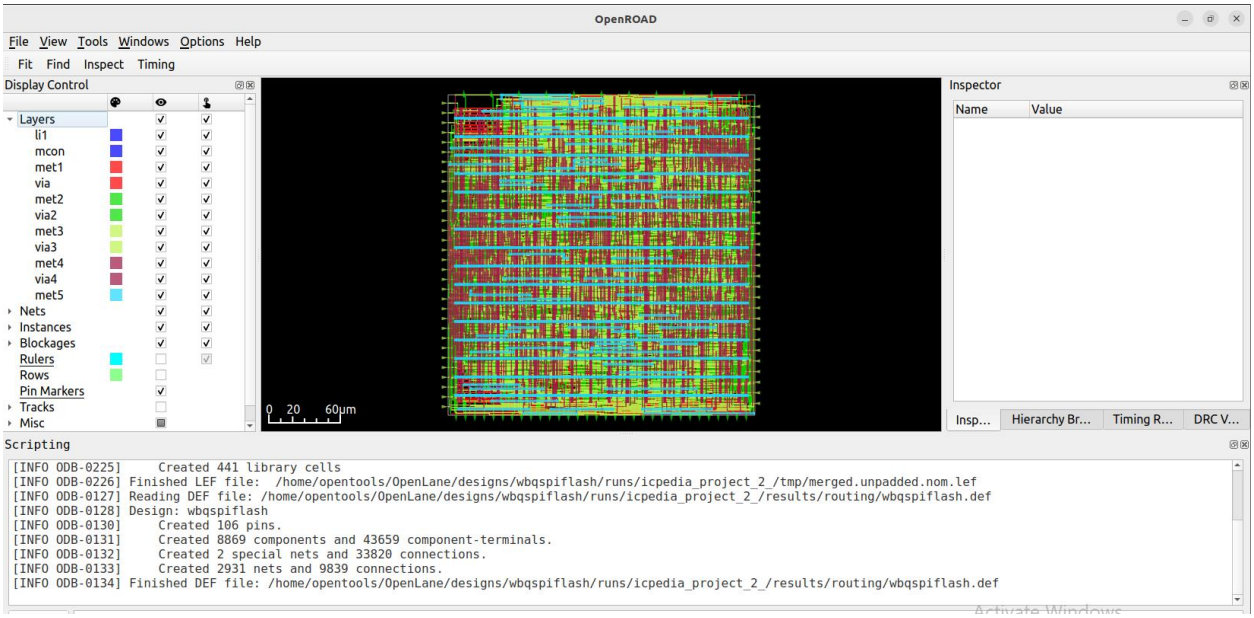
Setting: DRT_OPT_ITERS to 1

```
icpedia@icpedia-virtual-machine: /home/opentools/OpenLane
[INFO]: Running Detailed Placement...
[STEP 18]
[INFO]: Running Global Routing...
[INFO]: Starting FastRoute Antenna Repair Iterations...
[STEP 19]
[INFO]: Running Fill Insertion...
[STEP 20]
[INFO]: Writing Verilog...
[STEP 21]
[INFO]: Running Detailed Routing...
[ERROR]: There are violations in the design after detailed routing.
[ERROR]: Total Number of violations is 1492
[INFO]: Saving current set of views in 'designs/wbqspiflash/runs/icpedia_project_2__/results/final'...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/wbqspiflash/runs/icpedia_project_2__/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/wbqspiflash/runs/icpedia_project_2__/reports/metrics.csv'.
[INFO]: Saving runtime environment...
[ERROR]: Flow failed.

    while executing
"flow_fail"
    (procedure "quit_on_tr_drc" line 8)
    invoked from within
"quit_on_tr_drc"
    (procedure "detailed_routing_tritonroute" line 10)
    invoked from within
"detailed_routing_tritonroute"
    (procedure "detailed_routing" line 14)
    invoked from within
"detailed_routing"
    (procedure "run_routing" line 52)
    invoked from within
"run_routing"
    (procedure "run_routing_step" line 8)
    invoked from within
"[lindex $step_exe 0] [lindex $step_exe 1] "
    (procedure "run_non_interactive_mode" line 56)
    invoked from within
"run_non_interactive_mode {*}$argv"
    invoked from within
"if { [info exists flags_map(-interactive)] || [info exists flags_map(-it)] } {
    if { [info exists arg_values(-file)] } {
        run_file [file nor..."
    (file "./flow.tcl" line 388)
icpedia@icpedia-virtual-machine:/home/opentools/OpenLane$
```

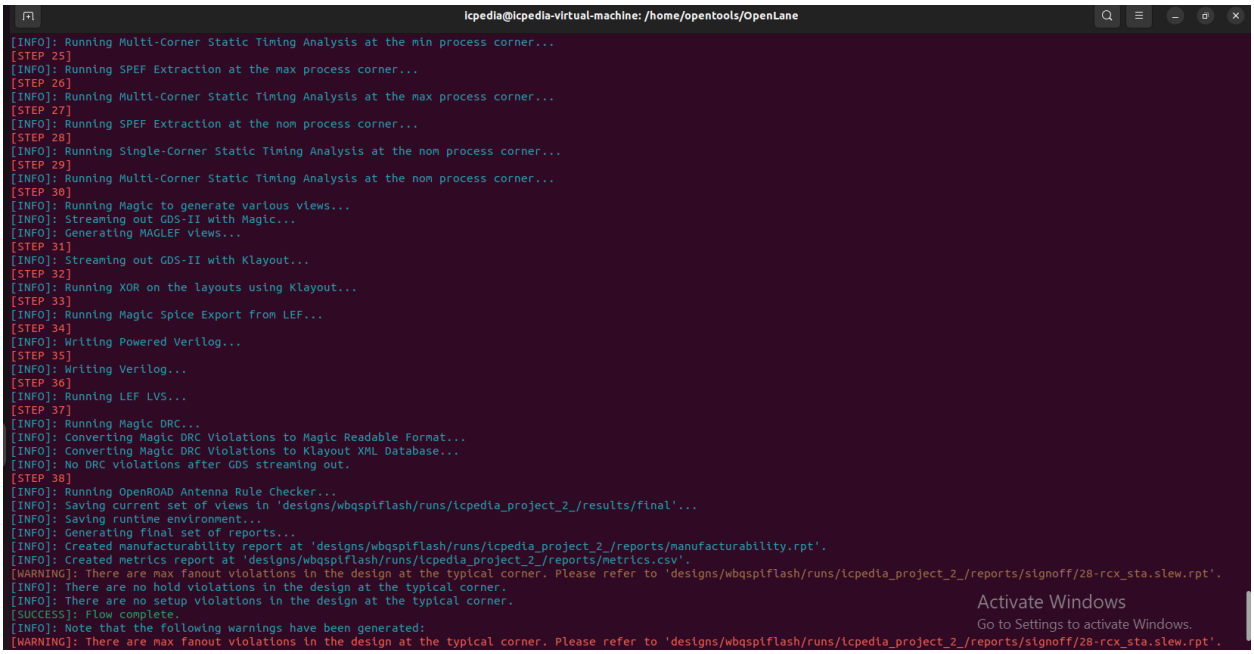
Violations appeared.

64 iterations	1 iteration
No DRCs 	1492 DRCs 
5~10 mins	3~5 mins

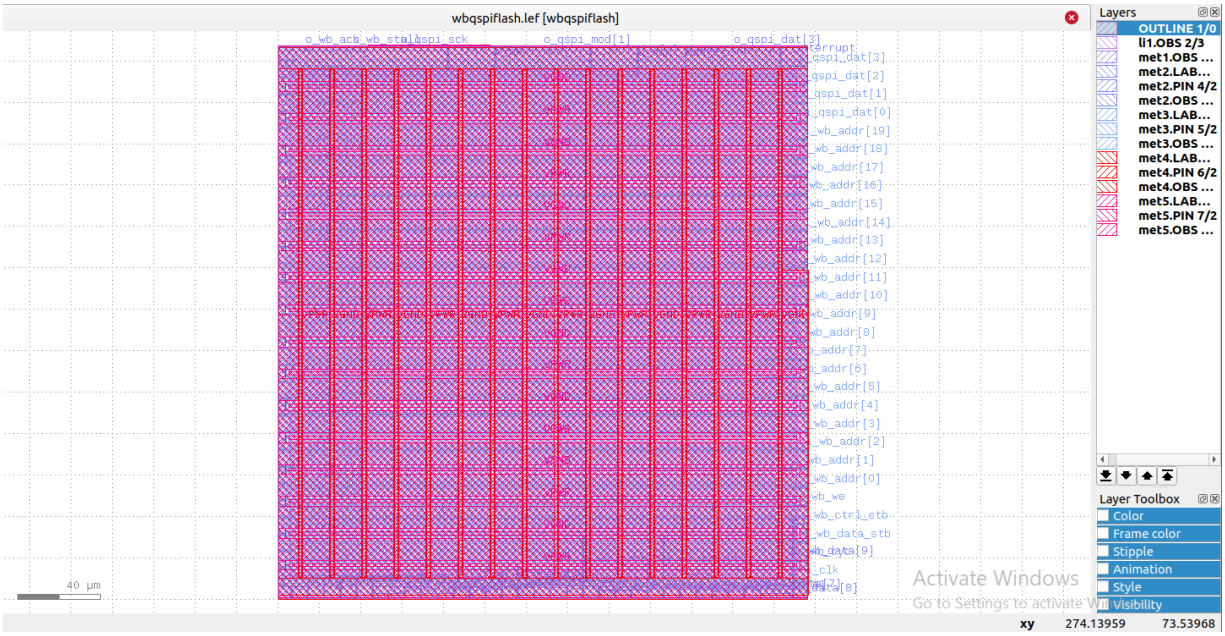
➔ Iterations is set to 64 to continue without DRCs.



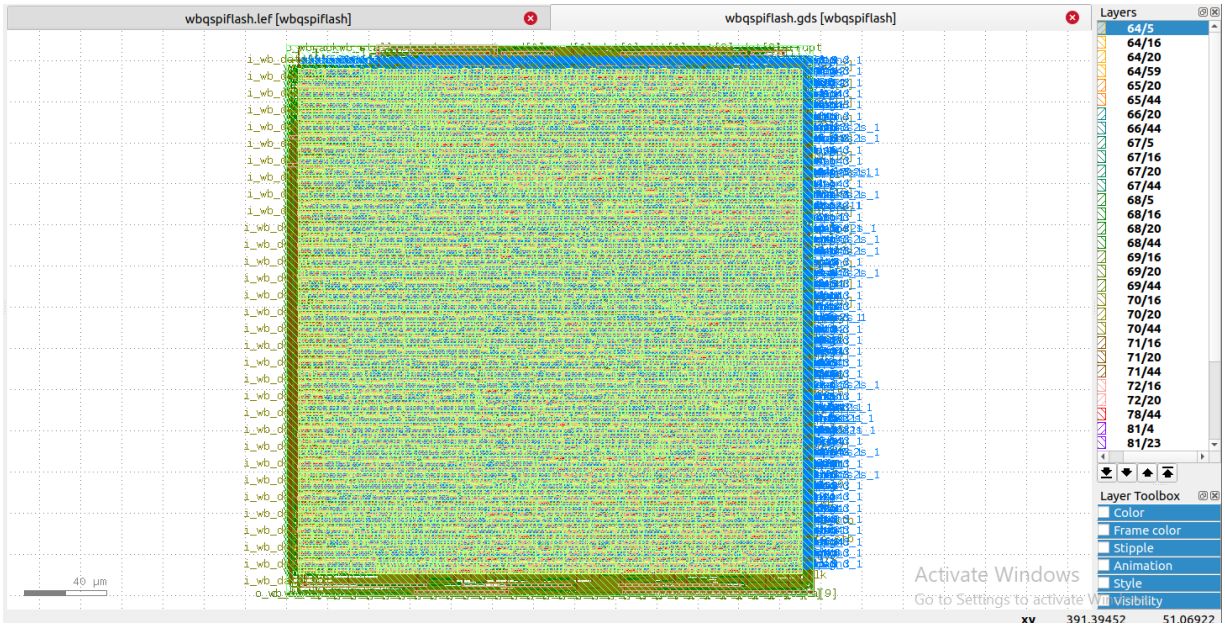
Continue the flow.tcl



The final .lef file in klayout:



The final .gds file in klayout:

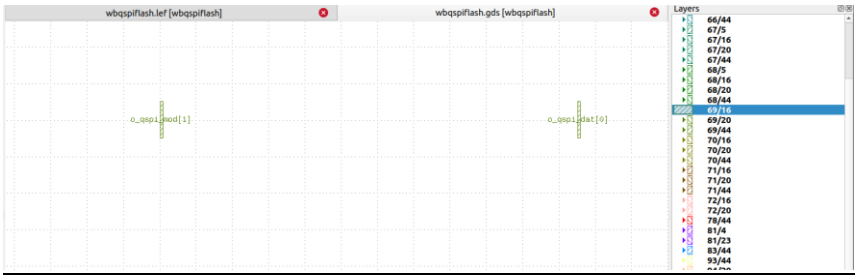


.lef and .gds are two different file formats used for representing layouts.

- ➔ .lef: includes details such as the cell dimensions, pin locations, layer information, and other properties.
- ➔ .gds: geometric data of layout. the actual shapes and layers that make up the layout, commonly used for manufacturing purposes, as they provide a precise representation of the layout that can be used by fabrication facilities.

Pins in Klayout:

o/p pins on metal 2



i/p pins on metal 3

Metal 2 → 69

Metal 3 → 70

```
334
335 layer  MET2 MET2,MET2T,MET2P,VIA1
336 calma 69 20
337
338 layer  MET2T
339 labels MET2T noport
340 calma 69 16
341
342 layer  MET2P
343 labels MET2P port
344 calma 69 5
345
346 layer  VIA1 VIA1
347 labels VIA1
348 calma 68 44
349
350 layer  RERAM RERAM
351 labels RERAM
352 calma 201 20
353
354 layer  MET3 MET3,MET3T,MET3P,VIA2
355 calma 70 20
356
357 layer  MET3T
358 labels MET3T noport
359 calma 70 16
360
361 layer  MET3P
362 labels MET3P port
363 calma 70 5
```

Iteration #	Changed Parameters	Clock period	Core area	Die Area	DRCs
1	No. of iterations = 1 Placement Target density = 0.55	20	245.7*245.68	256.315 * 267.035	1492
2	No. of iterations = 64 Placement Target density = 0.6 Enabled fill insertion Using time driven placement	15	245.18*244.8	256.315 * 267.035	0
3	Cts tolerance = 50 Cts skew = 100 Core util = 50 Fill insertion = 0 GLB_RT_MAX_DIODE_INS_ITERS= 5 Placement Target density = 0.5	5	218.96 * 217.6		

Could not solve the over-congestion error in detailed routing , probably the solution is in increasing halos and unused area surrounding blocks.