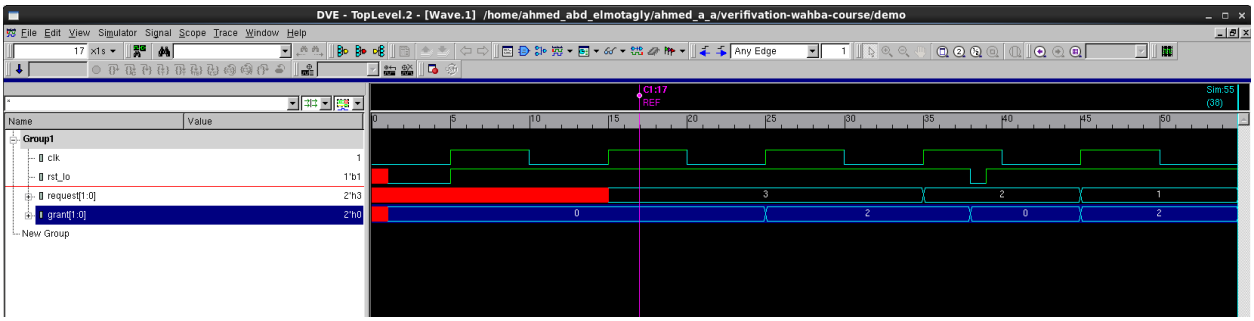
VCS Simulation results for bus arbiter testbench without using system Verilog interface



Race condition occurred at time 15 where the request changed just at the edge of clock and did not got captured resulting in a delay in the grant signal

This shows the importance of STA analysis and setup/hold timing requirements