Applying verification concepts on a D FF

Verification plan for a positive edge triggered D flip flop with active low reset

Verify		Check that	Test case
1.	Normal operation	@ posedge of clock the data is transferred to output and the inverted output is correct. Output is only updated at posedge of clock	D = 1 #1 D=0 #2 D=1
2.	Reset	When reset=0 the output is zero	Rst=0 #3 Rst=1

Testbench simulation with Synopsys VCS tool