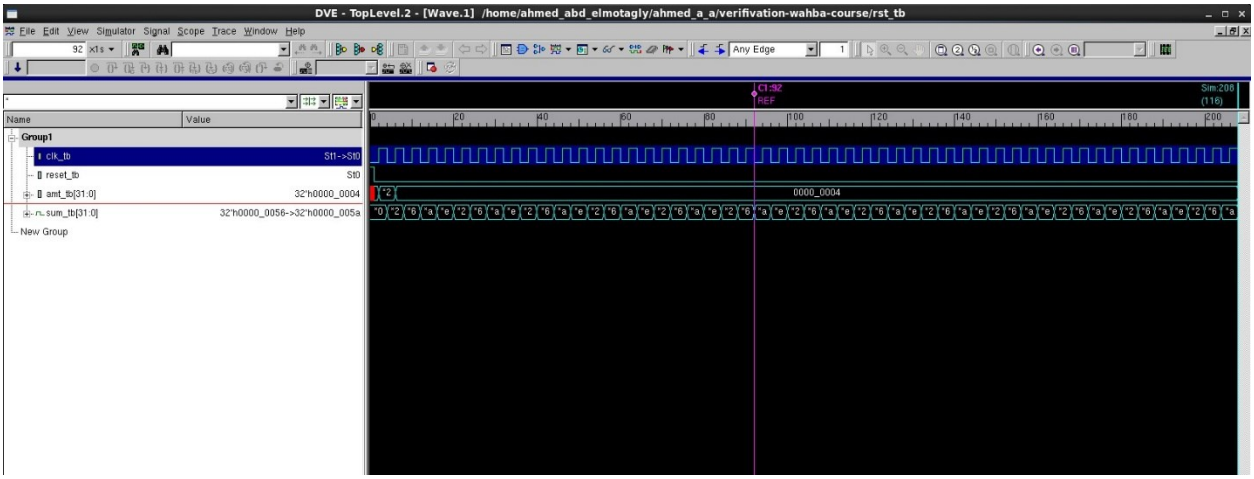
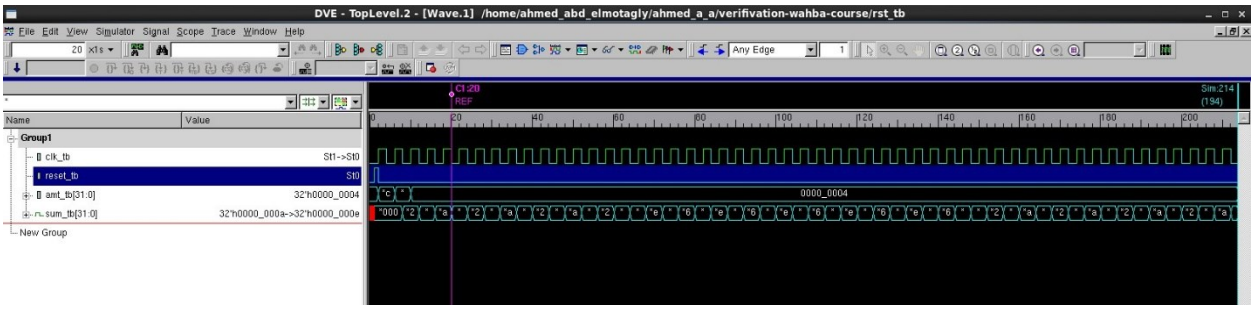
Accumulator verification plan

Verification plan for an asynchronous reset accumulator design

Features		Checkers list	Stimulus	Priority
1.	Reset	- @posedge reset Sum=0 - @negedge reset sum=0 i.e. till next posedge clk - While reset = 1 -> sum=0 - While reset=0 -> sum counting	- Reset = 0 → 1	- High - High - Medium - Low
2.	Clock sensitivity	Sum updated @negedge clk Addition occurs @posedge clk	- Change amt before negedge	- High
3.	Accumulation	Correct sum result	- Apply different inputs	- High

Simulation with VCS and results viewed in Synopsys DVE






```
Simulation complete, time is 208.
           V C S   S i m u l a t i o n   R e p o r t
Time: 208
CPU Time:      3.280 seconds;       Data structure size:   0.0Mb
Fri Apr 29 03:22:28 2016
```