Zagazig University
Faculty of Engineering
ECE Department
Second Year (2024-2025)

Digital Logic Design
Data Stream Analyser
Project Report

DIGITAL LOGIC DESIGN

Data Stream Analyser

Project Report

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1. The Assignment Aim

The aim of this project is to design and implement a sequence detector circuit that identifies specific 4-bit binary input sequences and performs corresponding actions based on each detected sequence. The circuit will be capable of detecting the following four input sequences:

1111 – activates a fan

1010 – turns on a Flashing LED

0110 – triggers a buzzer alarm

0000 – starts a counter

The primary goal is to demonstrate the application of combinational and sequential logic in building a reliable digital system that interprets specific binary messages and responds with the correct control signals. This project emphasizes the use of finite state machines, logic gates, flip-flops, and output interface control to build a fully functional sequence detection system.

2. The Solution Steps

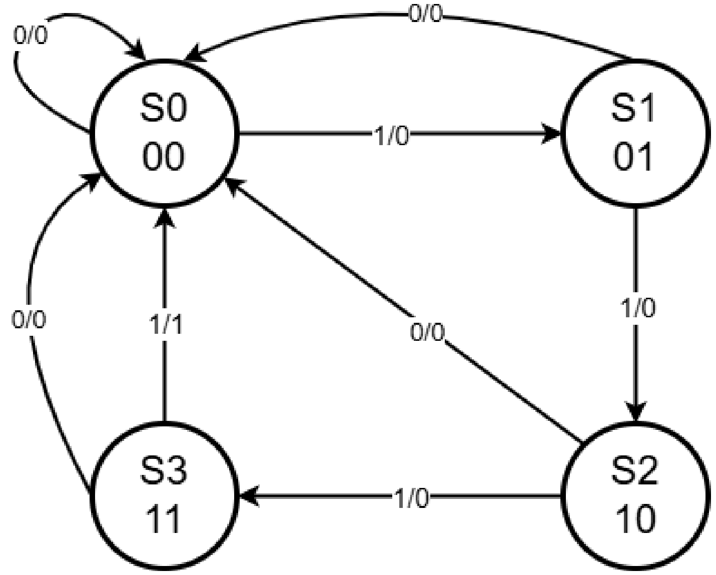
2.1 Code 1111 Circuit

2.1.1. Defining the inputs and outputs and the State Diagram

The input is the data stream “X” (to be analyzed) and the output signal “Y” that corresponds to the occurrence of the code 1111.

Since it’s a 4-bit message then 2 flip flops is needed to have 4 states.

From this information we can deduce the State Diagram:



2.1.2. State Table, State Equations and K-Maps

Then the state table is constructed based on the state diagram:

Present State		Inputs	Next State		Output
A	B	X	A^+	B^+	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	1

A\BX	$\bar{B}$		B	
$\bar{A}$	0	0	1	0
A	0	1	0	0
For A^+	$\bar{X}$	X		$\bar{X}$

$$A^+ = \bar{A}BX + A\bar{B}X = (A \oplus B)X$$

A\BX	$\bar{B}$		B	
$\bar{A}$	0	1	0	0
A	0	1	0	0
For B^+	$\bar{X}$	X		$\bar{X}$

$$B^+ = \bar{B}X$$

$$Y = ABX$$

2.1.3. Designing the Logic Circuit

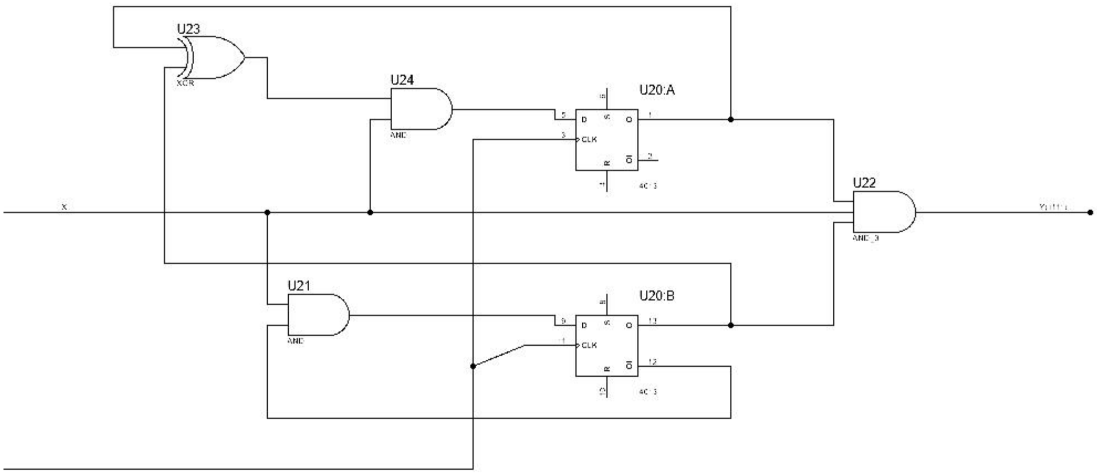
Using D-Flip Flop with the State equations:

$$D_A = A^+ = \bar{A}BX + A\bar{B}X = (A \oplus B)X$$

$$D_B = B^+ = \bar{B}X$$

$$Y = ABX$$

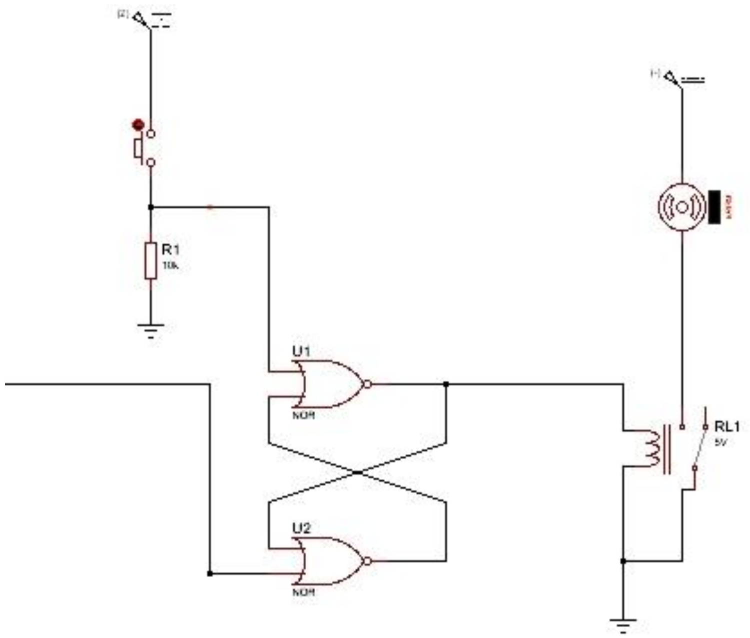
So the Final Circuit would be :



2.1.4. Fan Circuit

Since the Fan Circuit requires higher voltage than low digital signal, we’ll use the digital signal to control a relay which controls the Fan.

And since the output is an instantaneous pulse, we’ll use an SR latch to make it a constant voltage state with a stop button to reset the latch (this method is used throughout the project).



Fan Circuit

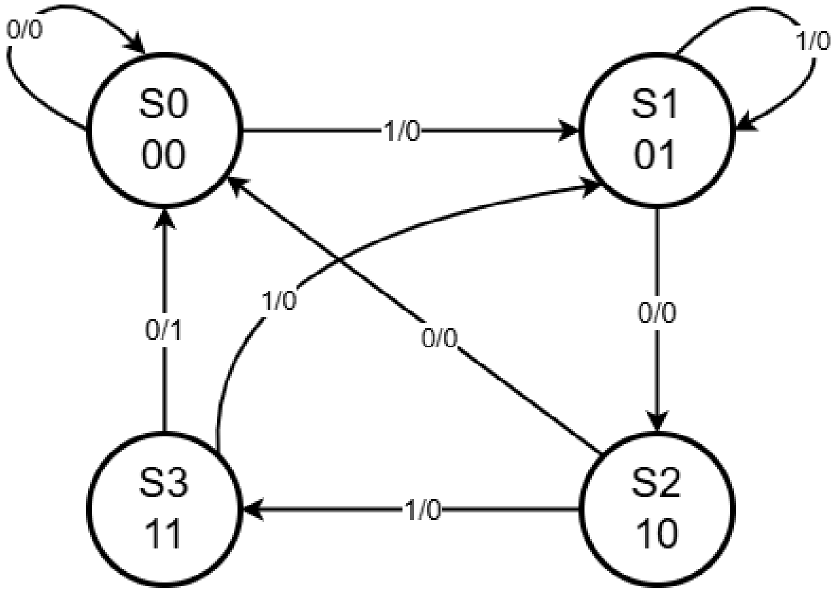
2.2 Code 1010 Circuit

2.2.1. Defining the inputs and outputs and the State Diagram

The input is the data stream “X” (to be analyzed) and the output signal “Y” that corresponds to the occurrence of the code 1010.

Since it’s a 4-bit message then 2 flip flops is needed to have 4 states.

From this information we can deduce the State Diagram:



2.2.2. State Table, State Equations and K-Maps

Then the state table is constructed based on the state diagram:

Present State		Inputs	Next State		Output
A	B	X	A$^+$	B$^+$	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	0	1	0

A\BX	$\bar{B}$		B	
$\bar{A}$	0	0	0	$\boxed{1}$
A	0	$\boxed{1}$	0	0
For A$^+$	$\bar{X}$	X		$\bar{X}$

$$A^+ = \bar{A}B\bar{X} + A\bar{B}X$$

A\BX	$\bar{B}$		B	
$\bar{A}$	0	1	1	0
A	0	1	1	0
For B$^+$	$\bar{X}$	X		$\bar{X}$

$$B^+ = X$$

$$Y = AB\bar{X}$$

2.2.3. Designing the Logic Circuit

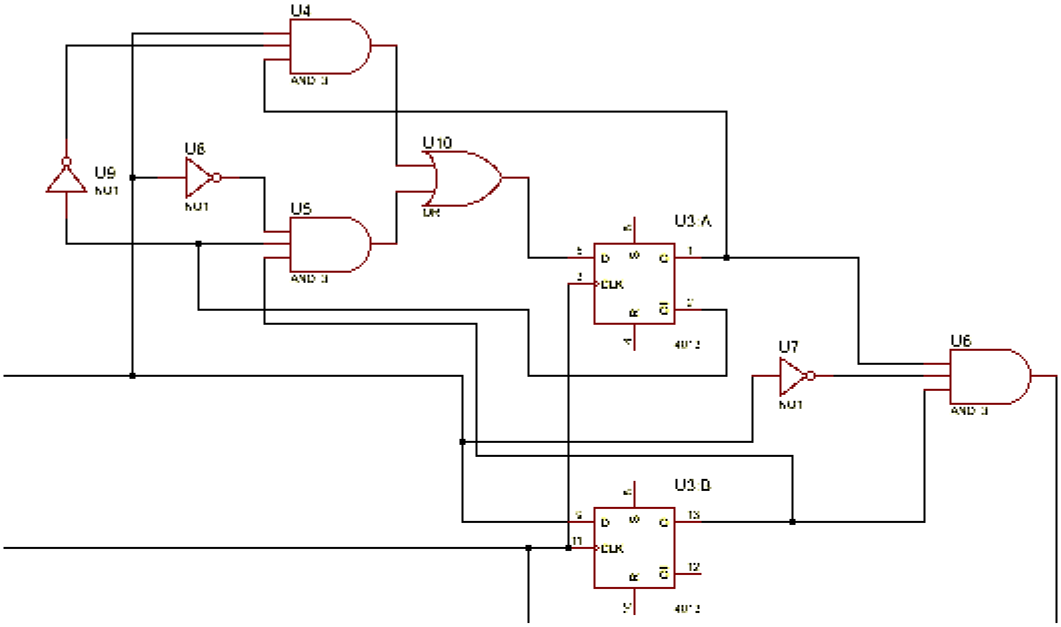
Using D-Flip Flop with the State equations:

$D_A = A^+ = \bar{A}B\bar{X} + A\bar{B}X$

$D_B = B^+ = X$

$Y = AB\bar{X}$

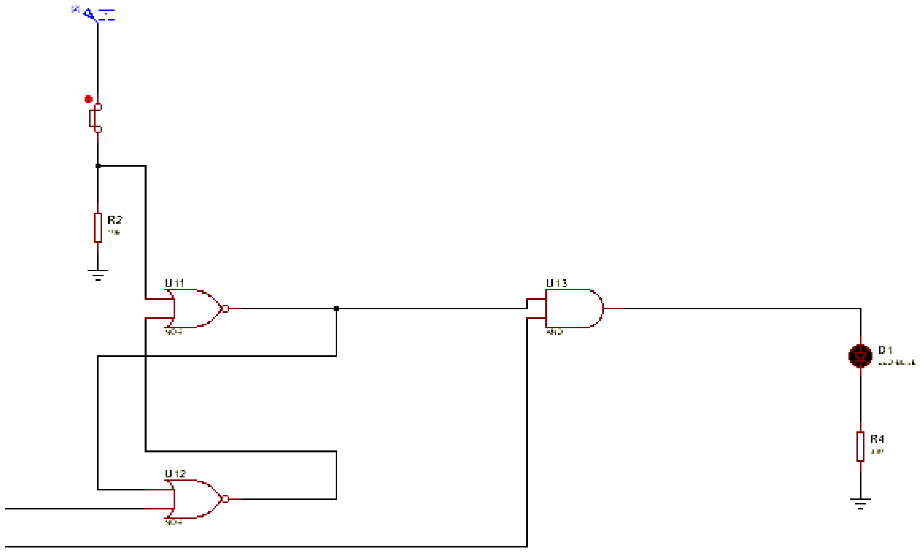
So the Final Circuit would be :



2.2.4. Flashing light Circuit

Since the output is an instantaneous pulse, we'll use an SR latch to make it a constant voltage state with a stop button to reset the latch (this method is used throughout the project).

To make the LED flash we'll connect it to the clock signal AND-ed with the control signal.



Flashing light Circuit

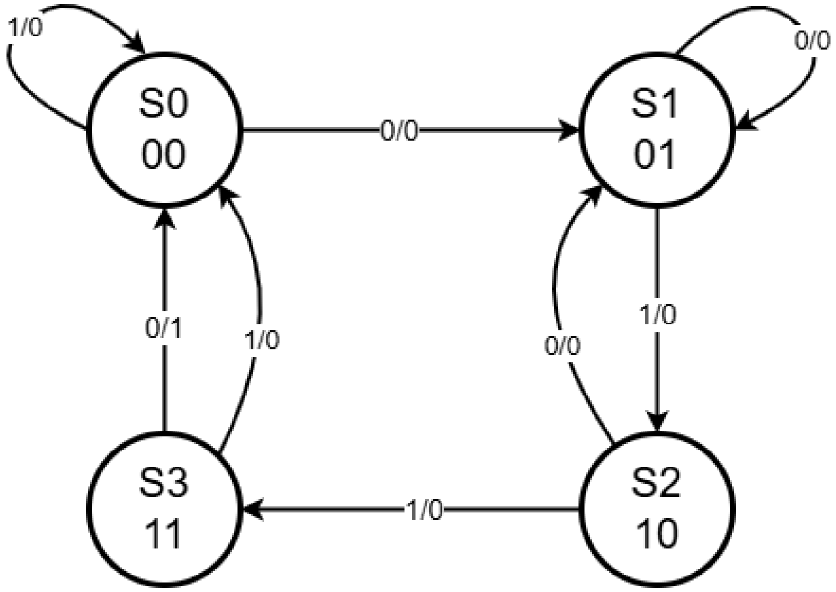
2.3 Code 0110 Circuit

2.3.1. Defining the inputs and outputs and the State Diagram

The input is the data stream “X” (to be analyzed) and the output signal “Y” that corresponds to the occurrence of the code 0110.

Since it’s a 4-bit message then 2 flip flops is needed to have 4 states.

From this information we can deduce the State Diagram:



2.3.2. State Table, State Equations and K-Maps

Then the state table is constructed based on the state diagram:

Present State		Inputs	Next State		Output
A	B	X	A^+	B^+	Y
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	0	0	0

A\BX	$\bar{B}$		B	
$\bar{A}$	0	0	1	0
A	0	1	0	0
For A^+	$\bar{X}$	X		$\bar{X}$

$$A^+ = \bar{A}BX + A\bar{B}X = (A \oplus B)X$$

A\BX	$\bar{B}$		B	
$\bar{A}$	1	0	0	1
A	1	1	0	0
For B^+	$\bar{X}$	X		$\bar{X}$

$$B^+ = A\bar{B} + \bar{A}\bar{X}$$

$$Y = AB\bar{X}$$

2.3.3. Designing the Logic Circuit

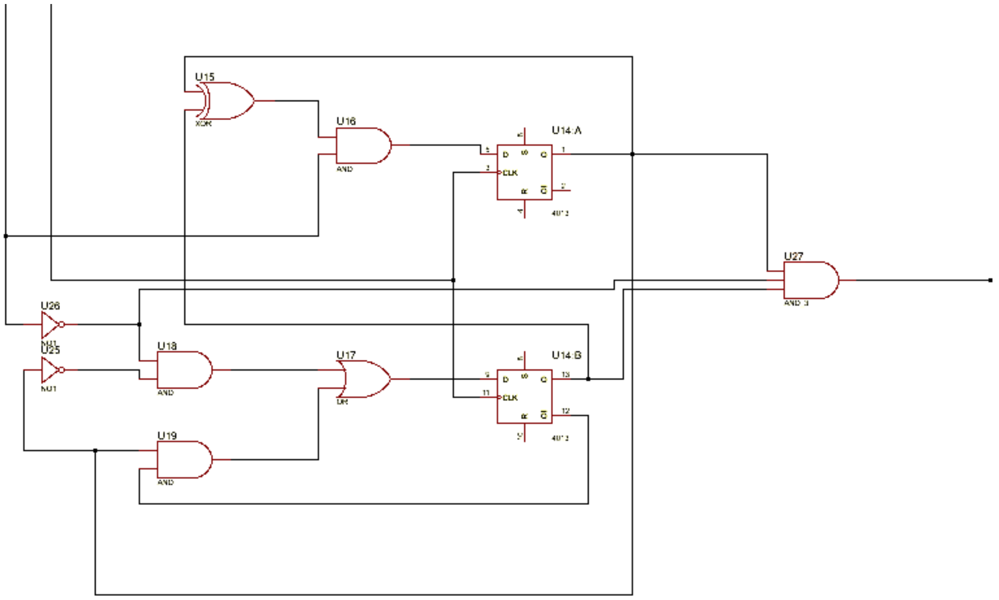
Using D-Flip Flop with the State equations:

$$D_A = A^+ = \bar{A}BX + A\bar{B}X = (A \oplus B)X$$

$$D_B = B^+ = A\bar{B} + \bar{A}\bar{X}$$

$$Y = AB\bar{X}$$

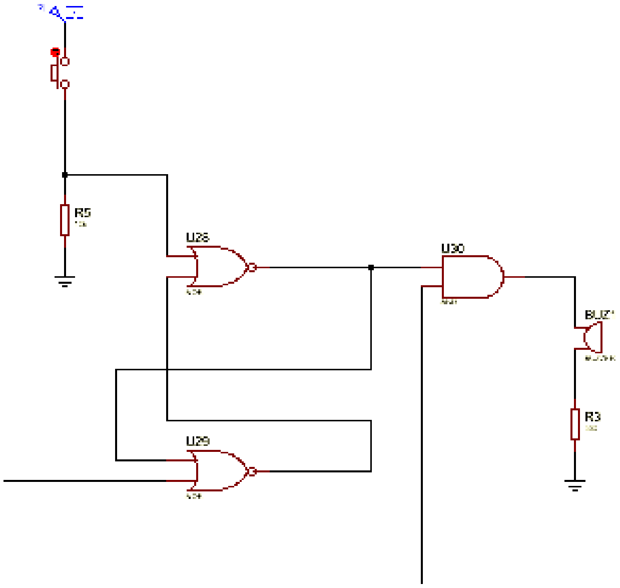
So the Final Circuit would be :



2.3.4. Buzzer Alarm Circuit

Since the output is an instantaneous pulse, we'll use an SR latch to make it a constant voltage state with a stop button to reset the latch (this method is used throughout the project).

To Trigger the Buzzer we'll connect it to the clock signal AND-ed with the control signal.



Buzzer Alarm Circuit

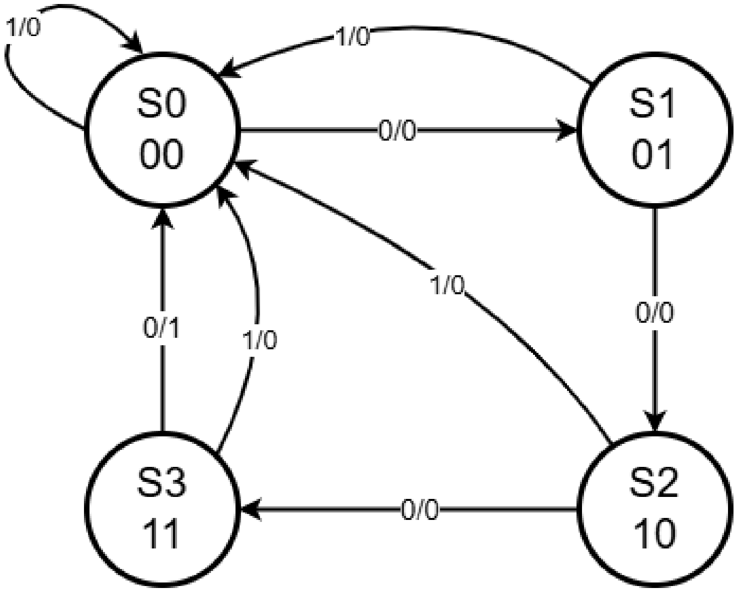
2.4 Code 0000 Circuit

2.4.1. Defining the inputs and outputs and the State Diagram

The input is the data stream “X” (to be analyzed) and the output signal “Y” that corresponds to the occurrence of the code 0000.

Since it’s a 4-bit message then 2 flip flops is needed to have 4 states.

From this information we can deduce the State Diagram:



2.4.2. State Table, State Equations and K-Maps

Then the state table is constructed based on the state diagram:

Present State		Inputs	Next State		Output
A	B	X	A$^+$	B$^+$	Y
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	0	0	1
1	1	1	0	0	0

A\BX	$\bar{B}$		B	
$\bar{A}$	0	0	0	1
A	1	0	0	0
For A$^+$	$\bar{X}$	X		$\bar{X}$

$$A^+ = \bar{A}B\bar{X} + A\bar{B}\bar{X} = (A \oplus B)\bar{X}$$

A\BX	$\bar{B}$		B	
$\bar{A}$	1	0	0	0
A	1	0	0	0
For B$^+$	$\bar{X}$	X		$\bar{X}$

$$B^+ = \bar{B}\bar{X}$$

$$Y = AB\bar{X}$$

2.4.3. Designing the Logic Circuit

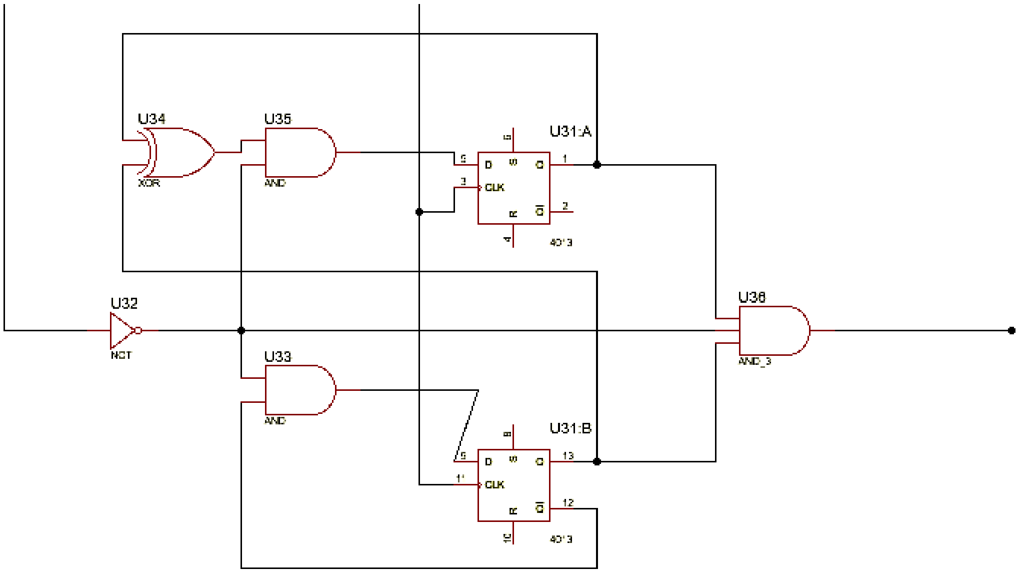
Using D-Flip Flop with the State equations:

$$D_A = A^+ = \bar{A}B\bar{X} + A\bar{B}\bar{X} = (A \oplus B)\bar{X}$$

$$D_B = B^+ = \bar{B}\bar{X}$$

$$Y = AB\bar{X}$$

So the Final Circuit would be :

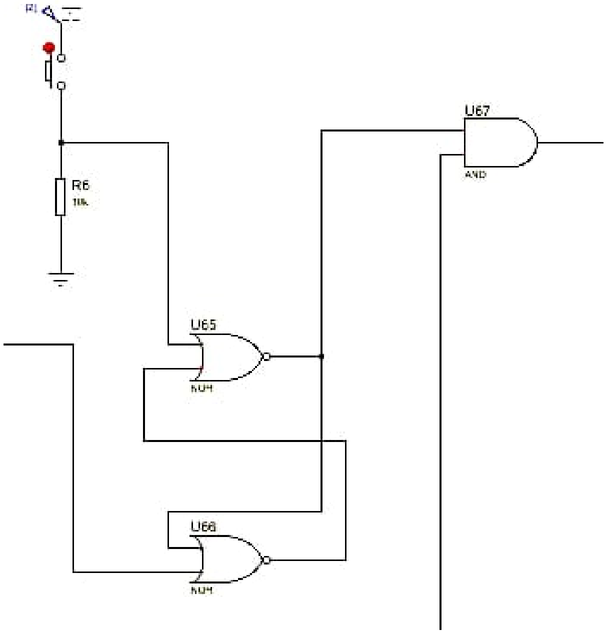


Note: it’s the same 1111 code circuit but with the input inverted (which is expected).

2.4.4. Counter Circuit

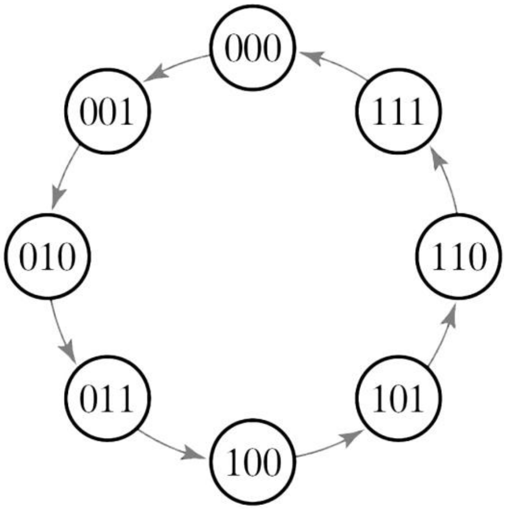
Since the output is an instantaneous pulse, we'll use an SR latch to make it a constant voltage state with a stop button to reset the latch (this method is used throughout the project).

To Trigger the counter we'll connect it to the clock signal AND-ed with the control signal.



Counter Circuit

- **Designing the counter circuit :**



State diagram

Present State			Next State		
A	B	C	A^+	B^+	C^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

State Table

A\BC	$\bar{B}$		B	
$\bar{A}$	0	0	1	0
A	1	1	0	1
For A^+	$\bar{C}$	C		$\bar{C}$

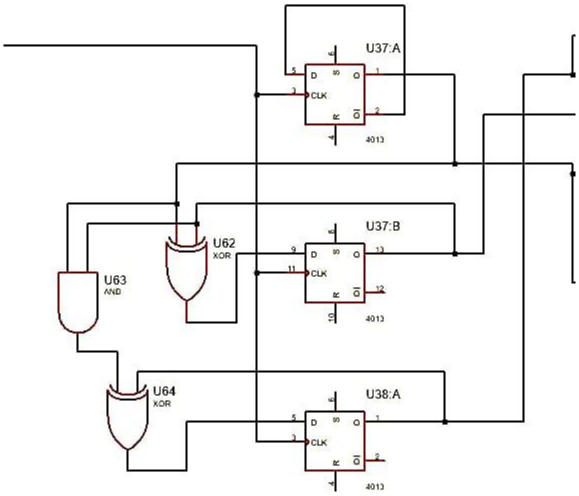
$$A^+ = A\bar{C} + A\bar{B} + \bar{A}BC = (C \oplus AB)$$

A\BC	$\bar{B}$		B	
$\bar{A}$	0	1	0	1
A	0	1	0	1
For B$^+$	$\bar{C}$	C		$\bar{C}$

$$B^+ = B\bar{C} + C\bar{B} = (C \oplus B)$$

A\BC	$\bar{B}$		B	
$\bar{A}$	1	0	0	1
A	1	0	0	1
For C$^+$	$\bar{C}$	C		$\bar{C}$

$$C^+ = \bar{C}$$



Counter Circuit

- Binary to 7 Segment Converter

Inputs			Output						
A	B	C	a	b	c	d	e	f	g
0	0	0	1	1	1	1	1	1	0
0	0	1	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	1
0	1	1	1	1	1	1	0	0	1
1	0	0	0	1	1	0	0	1	1
1	0	1	1	0	1	1	0	1	1
1	1	0	1	0	1	1	1	1	1
1	1	1	1	1	1	0	0	0	0

A\BC	$\bar{B}$		B	
$\bar{A}$	1	0	1	1
A	0	1	1	1
For a	$\bar{C}$	C		$\bar{C}$

$$a = AC + \bar{A}\bar{C} + B = (A \odot C) + B$$

A\BC	$\bar{B}$		B	
$\bar{A}$	1	1	1	1
A	1	0	1	0
For b	$\bar{C}$	C		$\bar{C}$

$$b = \bar{A} + \bar{B}\bar{C} + BC = (B \odot C) + \bar{A}$$

A\BC	$\bar{B}$		B	
$\bar{A}$	1	1	1	0
A	1	1	1	1
For c	$\bar{C}$	C		$\bar{C}$

$$c = A + \bar{B} + C$$

A\BC	$\bar{B}$		B	
$\bar{A}$	1	0	1	1
A	0	1	0	1
For d	$\bar{C}$	C		$\bar{C}$

$$d = \bar{A}B + \bar{A}\bar{C} + B\bar{C} + A\bar{B}C$$

A\BC	$\bar{B}$		B	
$\bar{A}$	1	0	0	1
A	0	0	0	1
For e	$\bar{C}$	C		$\bar{C}$

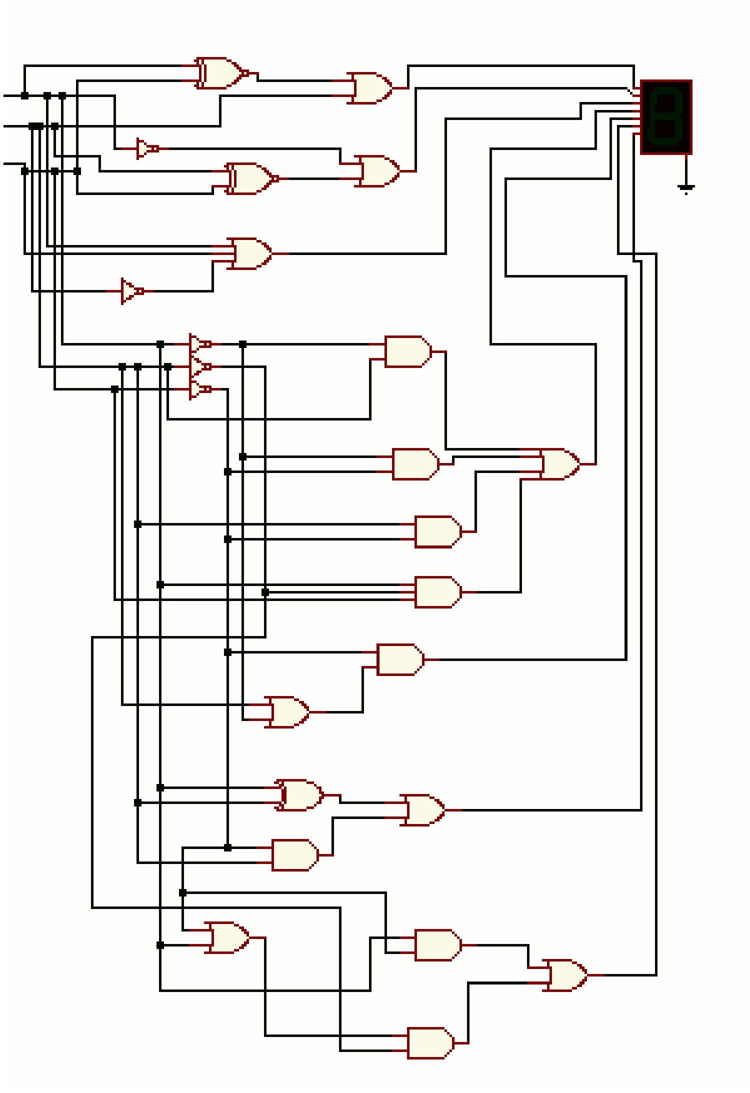
$$e = B\bar{C} + \bar{A}\bar{C} = \bar{C}(B + \bar{A})$$

A\BC	$\bar{B}$		B	
$\bar{A}$	1	0	0	0
A	1	1	0	1
For f	$\bar{C}$	C		$\bar{C}$

$$f = \bar{B}\bar{C} + A\bar{B} + A\bar{C} = \bar{B}(\bar{C} + A) + A\bar{C}$$

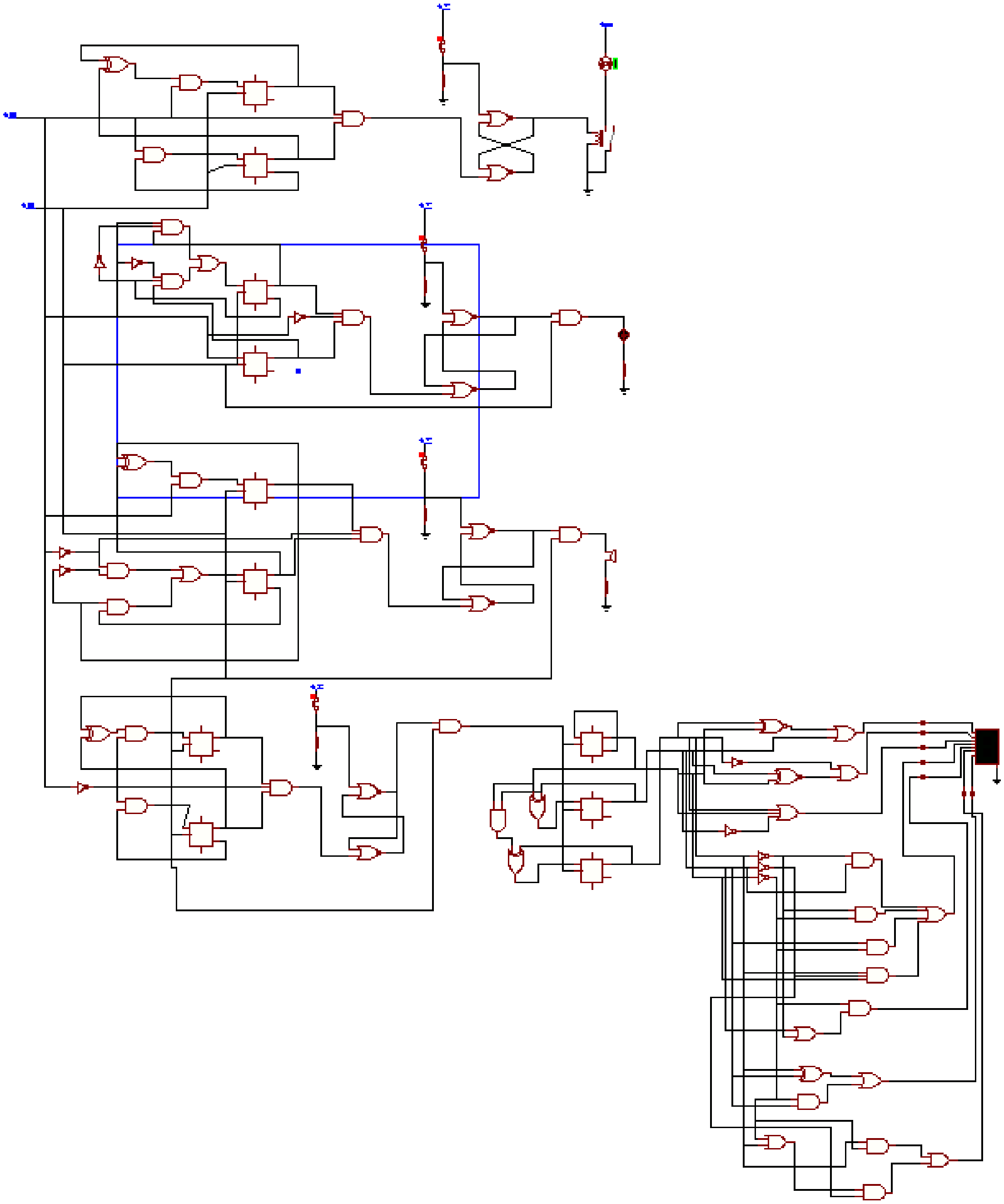
A\BC	$\bar{B}$		B	
$\bar{A}$	0	0	1	1
A	1	1	0	1
For g	$\bar{C}$	C		$\bar{C}$

$$g = A\bar{B} + \bar{A}B + B\bar{C} = (A \oplus B) + B\bar{C}$$

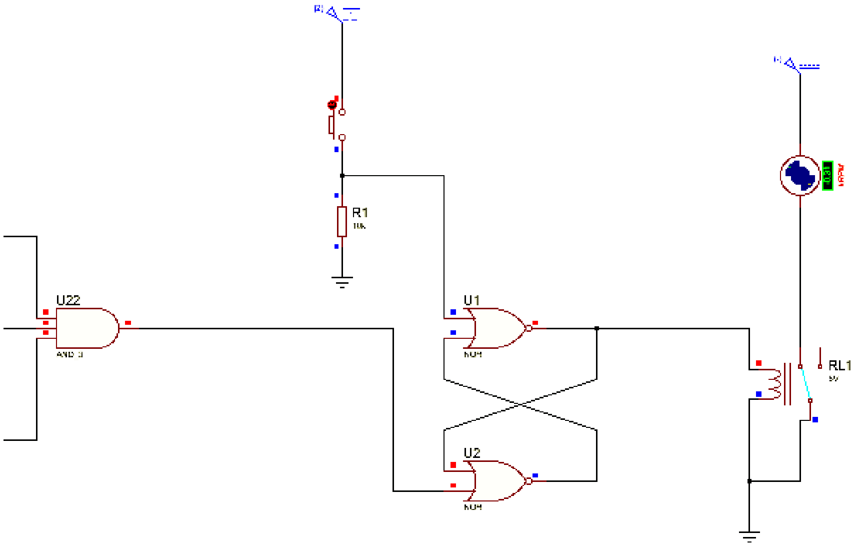


3.implementation in proteus

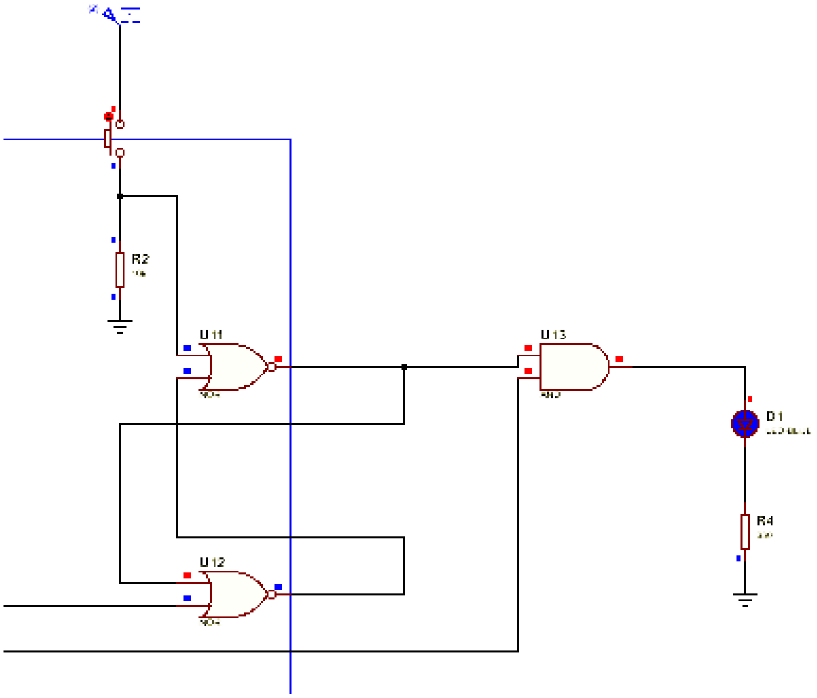
3.1. Schematic Diagram



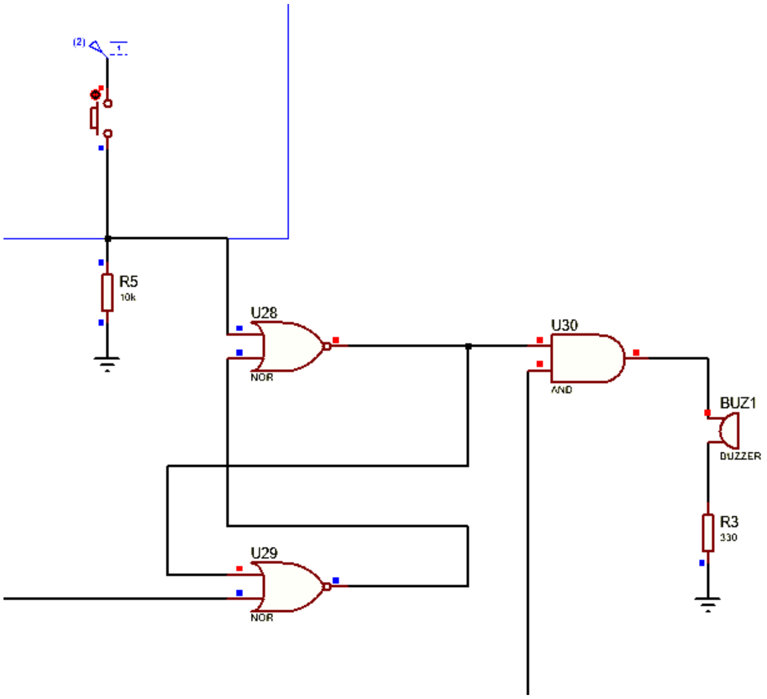
3.2. Testing the Circuit



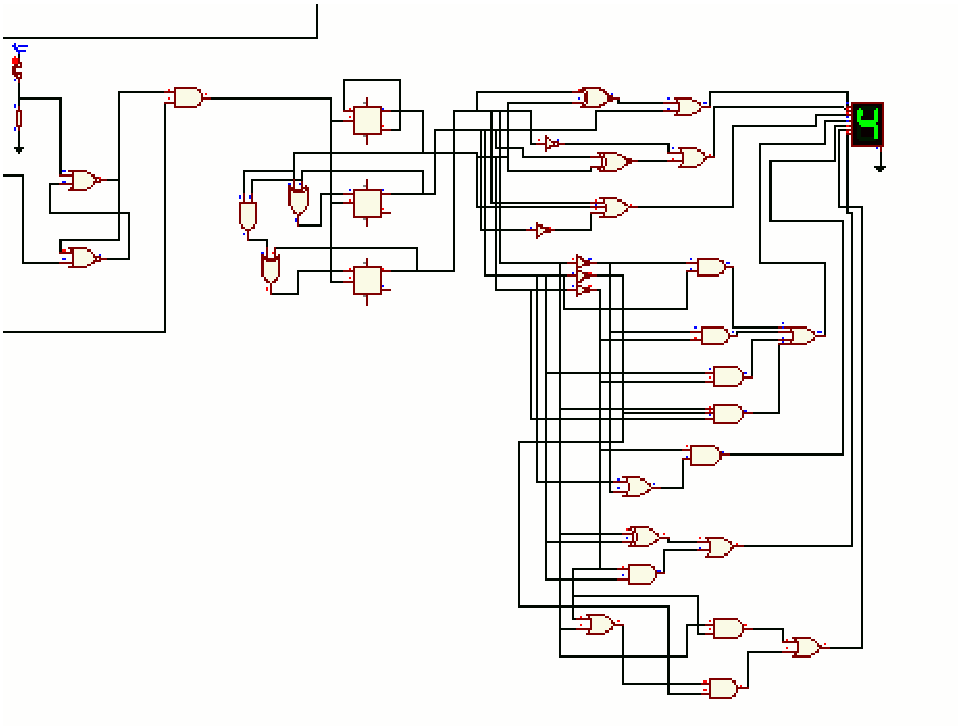
Testing the 1111 Code Circuit



Testing the 1010 Code Circuit



Testing the 0110 Code Circuit



Testing the 0000 Code Circuit