

Amplifier Design

احمد حسين عبدالعال علي

Required Specifications:

Gain	40 db	$= 10^{40/20} \approx 100$
Bandwidth	1M Hz	At $C_L = 1nF$
Power consumption	20μW	At $V_{CC} = 1.5V$

Since $BW = \frac{1}{2\pi C_{out} R_{out}}$ (Where the dominant pole is the output's)

Assuming direct coupling ($f_o \approx 0$),

$C_{out} \cong C_L$ or $1.05C_L$ (Taking in consideration C_{BC})

$$\text{So, } R_{out(MAX)} = \frac{1}{2\pi C_{out} BW} = \frac{1}{2\pi \times 1.05 \times 10^{-9} \times 10^6} = 151.57 \Omega$$

BW stage:

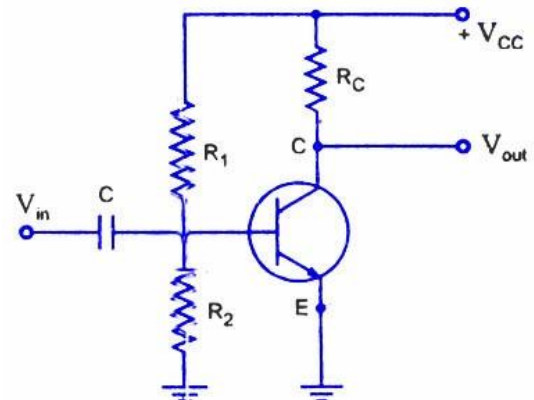
CE stage with $R_C = R_{out} = 100 \Omega$ (Leaving margin for the other stages).

- For R_1, R_2 :

$$V_{th} = I_B R_{th} + V_{BE}$$

$$V_{CC} \times \frac{R_2}{R_1 + R_2} = I_B \times \frac{R_1 R_2}{R_1 + R_2} + V_{BE}$$

$$\text{And since } I_B = \frac{I_S}{\beta} e^{\frac{V_{BE}}{V_t}}$$



- So, for $R_2 = 1000K\Omega$, $R_1 = 1650K\Omega$ (for min current consumption in this branch).

$$|A_{VBWstage}| = g_m R_C = \frac{I_C}{V_t} R_C = \frac{12.2 \times 10^{-6} \times 100}{0.026} = 0.046923$$

$$|A_{VTotal}| = |A_{Vgainstage}|^n \times |A_{VBWstage}| = 100$$

$$|A_{Vgainstage}|^n \text{ must be } = 2131.14$$

✚ For The Gain Stages:

CE Stages for gain:

- First, we need to make sure that the output pole is the dominant so that the gain stages don't affect the BW
- Since C_{in} is based on the transistors parasitic capacitance which is in the pico range (Assuming 50pF)

$$\text{so } R_{C(Stages(max))} = \frac{1}{2\pi \times 50 \times 10^{-12} \times 10^6} = 3.183K\Omega$$

- We'll be using 1.1k Ω and 1k Ω .

$$|A_{Vgainstage}| = \sqrt[n]{2131.14} = \sqrt[7]{2131.14} \cong 3 \text{ (for 7 stages)}$$

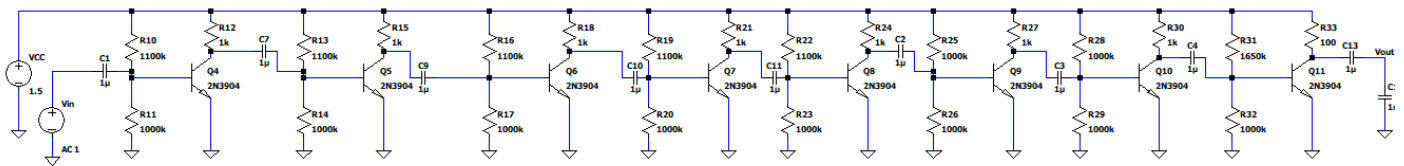
$$\text{But } |A_{Vgainstage}| = g_m R_C = g_m \times 1100 \text{ must be } 3$$

$$\text{So } g_m = \frac{3}{1100} = 2.727 \text{ mS}, g_m = \frac{I_C}{V_t} = 2.727 \times 10^{-3}$$

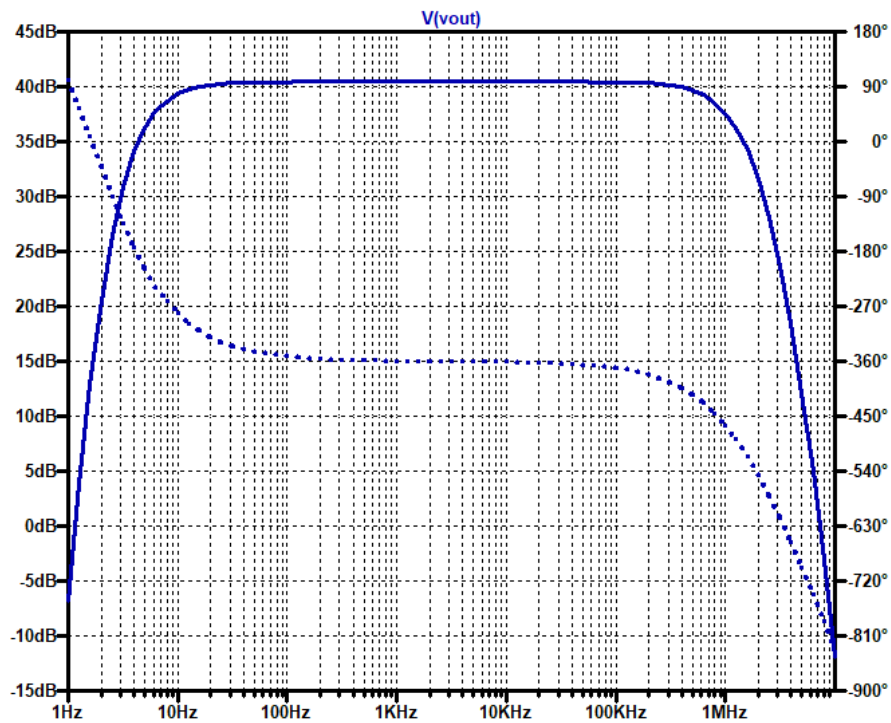
$$I_C = 0.026 \times 2.727 \times 10^{-3} = 70.9\mu A$$

- By using the same analysis method as before,
for $R_2 = 1000K\Omega$, $R_1 = 1100K\Omega$ (for min current consumption in this branch).

Final Circuit:



Simulation Results:



Gain	Bandwidth	Power consumption
40.437 db	1.0429 Mhz	861.15 μW

Results:

Spec	Required	Achieved
Gain	40 db	40.437 db
Bandwidth	1 MHz	1.0429 Mhz
Power consumption	20 μW	861.15 μW