

## Analog to Digital Converter

### Features

- 10-bit Resolution
- 0.5 LSB Integral Non-linearity
- $\pm 2$  LSB Absolute Accuracy
- 65 - 260  $\mu$ s Conversion Time
- Up to 15 kSPS at Maximum Resolution
- 8 Multiplexed Single Ended Input Channels
- 7 Differential Input Channels
- 2 Differential Input Channels with Optional Gain of 10x and 200x<sup>(1)</sup>
- Optional Left adjustment for ADC Result Readout
- 0 -  $V_{CC}$  ADC Input Voltage Range
- Selectable 2.56V ADC Reference Voltage
- Free Running or Single Conversion Mode
- ADC Start Conversion by Auto Triggering on Interrupt Sources
- Interrupt on ADC Conversion Complete
- Sleep Mode Noise Canceler

Note: 1. The differential input channels are not tested for devices in PDIP Package. This feature is only guaranteed to work for devices in TQFP and MLF Packages

The ATmega32 features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel Analog Multiplexer which allows 8 single-ended voltage inputs constructed from the pins of Port A. The single-ended voltage inputs refer to 0V (GND).

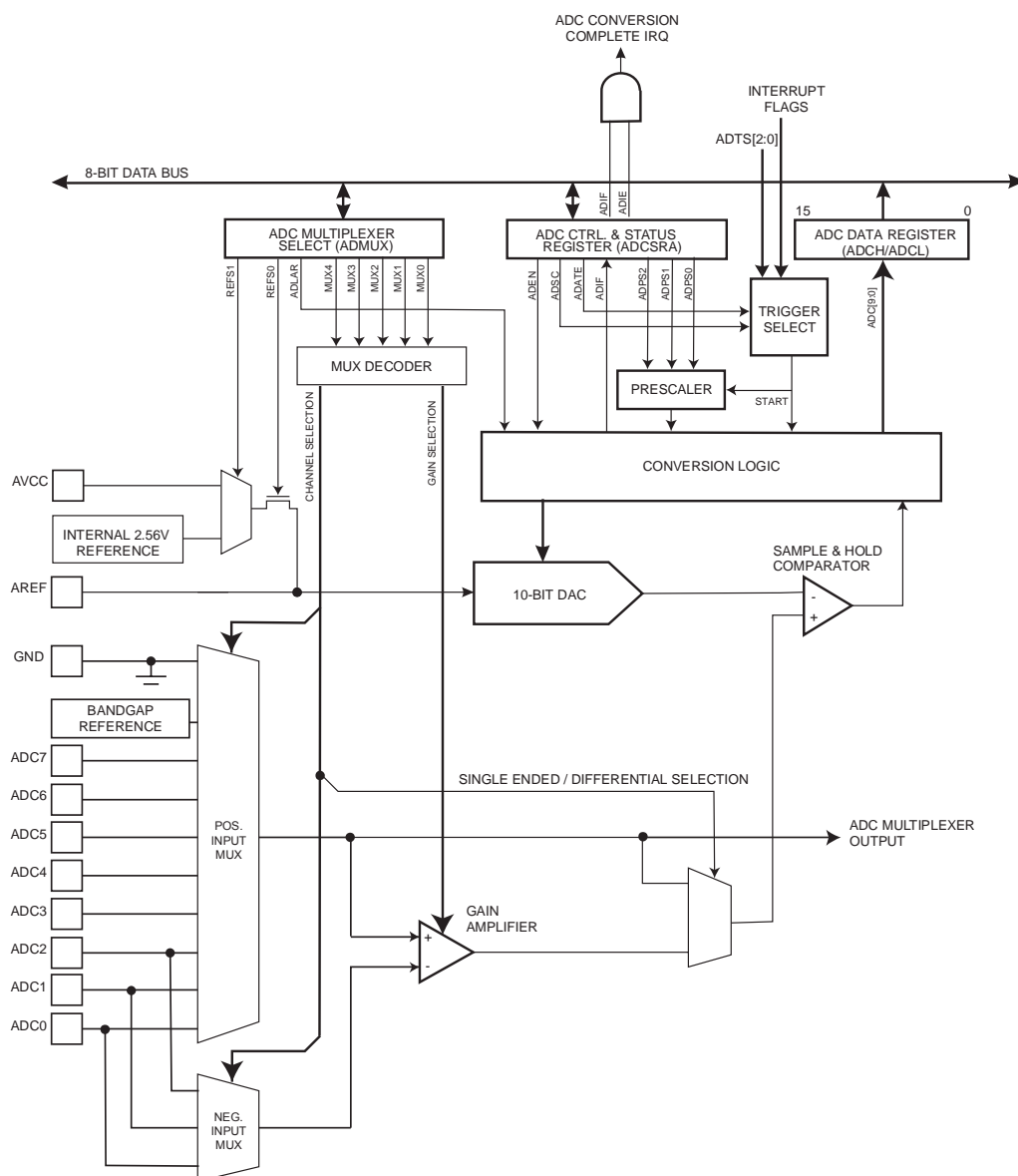
The device also supports 16 differential voltage input combinations. Two of the differential inputs (ADC1, ADC0 and ADC3, ADC2) are equipped with a programmable gain stage, providing amplification steps of 0 dB (1x), 20 dB (10x), or 46 dB (200x) on the differential input voltage before the A/D conversion. Seven differential analog input channels share a common negative terminal (ADC1), while any other ADC input can be selected as the positive input terminal. If 1x or 10x gain is used, 8-bit resolution can be expected. If 200x gain is used, 7-bit resolution can be expected.

The ADC contains a Sample and Hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 98.

The ADC has a separate analog supply voltage pin, AVCC. AVCC must not differ more than  $\pm 0.3$  V from  $V_{CC}$ . See the paragraph "ADC Noise Canceler" on page 207 on how to connect this pin.

Internal reference voltages of nominally 2.56V or AVCC are provided On-chip. The voltage reference may be externally decoupled at the AREF pin by a capacitor for better noise performance.

**Figure 98.** Analog to Digital Converter Block Schematic



## Operation

The ADC converts an analog input voltage to a 10-bit digital value through successive approximation. The minimum value represents GND and the maximum value represents the voltage on the AREF pin minus 1 LSB. Optionally, AVCC or an internal 2.56V reference voltage may be connected to the AREF pin by writing to the REFSn bits in the ADMUX Register. The internal voltage reference may thus be decoupled by an external capacitor at the AREF pin to improve noise immunity.

The analog input channel and differential gain are selected by writing to the MUX bits in ADMUX. Any of the ADC input pins, as well as GND and a fixed bandgap voltage reference, can be selected as single ended inputs to the ADC. A selection of ADC input pins can be selected as positive and negative inputs to the differential gain amplifier.

If differential channels are selected, the differential gain stage amplifies the voltage difference between the selected input channel pair by the selected gain factor. This

amplified value then becomes the analog input to the ADC. If single ended channels are used, the gain amplifier is bypassed altogether.

The ADC is enabled by setting the ADC Enable bit, ADEN in ADCSRA. Voltage reference and input channel selections will not go into effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power saving sleep modes.

The ADC generates a 10-bit result which is presented in the ADC Data Registers, ADCH and ADCL. By default, the result is presented right adjusted, but can optionally be presented left adjusted by setting the ADLAR bit in ADMUX.

If the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH, to ensure that the content of the Data Registers belongs to the same conversion. Once ADCL is read, ADC access to Data Registers is blocked. This means that if ADCL has been read, and a conversion completes before ADCH is read, neither register is updated and the result from the conversion is lost. When ADCH is read, ADC access to the ADCH and ADCL Registers is re-enabled.

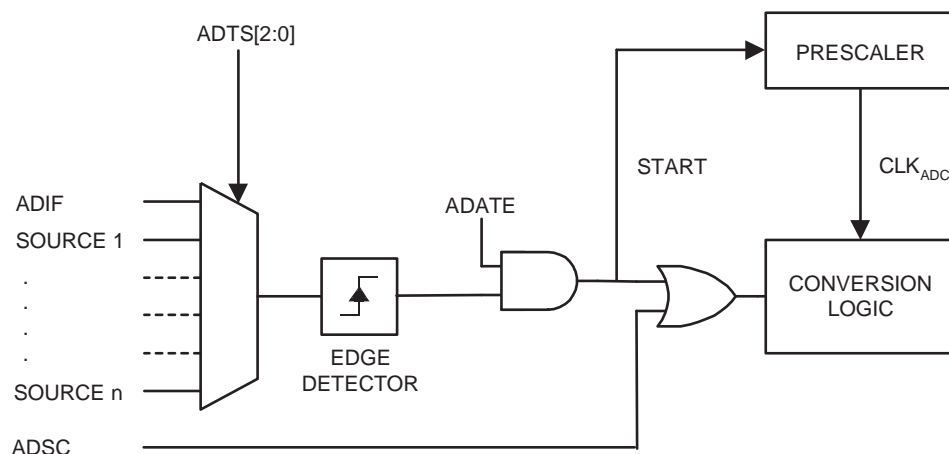
The ADC has its own interrupt which can be triggered when a conversion completes. When ADC access to the Data Registers is prohibited between reading of ADCH and ADCL, the interrupt will trigger even if the result is lost.

## **Starting a Conversion**

A single conversion is started by writing a logical one to the ADC Start Conversion bit, ADSC. This bit stays high as long as the conversion is in progress and will be cleared by hardware when the conversion is completed. If a different data channel is selected while a conversion is in progress, the ADC will finish the current conversion before performing the channel change.

Alternatively, a conversion can be triggered automatically by various sources. Auto Triggering is enabled by setting the ADC Auto Trigger Enable bit, ADATE in ADCSRA. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in SFIOR (see description of the ADTS bits for a list of the trigger sources). When a positive edge occurs on the selected trigger signal, the ADC prescaler is reset and a conversion is started. This provides a method of starting conversions at fixed intervals. If the trigger signal still is set when the conversion completes, a new conversion will not be started. If another positive edge occurs on the trigger signal during conversion, the edge will be ignored. Note that an Interrupt Flag will be set even if the specific interrupt is disabled or the global interrupt enable bit in SREG is cleared. A conversion can thus be triggered without causing an interrupt. However, the Interrupt Flag must be cleared in order to trigger a new conversion at the next interrupt event.

**Figure 99.** ADC Auto Trigger Logic

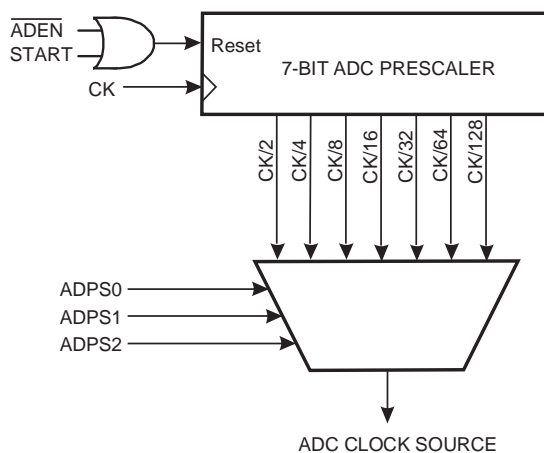


Using the ADC Interrupt Flag as a trigger source makes the ADC start a new conversion as soon as the ongoing conversion has finished. The ADC then operates in Free Running mode, constantly sampling and updating the ADC Data Register. The first conversion must be started by writing a logical one to the ADSC bit in ADCSRA. In this mode the ADC will perform successive conversions independently of whether the ADC Interrupt Flag, ADIF, is cleared or not.

If Auto Triggering is enabled, single conversions can be started by writing ADSC in ADCSRA to one. ADSC can also be used to determine if a conversion is in progress. The ADSC bit will be read as one during a conversion, independently of how the conversion was started.

## Prescaling and Conversion Timing

**Figure 100.** ADC Prescaler



By default, the successive approximation circuitry requires an input clock frequency between 50 kHz and 200 kHz to get maximum resolution. If a lower resolution than 10 bits is needed, the input clock frequency to the ADC can be higher than 200 kHz to get a higher sample rate.

The ADC module contains a prescaler, which generates an acceptable ADC clock frequency from any CPU frequency above 100 kHz. The prescaling is set by the ADPS bits in ADCSRA. The prescaler starts counting from the moment the ADC is switched on by

setting the ADEN bit in ADCSRA. The prescaler keeps running for as long as the ADEN bit is set, and is continuously reset when ADEN is low.

When initiating a single ended conversion by setting the ADSC bit in ADCSRA, the conversion starts at the following rising edge of the ADC clock cycle. See “Differential Gain Channels” on page 205 for details on differential conversion timing.

A normal conversion takes 13 ADC clock cycles. The first conversion after the ADC is switched on (ADEN in ADCSRA is set) takes 25 ADC clock cycles in order to initialize the analog circuitry.

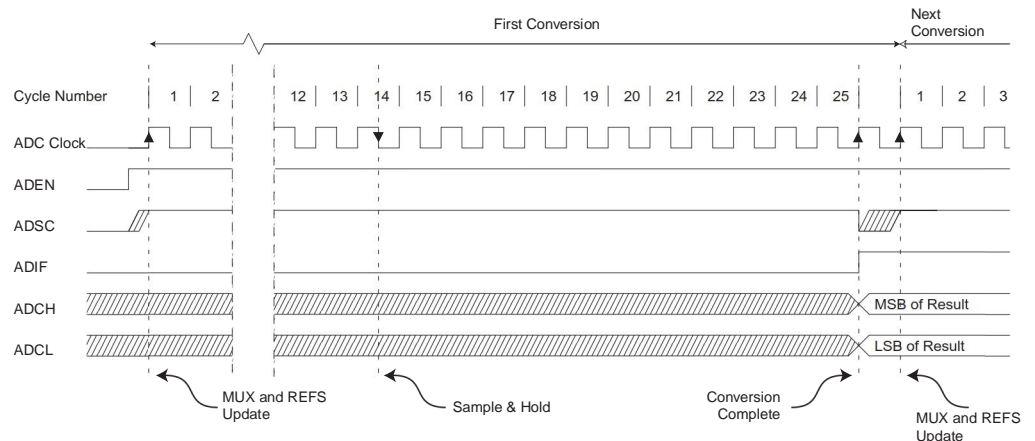
The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of a normal conversion and 13.5 ADC clock cycles after the start of a first conversion. When a conversion is complete, the result is written to the ADC Data Registers, and ADIF is set. In single conversion mode, ADSC is cleared simultaneously. The software may then set ADSC again, and a new conversion will be initiated on the first rising ADC clock edge.

When Auto Triggering is used, the prescaler is reset when the trigger event occurs. This assures a fixed delay from the trigger event to the start of conversion. In this mode, the sample-and-hold takes place 2 ADC clock cycles after the rising edge on the trigger source signal. Three additional CPU clock cycles are used for synchronization logic.

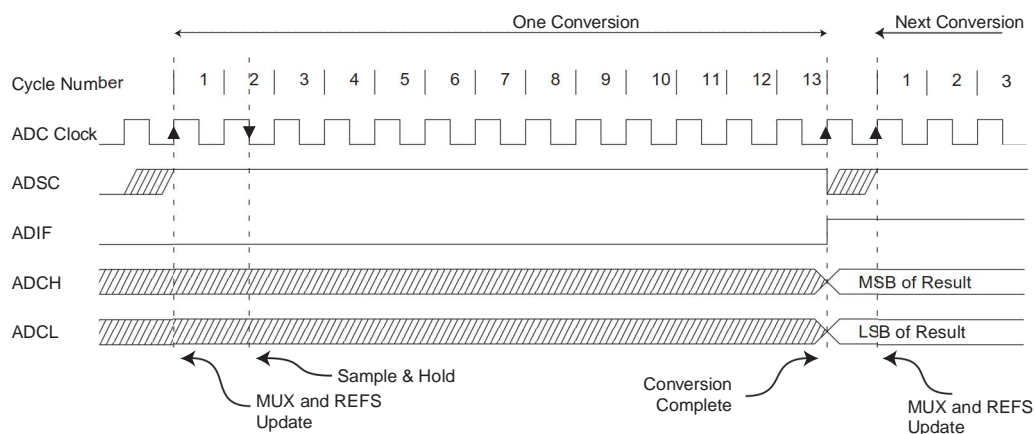
When using Differential mode, along with Auto Triggering from a source other than the ADC Conversion Complete, each conversion will require 25 ADC clocks. This is because the ADC must be disabled and re-enabled after every conversion.

In Free Running mode, a new conversion will be started immediately after the conversion completes, while ADSC remains high. For a summary of conversion times, see Table 81.

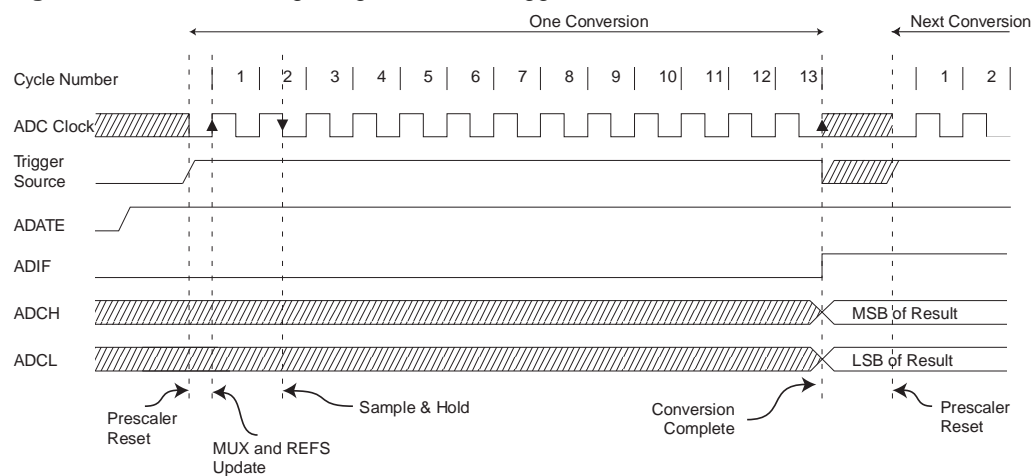
**Figure 101.** ADC Timing Diagram, First Conversion (Single Conversion Mode)



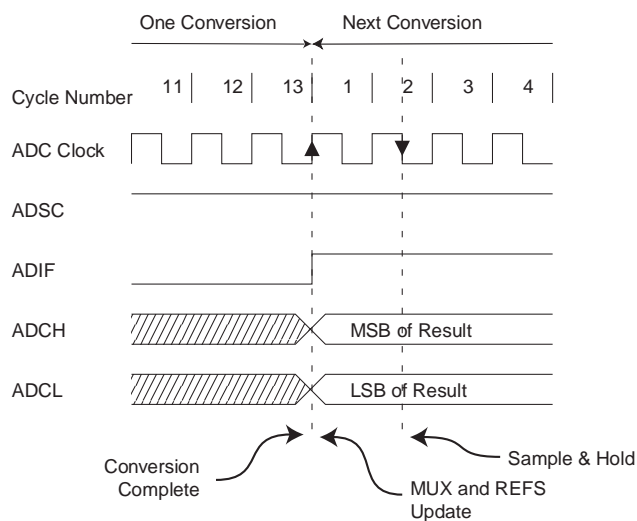
**Figure 102. ADC Timing Diagram, Single Conversion**



**Figure 103. ADC Timing Diagram, Auto Triggered Conversion**



**Figure 104. ADC Timing Diagram, Free Running Conversion**



**Table 81.** ADC Conversion Time

| Condition                        | Sample & Hold (Cycles from Start of Conversion) | Conversion Time (Cycles) |
|----------------------------------|---|--------------------------|
| First conversion                 | 14.5  | 25                       |
| Normal conversions, single ended | 1.5   | 13                       |
| Auto Triggered conversions       | 2   | 13.5                     |
| Normal conversions, differential | 1.5/2.5   | 13/14                    |

## Differential Gain Channels

When using differential gain channels, certain aspects of the conversion need to be taken into consideration.

Differential conversions are synchronized to the internal clock  $CK_{ADC2}$  equal to half the ADC clock. This synchronization is done automatically by the ADC interface in such a way that the sample-and-hold occurs at a specific phase of  $CK_{ADC2}$ . A conversion initiated by the user (i.e., all single conversions, and the first free running conversion) when  $CK_{ADC2}$  is low will take the same amount of time as a single ended conversion (13 ADC clock cycles from the next prescaled clock cycle). A conversion initiated by the user when  $CK_{ADC2}$  is high will take 14 ADC clock cycles due to the synchronization mechanism. In Free Running mode, a new conversion is initiated immediately after the previous conversion completes, and since  $CK_{ADC2}$  is high at this time, all automatically started (i.e., all but the first) free running conversions will take 14 ADC clock cycles.

The gain stage is optimized for a bandwidth of 4 kHz at all gain settings. Higher frequencies may be subjected to non-linear amplification. An external low-pass filter should be used if the input signal contains higher frequency components than the gain stage bandwidth. Note that the ADC clock frequency is independent of the gain stage bandwidth limitation. For example, the ADC clock period may be 6  $\mu$ s, allowing a channel to be sampled at 12 kSPS, regardless of the bandwidth of this channel.

If differential gain channels are used and conversions are started by Auto Triggering, the ADC must be switched off between conversions. When Auto Triggering is used, the ADC prescaler is reset before the conversion is started. Since the gain stage is dependent of a stable ADC clock prior to the conversion, this conversion will not be valid. By disabling and then re-enabling the ADC between each conversion (writing ADEN in ADCSRA to “0” then to “1”), only extended conversions are performed. The result from the extended conversions will be valid. See “Prescaling and Conversion Timing” on page 202 for timing details.

## Changing Channel or Reference Selection

The MUXn and REFS1:0 bits in the ADMUX Register are single buffered through a temporary register to which the CPU has random access. This ensures that the channels and reference selection only takes place at a safe point during the conversion. The channel and reference selection is continuously updated until a conversion is started. Once the conversion starts, the channel and reference selection is locked to ensure a sufficient sampling time for the ADC. Continuous updating resumes in the last ADC clock cycle before the conversion completes (ADIF in ADCSRA is set). Note that the conversion starts on the following rising ADC clock edge after ADSC is written. The user is thus advised not to write new channel or reference selection values to ADMUX until one ADC clock cycle after ADSC is written.

If Auto Triggering is used, the exact time of the triggering event can be indeterministic. Special care must be taken when updating the ADMUX Register, in order to control which conversion will be affected by the new settings.

If both ADATE and ADEN is written to one, an interrupt event can occur at any time. If the ADMUX Register is changed in this period, the user cannot tell if the next conversion is based on the old or the new settings. ADMUX can be safely updated in the following ways:

1. When ADATE or ADEN is cleared.
2. During conversion, minimum one ADC clock cycle after the trigger event.
3. After a conversion, before the Interrupt Flag used as trigger source is cleared.

When updating ADMUX in one of these conditions, the new settings will affect the next ADC conversion.

Special care should be taken when changing differential channels. Once a differential channel has been selected, the gain stage may take as much as 125  $\mu$ s to stabilize to the new value. Thus conversions should not be started within the first 125  $\mu$ s after selecting a new differential channel. Alternatively, conversion results obtained within this period should be discarded.

The same settling time should be observed for the first differential conversion after changing ADC reference (by changing the REFS1:0 bits in ADMUX).

## ADC Input Channels

When changing channel selections, the user should observe the following guidelines to ensure that the correct channel is selected:

In Single Conversion mode, always select the channel before starting the conversion. The channel selection may be changed one ADC clock cycle after writing one to ADSC. However, the simplest method is to wait for the conversion to complete before changing the channel selection.

In Free Running mode, always select the channel before starting the first conversion. The channel selection may be changed one ADC clock cycle after writing one to ADSC. However, the simplest method is to wait for the first conversion to complete, and then change the channel selection. Since the next conversion has already started automatically, the next result will reflect the previous channel selection. Subsequent conversions will reflect the new channel selection.

When switching to a differential gain channel, the first conversion result may have a poor accuracy due to the required settling time for the automatic offset cancellation circuitry. The user should preferably disregard the first conversion result.

## ADC Voltage Reference

The reference voltage for the ADC ( $V_{REF}$ ) indicates the conversion range for the ADC. Single ended channels that exceed  $V_{REF}$  will result in codes close to 0x3FF.  $V_{REF}$  can be selected as either AVCC, internal 2.56V reference, or external AREF pin.

AVCC is connected to the ADC through a passive switch. The internal 2.56V reference is generated from the internal bandgap reference ( $V_{BG}$ ) through an internal amplifier. In either case, the external AREF pin is directly connected to the ADC, and the reference voltage can be made more immune to noise by connecting a capacitor between the AREF pin and ground.  $V_{REF}$  can also be measured at the AREF pin with a high impedant voltmeter. Note that  $V_{REF}$  is a high impedant source, and only a capacitive load should be connected in a system.

If the user has a fixed voltage source connected to the AREF pin, the user may not use the other reference voltage options in the application, as they will be shorted to the



external voltage. If no external voltage is applied to the AREF pin, the user may switch between AVCC and 2.56V as reference selection. The first ADC conversion result after switching reference voltage source may be inaccurate, and the user is advised to discard this result.

If differential channels are used, the selected reference should not be closer to AVCC than indicated in Table 122 on page 291.

## ADC Noise Canceler

The ADC features a noise canceler that enables conversion during sleep mode to reduce noise induced from the CPU core and other I/O peripherals. The noise canceler can be used with ADC Noise Reduction and Idle mode. To make use of this feature, the following procedure should be used:

1. Make sure that the ADC is enabled and is not busy converting. Single Conversion Mode must be selected and the ADC conversion complete interrupt must be enabled.
2. Enter ADC Noise Reduction mode (or Idle mode). The ADC will start a conversion once the CPU has been halted.
3. If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the CPU and execute the ADC Conversion Complete interrupt routine. If another interrupt wakes up the CPU before the ADC conversion is complete, that interrupt will be executed, and an ADC Conversion Complete interrupt request will be generated when the ADC conversion completes. The CPU will remain in active mode until a new sleep command is executed.

Note that the ADC will not be automatically turned off when entering other sleep modes than Idle mode and ADC Noise Reduction mode. The user is advised to write zero to ADEN before entering such sleep modes to avoid excessive power consumption. If the ADC is enabled in such sleep modes and the user wants to perform differential conversions, the user is advised to switch the ADC off and on after waking up from sleep to prompt an extended conversion to get a valid result.

## Analog Input Circuitry

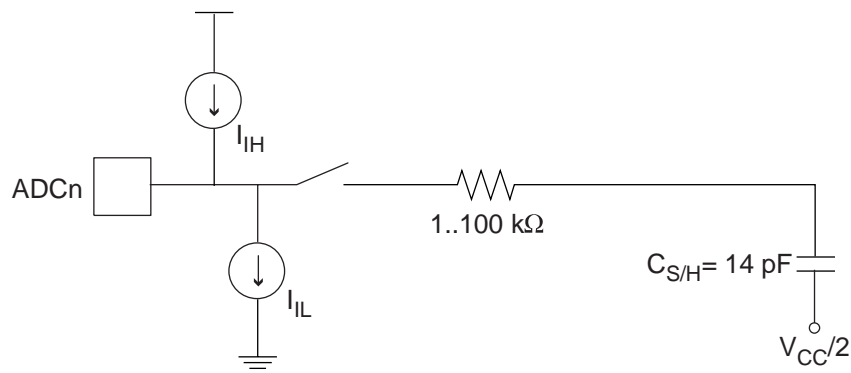
The Analog Input Circuitry for single ended channels is illustrated in Figure 105. An analog source applied to ADCn is subjected to the pin capacitance and input leakage of that pin, regardless of whether that channel is selected as input for the ADC. When the channel is selected, the source must drive the S/H capacitor through the series resistance (combined resistance in the input path).

The ADC is optimized for analog signals with an output impedance of approximately 10 k $\Omega$  or less. If such a source is used, the sampling time will be negligible. If a source with higher impedance is used, the sampling time will depend on how long time the source needs to charge the S/H capacitor, with can vary widely. The user is recommended to only use low impedant sources with slowly varying signals, since this minimizes the required charge transfer to the S/H capacitor.

If differential gain channels are used, the input circuitry looks somewhat different, although source impedances of a few hundred k $\Omega$  or less is recommended.

Signal components higher than the Nyquist frequency ( $f_{\text{ADC}}/2$ ) should not be present for either kind of channels, to avoid distortion from unpredictable signal convolution. The user is advised to remove high frequency components with a low-pass filter before applying the signals as inputs to the ADC.

**Figure 105.** Analog Input Circuitry

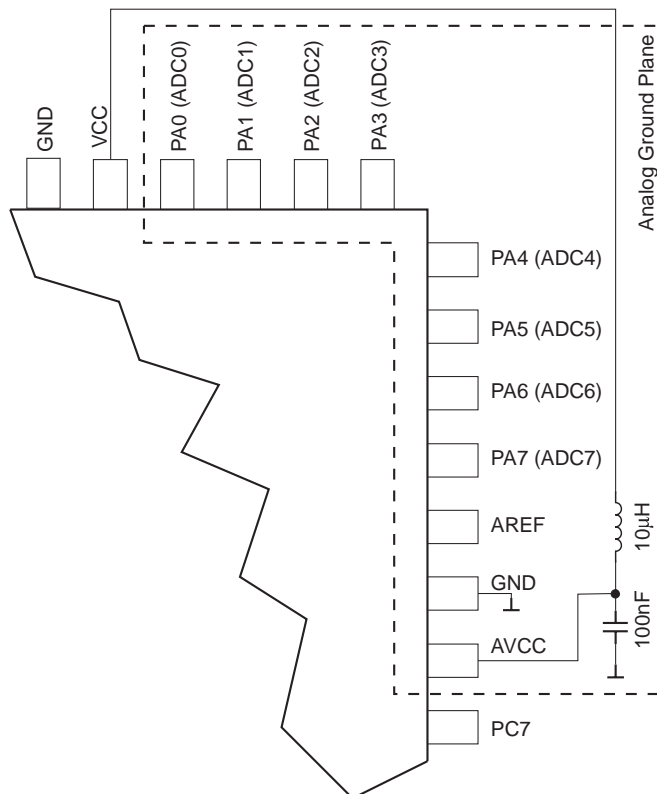


### Analog Noise Canceling Techniques

Digital circuitry inside and outside the device generates EMI which might affect the accuracy of analog measurements. If conversion accuracy is critical, the noise level can be reduced by applying the following techniques:

1. Keep analog signal paths as short as possible. Make sure analog tracks run over the analog ground plane, and keep them well away from high-speed switching digital tracks.
2. The AVCC pin on the device should be connected to the digital  $V_{CC}$  supply voltage via an LC network as shown in Figure 106.
3. Use the ADC noise canceler function to reduce induced noise from the CPU.
4. If any ADC port pins are used as digital outputs, it is essential that these do not switch while a conversion is in progress.

**Figure 106.** ADC Power Connections



## Offset Compensation Schemes

The gain stage has a built-in offset cancellation circuitry that nulls the offset of differential measurements as much as possible. The remaining offset in the analog path can be measured directly by selecting the same channel for both differential inputs. This offset residue can be then subtracted in software from the measurement results. Using this kind of software based offset correction, offset on any channel can be reduced below one LSB.

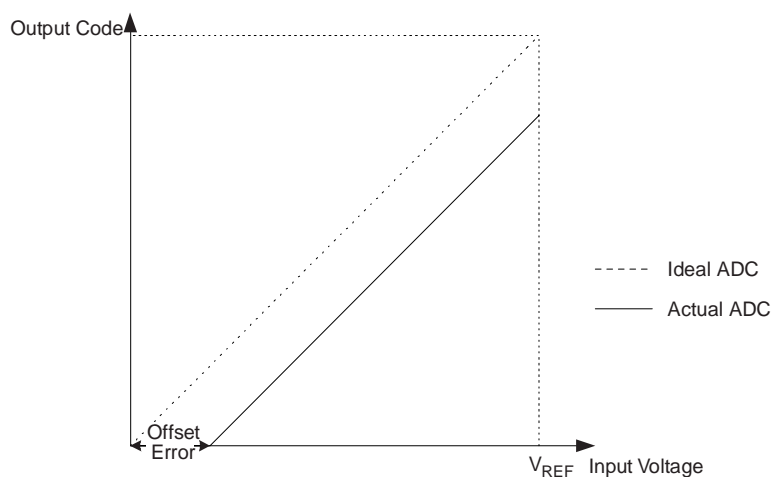
## ADC Accuracy Definitions

An n-bit single-ended ADC converts a voltage linearly between GND and  $V_{REF}$  in  $2^n$  steps (LSBs). The lowest code is read as 0, and the highest code is read as  $2^n-1$ .

Several parameters describe the deviation from the ideal behavior:

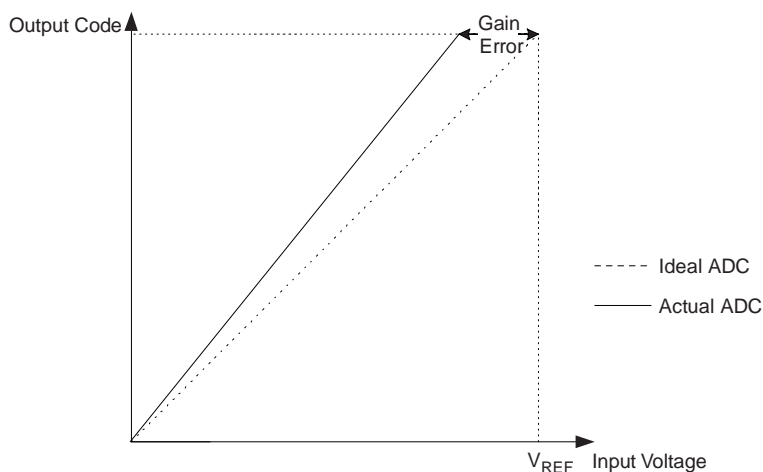
- **Offset:** The deviation of the first transition (0x000 to 0x001) compared to the ideal transition (at 0.5 LSB). Ideal value: 0 LSB.

**Figure 107. Offset Error**



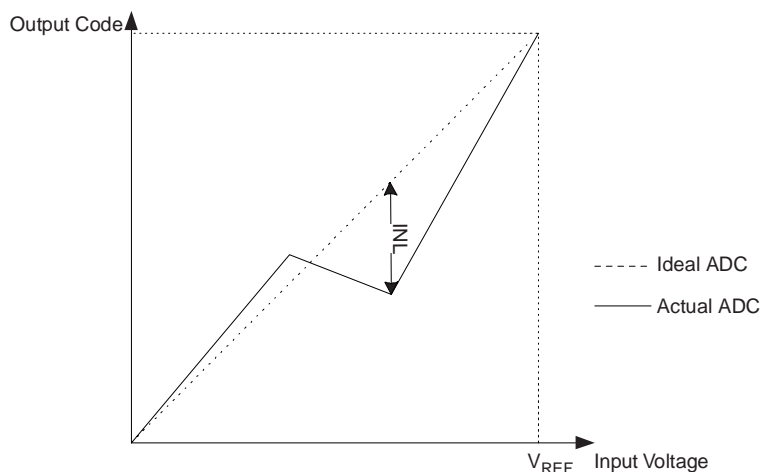
- **Gain Error:** After adjusting for offset, the Gain Error is found as the deviation of the last transition (0x3FE to 0x3FF) compared to the ideal transition (at 1.5 LSB below maximum). Ideal value: 0 LSB

**Figure 108. Gain Error**



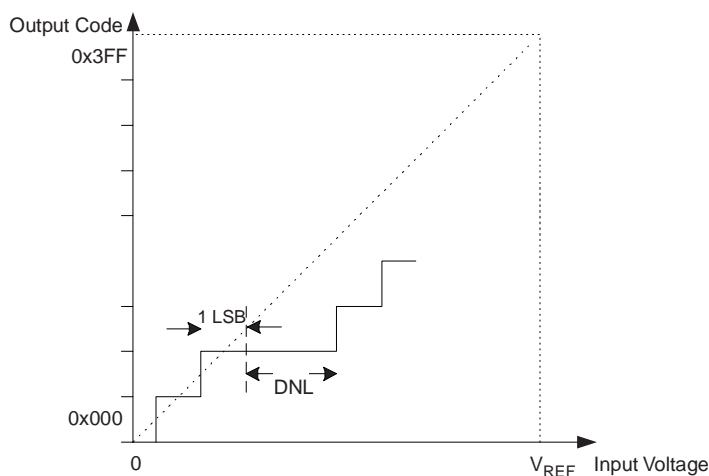
- Integral Non-linearity (INL): After adjusting for offset and gain error, the INL is the maximum deviation of an actual transition compared to an ideal transition for any code. Ideal value: 0 LSB.

**Figure 109.** Integral Non-linearity (INL)



- Differential Non-linearity (DNL): The maximum deviation of the actual code width (the interval between two adjacent transitions) from the ideal code width (1 LSB). Ideal value: 0 LSB.

**Figure 110.** Differential Non-linearity (DNL)



- Quantization Error: Due to the quantization of the input voltage into a finite number of codes, a range of input voltages (1 LSB wide) will code to the same value. Always  $\pm 0.5$  LSB.
- Absolute Accuracy: The maximum deviation of an actual (unadjusted) transition compared to an ideal transition for any code. This is the compound effect of Offset, Gain Error, Differential Error, Non-linearity, and Quantization Error. Ideal value:  $\pm 0.5$  LSB.

## ADC Conversion Result

After the conversion is complete (ADIF is high), the conversion result can be found in the ADC Result Registers (ADCL, ADCH).

For single ended conversion, the result is

$$ADC = \frac{V_{IN} \cdot 1024}{V_{REF}}$$

where  $V_{IN}$  is the voltage on the selected input pin and  $V_{REF}$  the selected voltage reference (see Table 83 on page 212 and Table 84 on page 213). 0x000 represents analog ground, and 0x3FF represents the selected reference voltage minus one LSB.

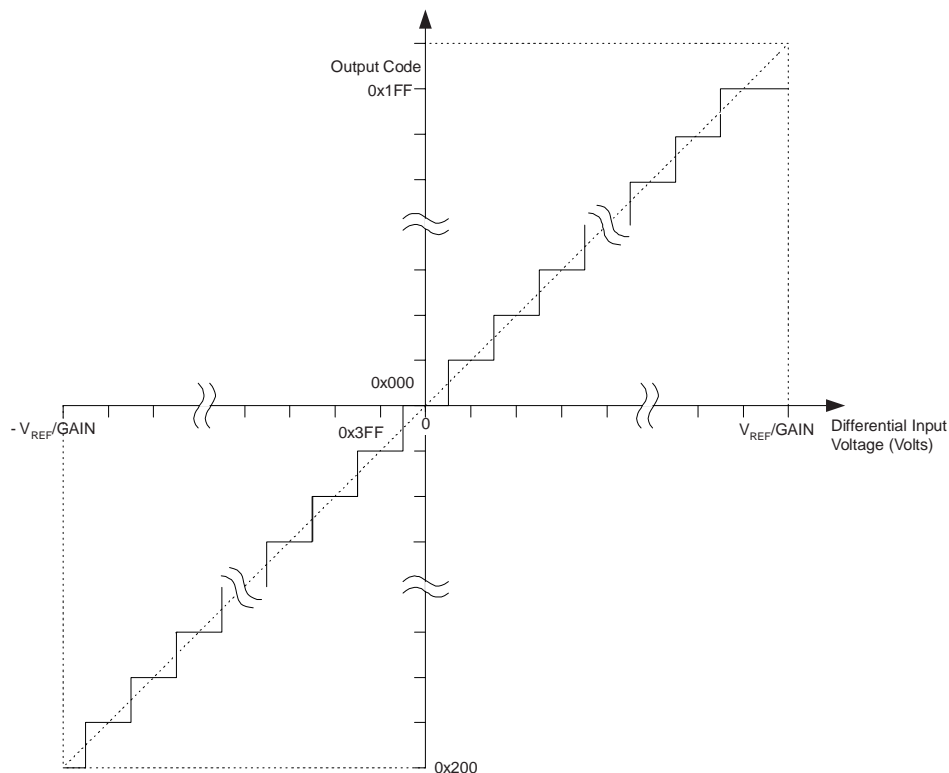
If differential channels are used, the result is

$$ADC = \frac{(V_{POS} - V_{NEG}) \cdot GAIN \cdot 512}{V_{REF}}$$

where  $V_{POS}$  is the voltage on the positive input pin,  $V_{NEG}$  the voltage on the negative input pin, GAIN the selected gain factor, and  $V_{REF}$  the selected voltage reference. The result is presented in two's complement form, from 0x200 (-512d) through 0x1FF (+511d). Note that if the user wants to perform a quick polarity check of the results, it is sufficient to read the MSB of the result (ADC9 in ADCH). If this bit is one, the result is negative, and if this bit is zero, the result is positive. Figure 111 shows the decoding of the differential input range.

Table 82 shows the resulting output codes if the differential input channel pair (ADCn - ADCm) is selected with a gain of GAIN and a reference voltage of  $V_{REF}$ .

**Figure 111.** Differential Measurement Range



**Table 82.** Correlation between Input Voltage and Output Codes

| $V_{ADCn}$                      | Read code | Corresponding Decimal Value |
|---------------------------------|-----------|-----------------------------|
| $V_{ADCm} + V_{REF}/GAIN$       | 0x1FF     | 511                         |
| $V_{ADCm} + 0.999 V_{REF}/GAIN$ | 0x1FF     | 511                         |
| $V_{ADCm} + 0.998 V_{REF}/GAIN$ | 0x1FE     | 510                         |
| ...                             | ...       | ...                         |
| $V_{ADCm} + 0.001 V_{REF}/GAIN$ | 0x001     | 1                           |
| $V_{ADCm}$                      | 0x000     | 0                           |
| $V_{ADCm} - 0.001 V_{REF}/GAIN$ | 0x3FF     | -1                          |
| ...                             | ...       | ...                         |
| $V_{ADCm} - 0.999 V_{REF}/GAIN$ | 0x201     | -511                        |
| $V_{ADCm} - V_{REF}/GAIN$       | 0x200     | -512                        |

Example:

ADMUX = 0xED (ADC3 - ADC2, 10x gain, 2.56V reference, left adjusted result)

Voltage on ADC3 is 300 mV, voltage on ADC2 is 500 mV.

ADCR =  $512 * 10 * (300 - 500) / 2560 = -400 = 0x270$

ADCL will thus read 0x00, and ADCH will read 0x9C. Writing zero to ADLAR right adjusts the result: ADCL = 0x70, ADCH = 0x02.

## ADC Multiplexer Selection Register – ADMUX

| Bit           | 7     | 6     | 5     | 4    | 3    | 2    | 1    | 0    |       |
|---------------|-------|-------|-------|------|------|------|------|------|-------|
|               | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | ADMUX |
| Read/Write    | R/W   | R/W   | R/W   | R/W  | R/W  | R/W  | R/W  | R/W  |       |
| Initial Value | 0     | 0     | 0     | 0    | 0    | 0    | 0    | 0    |       |

### • Bit 7:6 – REFS1:0: Reference Selection Bits

These bits select the voltage reference for the ADC, as shown in Table 83. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set). The internal voltage reference options may not be used if an external reference voltage is being applied to the AREF pin.

**Table 83.** Voltage Reference Selections for ADC

| REFS1 | REFS0 | Voltage Reference Selection  |
|-------|-------|--|
| 0     | 0     | AREF, Internal Vref turned off                                       |
| 0     | 1     | AVCC with external capacitor at AREF pin                             |
| 1     | 0     | Reserved   |
| 1     | 1     | Internal 2.56V Voltage Reference with external capacitor at AREF pin |

### • Bit 5 – ADLAR: ADC Left Adjust Result

The ADLAR bit affects the presentation of the ADC conversion result in the ADC Data Register. Write one to ADLAR to left adjust the result. Otherwise, the result is right adjusted. Changing the ADLAR bit will affect the ADC Data Register immediately,

regardless of any ongoing conversions. For a complete description of this bit, see “The ADC Data Register – ADCL and ADCH” on page 215.

- **Bits 4:0 – MUX4:0: Analog Channel and Gain Selection Bits**

The value of these bits selects which combination of analog inputs are connected to the ADC. These bits also select the gain for the differential channels. See Table 84 for details. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set).

**Table 84.** Input Channel and Gain Selections

| MUX4..0              | Single Ended Input | Positive Differential Input | Negative Differential Input | Gain |
|----------------------|--------------------|-----------------------------|-----------------------------|------|
| 00000                | ADC0               | N/A                         |                             |      |
| 00001                | ADC1               |                             |                             |      |
| 00010                | ADC2               |                             |                             |      |
| 00011                | ADC3               |                             |                             |      |
| 00100                | ADC4               |                             |                             |      |
| 00101                | ADC5               |                             |                             |      |
| 00110                | ADC6               |                             |                             |      |
| 00111                | ADC7               |                             |                             |      |
| 01000                | N/A                | ADC0                        | ADC0                        | 10x  |
| 01001                |                    | ADC1                        | ADC0                        | 10x  |
| 01010 <sup>(1)</sup> |                    | ADC0                        | ADC0                        | 200x |
| 01011 <sup>(1)</sup> |                    | ADC1                        | ADC0                        | 200x |
| 01100                |                    | ADC2                        | ADC2                        | 10x  |
| 01101                |                    | ADC3                        | ADC2                        | 10x  |
| 01110 <sup>(1)</sup> |                    | ADC2                        | ADC2                        | 200x |
| 01111 <sup>(1)</sup> |                    | ADC3                        | ADC2                        | 200x |
| 10000                |                    | ADC0                        | ADC1                        | 1x   |
| 10001                |                    | ADC1                        | ADC1                        | 1x   |
| 10010                |                    | ADC2                        | ADC1                        | 1x   |
| 10011                |                    | ADC3                        | ADC1                        | 1x   |
| 10100                |                    | ADC4                        | ADC1                        | 1x   |
| 10101                |                    | ADC5                        | ADC1                        | 1x   |
| 10110                |                    | ADC6                        | ADC1                        | 1x   |
| 10111                |                    | ADC7                        | ADC1                        | 1x   |
| 11000                |                    | ADC0                        | ADC2                        | 1x   |
| 11001                |                    | ADC1                        | ADC2                        | 1x   |
| 11010                |                    | ADC2                        | ADC2                        | 1x   |
| 11011                |                    | ADC3                        | ADC2                        | 1x   |
| 11100                |                    | ADC4                        | ADC2                        | 1x   |

**Table 84.** Input Channel and Gain Selections (Continued)

| MUX4..0 | Single Ended Input  | Positive Differential Input | Negative Differential Input | Gain |
|---------|---------------------|-----------------------------|-----------------------------|------|
| 11101   |                     | ADC5                        | ADC2                        | 1x   |
| 11110   | 1.22 V ( $V_{BG}$ ) | N/A                         |                             |      |
| 11111   | 0 V (GND)           |                             |                             |      |

Note: 1. The differential input channels are not tested for devices in PDIP Package. This feature is only guaranteed to work for devices in TQFP and MLF Packages

## ADC Control and Status Register A – ADCSRA

| Bit           | 7    | 6    | 5     | 4    | 3    | 2     | 1     | 0     |        |
|---------------|------|------|-------|------|------|-------|-------|-------|--------|
|               | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | ADCSRA |
| Read/Write    | R/W  | R/W  | R/W   | R/W  | R/W  | R/W   | R/W   | R/W   |        |
| Initial Value | 0    | 0    | 0     | 0    | 0    | 0     | 0     | 0     |        |

### • Bit 7 – ADEN: ADC Enable

Writing this bit to one enables the ADC. By writing it to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress, will terminate this conversion.

### • Bit 6 – ADSC: ADC Start Conversion

In Single Conversion mode, write this bit to one to start each conversion. In Free Running Mode, write this bit to one to start the first conversion. The first conversion after ADSC has been written after the ADC has been enabled, or if ADSC is written at the same time as the ADC is enabled, will take 25 ADC clock cycles instead of the normal 13. This first conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. Writing zero to this bit has no effect.

### • Bit 5 – ADATE: ADC Auto Trigger Enable

When this bit is written to one, Auto Triggering of the ADC is enabled. The ADC will start a conversion on a positive edge of the selected trigger signal. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in SFIOR.

### • Bit 4 – ADIF: ADC Interrupt Flag

This bit is set when an ADC conversion completes and the Data Registers are updated. The ADC Conversion Complete Interrupt is executed if the ADIE bit and the I-bit in SREG are set. ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical one to the flag. Beware that if doing a Read-Modify-Write on ADCSRA, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

### • Bit 3 – ADIE: ADC Interrupt Enable

When this bit is written to one and the I-bit in SREG is set, the ADC Conversion Complete Interrupt is activated.



## • Bits 2:0 – ADPS2:0: ADC Prescaler Select Bits

These bits determine the division factor between the XTAL frequency and the input clock to the ADC.

**Table 85.** ADC Prescaler Selections

| ADPS2 | ADPS1 | ADPS0 | Division Factor |
|-------|-------|-------|-----------------|
| 0     | 0     | 0     | 2               |
| 0     | 0     | 1     | 2               |
| 0     | 1     | 0     | 4               |
| 0     | 1     | 1     | 8               |
| 1     | 0     | 0     | 16              |
| 1     | 0     | 1     | 32              |
| 1     | 1     | 0     | 64              |
| 1     | 1     | 1     | 128             |

## The ADC Data Register – ADCL and ADCH

*ADLAR = 0*

| Bit           | 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    |      |
|---------------|------|------|------|------|------|------|------|------|------|
|               | –    | –    | –    | –    | –    | –    | ADC9 | ADC8 | ADCH |
|               | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 | ADCL |
|               | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |      |
| Read/Write    | R    | R    | R    | R    | R    | R    | R    | R    |      |
|               | R    | R    | R    | R    | R    | R    | R    | R    |      |
| Initial Value | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |      |
|               | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |      |

*ADLAR = 1*

| Bit           | 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    |      |
|---------------|------|------|------|------|------|------|------|------|------|
|               | ADC9 | ADC8 | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADCH |
|               | ADC1 | ADC0 | –    | –    | –    | –    | –    | –    | ADCL |
|               | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |      |
| Read/Write    | R    | R    | R    | R    | R    | R    | R    | R    |      |
|               | R    | R    | R    | R    | R    | R    | R    | R    |      |
| Initial Value | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |      |
|               | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |      |

When an ADC conversion is complete, the result is found in these two registers. If differential channels are used, the result is presented in two's complement form.

When ADCL is read, the ADC Data Register is not updated until ADCH is read. Consequently, if the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH.

The ADLAR bit in ADMUX, and the MUXn bits in ADMUX affect the way the result is read from the registers. If ADLAR is set, the result is left adjusted. If ADLAR is cleared (default), the result is right adjusted.

### • ADC9:0: ADC Conversion Result

These bits represent the result from the conversion, as detailed in “ADC Conversion Result” on page 211.

## Special FunctionIO Register – SFIOR

| Bit           | 7     | 6     | 5     | 4 | 3    | 2   | 1    | 0     |       |
|---------------|-------|-------|-------|---|------|-----|------|-------|-------|
|               | ADTS2 | ADTS1 | ADTS0 | – | ACME | PUD | PSR2 | PSR10 | SFIOR |
| Read/Write    | R/W   | R/W   | R/W   | R | R/W  | R/W | R/W  | R/W   |       |
| Initial Value | 0     | 0     | 0     | 0 | 0    | 0   | 0    | 0     |       |

### • Bit 7:5 – ADTS2:0: ADC Auto Trigger Source

If ADATE in ADCSRA is written to one, the value of these bits selects which source will trigger an ADC conversion. If ADATE is cleared, the ADTS2:0 settings will have no effect. A conversion will be triggered by the rising edge of the selected Interrupt Flag. Note that switching from a trigger source that is cleared to a trigger source that is set, will generate a positive edge on the trigger signal. If ADEN in ADCSRA is set, this will start a conversion. Switching to Free Running mode (ADTS[2:0]=0) will not cause a trigger event, even if the ADC Interrupt Flag is set.

**Table 86.** ADC Auto Trigger Source Selections

| ADTS2 | ADTS1 | ADTS0 | Trigger Source                |
|-------|-------|-------|-------------------------------|
| 0     | 0     | 0     | Free Running mode             |
| 0     | 0     | 1     | Analog Comparator             |
| 0     | 1     | 0     | External Interrupt Request 0  |
| 0     | 1     | 1     | Timer/Counter0 Compare Match  |
| 1     | 0     | 0     | Timer/Counter0 Overflow       |
| 1     | 0     | 1     | Timer/Counter Compare Match B |
| 1     | 1     | 0     | Timer/Counter1 Overflow       |
| 1     | 1     | 1     | Timer/Counter1 Capture Event  |

### • Bit 4 – Res: Reserved Bit

This bit is reserved for future use in the ATmega32. For ensuring compability with future devices, this bit must be written zero when SFIOR is written.