Register Summary

38 18 19 19 1	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
SSE (SSE)	\$3F (\$5F)	SREG	- 1	Т	Н	S	V	N	Z	С	10
SEC SEC CORP								1			
SAN 1580 GICR	, ,	SPL	SP7	SP6	SP5	SP4			SP1		12
SAN-SAM GFFR	\$3C (\$5C)	OCR0	Timer/Counter	0 Output Compar	e Register			_		_	82
\$39,1895 TMSK	\$3B (\$5B)	GICR	INT1	INT0	INT2	-	-	-	IVSEL	IVCE	47, 67
\$39,1859	\$3A (\$5A)	GIFR	INTF1	INTF0	INTF2	-	-	_	_	_	68
SPACE SPAC								1			
September TWCR					ICF1						
SSS 1559 MCUCR					- TIMOTA				PGERS		
SAI 98-91 MCUCSR					_			1	18001		
S32 S52 TCCR0					JIVI I						
\$2 (\$49) CORTIAL COMMAN					COM01			1			
SSC 1971 CORP. Decided Californian Register SSC					0001	0000		0002	0001	0000	
COURT COURT COURT COURT COM CO											
SPE (SEP) TOCR1A COM1A0 COM161 COM161 FOC1A FOC1A FOC1A WGM11 WGM10 107	\$31''' (\$51)'''	OCDR	On-Chip Debu	g Register							224
SEC (44E) TOCRIB ICNCT	\$30 (\$50)	SFIOR	ADTS2	ADTS1	ADTS0	_	ACME	PUD	PSR2	PSR10	56,85,131,198,218
SCI_SEC_ TONTH	\$2F (\$4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	107
SEC (SEC) TONTIL TimerCounter1 - Counter Register A low Byte 111					-	WGM13	WGM12	CS12	CS11	CS10	
S2B (548)	, ,										
S2A (S4A)											
S29 (549) OCR18H Timer/Counter1 - Output Compare Register B Lingh Byte 1111 \$27 (547) Imericating Timer/Counter1 - Input Capture Register B Low Byte 1111 \$26 (546) Imericating Timer/Counter1 - Input Capture Register Low Byte 1111 \$26 (546) Imericating Timer/Counter1 - Input Capture Register Low Byte 1111 \$26 (546) Imericating Timer/Counter1 - Input Capture Register Low Byte 1111 Imericating Timer/Counter2 (58 list) 1111 Imericating Timer/Counter2 (58 list) Imericating Timer/Counte											
S22 (545) Circhiell Timer/Countert - Output Compare Register I Lov Byle	, ,										
S27 (S47)						• •					
S26(846) ICR1						-					
S22 (S45) TOCR2 FOC2 WGM20 COM21 COM20 WGM21 CS22 CS21 CS20 125											
\$22 (\$43)						1	WGM21	CS22	CS21	CS20	
\$22 (\$42)	\$24 (\$44)	TCNT2	Timer/Counter	2 (8 Bits)	•						127
S21 (\$41) WDTCR	\$23 (\$43)	OCR2	Timer/Counter	2 Output Compar	e Register						127
S20 S20 S20 UBRRH URSEL - - - UPM0 USBS USST USSZ UCPOL 162	\$22 (\$42)	ASSR	-	-	-	-	AS2	TCN2UB	OCR2UB	TCR2UB	128
SCO (\$40) UCSRC	\$21 (\$41)			-	-	WDTOE	WDE	1		WDP0	
S1F (S3F)	\$20 ⁽²⁾ (\$40) ⁽²⁾					-			r	1	
\$1E (\$3E)	` '		URSEL								
\$1D (\$3D)	` ,		-			-	-	-	EEAR9	EEAR8	
\$1C (\$3C)					v вуtе						
\$18 (\$38)				- Negistei	_	_	FERIE	FEMWE	FFWF	FERE	
\$14 (\$3A) DDRA DDA7 DDA6 DDA5 DDA4 DDA3 DDA2 DDA1 DDA0 64 \$19 (\$39) PINA PINA7 PINA6 PINA5 PINA6 PINA4 PINA3 PINA2 PINA1 PINA0 64 \$18 (\$38) PORTB PORTB7 PORTB6 PORTB5 PORTB6 PORTB5 DOB4 DDB3 DDB2 DDB1 DDB0 64 \$16 (\$36) PINB PINB7 PINB6 PINB5 PINB6 PINB8 PINB8 PINB2 PINB1 PINB0 65 \$15 (\$35) PORTC PORTC7 PORTC6 PORTC5 PORTC4 PORTC3 PORTC2 PORTC1 PORTC0 65 \$14 (\$34) DDRC DDC7 DDC6 DDC6 DDC6 DDC4 DDC3 DDC2 DDC1 DDC0 65 \$13 (\$33) PINC PINC7 PORTC6 PORTC5 PORTC4 PINC3 PINC2 PINC1 PINC0 65 \$13 (\$33) PINC PINC7 PORTC6 PORTC5 PORTC4 PORTC3 PORTC2 PORTC1 PORTC0 65 \$13 (\$33) PINC PINC7 PORTC6 PORTC5 PORTC4 PORTD3 PORTD2 PORTD1 PORTD0 65 \$11 (\$31) DDRD DDD7 DDD6 DDD6 DDD6 DDD6 DDD0 DDD7 DDD6 DDD6				PORTA6							
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\$17 (\$37) DDRB DDB7 DDB6 DDB5 DDB4 DDB3 DDB2 DDB1 DDB0 64	, ,		PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	
\$16 (\$36) PINB PINB7 PINB6 PINB5 PINB4 PINB3 PINB2 PINB1 PINB0 65 \$15 (\$35) PORTC PORTC7 PORTC6 PORTC6 PORTC5 PORTC4 PORTC3 PORTC2 PORTC1 PORTC0 65 \$14 (\$34) DDRC DDC7 DDC6 DDC5 DDC4 DDC3 DDC2 DDC1 DDC0 65 \$13 (\$33) PINC PINC7 PINC6 PINC5 PINC4 PINC3 PINC2 PINC1 PINC0 65 \$12 (\$32) PORTD PORTD7 PORTD6 PORTD5 PORTD4 PORTD3 PORTD2 PORTD1 PORTD0 65 \$11 (\$31) DDRD DDD7 DDD6 DDD5 DDD4 DDD3 DDD2 DDD1 DDD0 65 \$10 (\$30) PIND PIND7 PIND6 PIND5 PIND4 PIND3 PIND2 PIND1 PIND0 65 \$10 (\$30) PIND PIND7 PIND6 PIND5 PIND4 PIND3 PIND2 PIND1 PIND0 65 \$0F (\$2F) SPDR SPI Data Register \$0F (\$2F) SPDR SPI DATA Register \$0F (\$2F) SPCR SPIE SPE DORD MSTR CPOL CPHA SPR1 SPR0 136 \$0F (\$2C) UDR USART I/O Data Register \$0F (\$2C) UDR USART I/O Data Register \$0F (\$2C) UDR USART I/O DATA Register TXCIE UDRIE RXEN TXEN UCSZ2 RXB8 TXB8 161 \$0F (\$2F) USRAR ACR ACD ACBG ACO ACI ACIE ACIC ACIS1 ACIS0 199 \$0F (\$2F) ADMUX REFS1 REFS0 ADLAR MUX4 MUX3 MUX2 MUX1 MUX0 214 \$0F (\$2F) ADC ADC BAT REgister Low Byte \$0F (\$2F) ADC ADC ADC ADATE ADIF ADIF ADIE ADPS2 ADPS1 ADPS0 216 \$0F (\$2F) ADC ADC BAT Register Low Byte	\$18 (\$38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	64
\$15 (\$35)	\$17 (\$37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	64
\$14 (\$34) DDRC DDC7 DDC6 DDC5 DDC4 DDC3 DDC2 DDC1 DDC0 65 \$13 (\$33) PINC PINC7 PINC6 PINC5 PINC4 PINC3 PINC2 PINC1 PINC0 65 \$12 (\$32) PORTD PORTD7 PORTD6 PORTD5 PORTD4 PORTD3 PORTD2 PORTD1 PORTD0 65 \$11 (\$31) DDRD DDD7 DDD6 DDD5 DDD4 DDD3 DDD2 DDD1 DDD0 65 \$10 (\$30) PIND PIND7 PIND6 PIND5 PIND5 PIND4 PIND3 PIND2 PIND1 PIND0 65 \$01 (\$32) SPC SPID SPDR SPI Data Register 138 \$06 (\$2E) SPSR SPIF WCOL SPI2X 138 \$00 (\$2D) SPCR SPIE SPE DORD MSTR CPOL CPHA SPR1 SPR0 136 \$00 (\$2C) UDR USART I/O Data Register 159 \$08 (\$2B) UCSRA RXC TXC UDRE FE DOR PE U2X MPCM 160 \$04 (\$24) USRB RXCIE TXCIE UDRIE RXEN TXEN UCSZ2 RXB8 TXB8 161 \$08 (\$29) UBRRL USART Baud Rate Register Low Byte 164 \$08 (\$28) ACSR ACD ACBG ACO ACI ACIE ACIC ACIS1 ACIS0 199 \$07 (\$27) ADMUX REFS1 REFS0 ADLAR MUX4 MUX3 MUX2 MUX1 MUX0 214 \$05 (\$25) ADCH ADC Data Register Low Byte 217 \$04 (\$24) ADCL ACIC ACIS1 REPS0 217 \$04 (\$24) ADCL ACIC ACIC ACIS1 ADPS0 216 \$05 (\$25) ADCH ADC Data Register Low Byte 217 \$04 (\$24) ADCL ACIC ACIC ACIS1 ADPS0 216 \$05 (\$25) ADCH ADC Data Register Low Byte 217 \$04 (\$24) ADCL ACIC ACIC ACIC ACIC ACIC ACIC ACIC AC											
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\$0D (\$2D)					_	_	_	_	_	SPI2X	
\$0C (\$2C)					DORD	MSTR	CPOL	СРНА	SPR1		
\$0B (\$2B)											
\$09 (\$29) UBRRL USART Baud Rate Register Low Byte 164 \$08 (\$28) ACSR ACD ACBG ACO ACI ACIE ACIC ACIS1 ACIS0 199 \$07 (\$27) ADMUX REFS1 REFS0 ADLAR MUX4 MUX3 MUX2 MUX1 MUX0 214 \$06 (\$26) ADCSRA ADEN ADSC ADATE ADIF ADIE ADPS2 ADPS1 ADPS0 216 \$05 (\$25) ADCH ADC Data Register High Byte 217 \$04 (\$24) ADCL ADC Data Register Low Byte 217 \$03 (\$23) TWDR Two-wire Serial Interface Data Register		UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	
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\$07 (\$27) ADMUX REFS1 REFS0 ADLAR MUX4 MUX3 MUX2 MUX1 MUX0 214 \$06 (\$26) ADCSRA ADEN ADSC ADATE ADIF ADIE ADPS2 ADPS1 ADPS0 216 \$05 (\$25) ADCH ADC Data Register High Byte 217 \$04 (\$24) ADCL ADC Data Register Low Byte 217 \$03 (\$23) TWDR Two-wire Serial Interface Data Register 179	\$09 (\$29)		USART Baud	Rate Register Lo	w Byte	•	•		1	,	164
\$06 (\$26) ADCSRA ADEN ADSC ADATE ADIF ADIE ADPS2 ADPS1 ADPS0 216 \$05 (\$25) ADCH ADC Data Register High Byte 217 \$04 (\$24) ADCL ADC Data Register Low Byte 217 \$03 (\$23) TWDR Two-wire Serial Interface Data Register 179											
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\$04 (\$24) ADCL ADC Data Register Low Byte 217 \$03 (\$23) TWDR Two-wire Serial Interface Data Register 179					ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	
\$03 (\$23) TWDR Two-wire Serial Interface Data Register 179											
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	\$03 (\$23) \$02 (\$22)	TWAR	TWA6	TWA5	Register TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	179 179



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$01 (\$21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	-	TWPS1	TWPS0	178
\$00 (\$20)	TWBR	Two-wire Serial Interface Bit Rate Register								177

Notes:

- 1. When the OCDEN Fuse is unprogrammed, the OSCCAL Register is always accessed on this address. Refer to the debugger specific documentation for details on how to use the OCDR Register.
- 2. Refer to the USART description for details on how to access UBRRH and UCSRC.
- 3. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
- 4. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

