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Project_1

Spartan6 - DSP48A1

Main code:

DSP48A1_Project_reg.v | DSP48A1_Project.v | DSP48A1_Project_tb.v | run_DSP.do

```
module DSP48A1_Project (a,b,d,c,carryin,m,p,carryout,carryoutf,clk,opmode,cea,ceb,cec,cecarryin,ced,cem,ceopmode,cep,rsta,rstb,rstc,rstca

/*PARAMETERS*/
    parameter A0REG=0;
    parameter A1REG=1;
    parameter B0REG=0;
    parameter B1REG=1;
    parameter CREG=1;
    parameter DREG=1;
    parameter MREG=1;
    parameter PREG=1;
    parameter CARRYINREG=1;
    parameter CARRYOUTREG=1;
    parameter OPMODEREG=1;

    parameter CARRYINSEL="OPMODE5"; //select bet. CARRYIN or OPMODE5 or tie
    parameter B_INPUT="DIRECT"; //DIRECT(B) ,CASCADE(BCIN), tie
    parameter RSTTYPE="SYNC"; //SYNC, ASYNC

/*INPUT PORTS*/
/*DATA*/
    input [17:0]a,b,d;
    input [47:0]c;
    input carryin;
    output [35:0]m;
    output [47:0]p;
    output carryout,carryoutf;

/*CONTROL*/
    input clk;
    input [7:0]opmode;

/*ENABLE*/
    input cea,ceb,cec,cecarryin,ced,cem,ceopmode,cep; //cecarryin for carry in/out

/*RESET*/
    input rsta,rstb,rstc,rstcarryin,rstd,rstm,rstopmode,rstp; //same in rstcarryin
```

```
/*RESET*/
    input rsta,rstb,rstc,rstcarryin,rstd,rstm,rstopmode,rstp; //same in rstcarryin

/*CASCADE*/
    input [17:0]bcin;
    output [17:0]bcout;
    input [47:0]pcin;
    output [47:0]pcout;

//WIRES
    wire [17:0]wa0,wa1,wb0,wb1,wd;
    wire [47:0]wc;
    wire wcarryin;
    wire [7:0]wopmode;
    wire [17:0] Pre_Adder_Subtractor;
    wire [47:0] Post_Adder_Subtractor;
    wire wcarryout_prev;
    wire [35:0] wm;
    wire [17:0] b00;
    wire carryin00;

    wire [35:0] wm00;
    assign wm00=(wa1 * wb1);

//SELECTIONS
    reg [47:0] X,Z;

//INSTATIATION
    //DSP48A1_Project_reg #(.WIDTH(), .REGISTER(), .RSTTYPE()) dut (clk,enable,rst,in,out);
    DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(A0REG), .RSTTYPE(RSTTYPE)) duta0 (clk,cea,rsta,a,wa0);
    DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(A1REG), .RSTTYPE(RSTTYPE)) duta1 (clk,cea,rsta,wa0,wa1);
    DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(B0REG), .RSTTYPE(RSTTYPE)) dutb0 (clk,ceb,rstb,b00,wb0);
    DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(B1REG), .RSTTYPE(RSTTYPE)) dutb1 (clk,ceb,rstb,((wopmode[4])?Pre_Adder_Subtractor:wb0),wb1);
    DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(DREG), .RSTTYPE(RSTTYPE)) dutd (clk,ced,rstd,d,wd);
    DSP48A1_Project_reg #(.WIDTH(48), .REGISTER(CREG), .RSTTYPE(RSTTYPE)) dutc (clk,cec,rstc,c,wc);
    DSP48A1_Project_reg #(.WIDTH(1), .REGISTER(CARRYINREG), .RSTTYPE(RSTTYPE)) dutcarryin (clk,cecarryin,rstcarryin,carryin00,wcarryin);
    DSP48A1_Project_reg #(.WIDTH(36), .REGISTER(MREG), .RSTTYPE(RSTTYPE)) dutm (clk,cem,rstm,wm00,wm);
```

```
59
60  //SELECTIONS
61      reg [47:0] X,Z;
62
63  //INSTATIATION
64      //DSP48A1_Project_reg #(.WIDTH(), .REGISTER(), .RSTTYPE()) dut (clk,enable,rst,in,out);
65      DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(A0REG), .RSTTYPE(RSTTYPE)) duta0 (clk,cea,rsta,a,wa0);
66      DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(A1REG), .RSTTYPE(RSTTYPE)) duta1 (clk,cea,rsta,wa0,wa1);
67      DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(B0REG), .RSTTYPE(RSTTYPE)) dutb0 (clk,ceb,rstb,b00,wb0);
68      DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(B1REG), .RSTTYPE(RSTTYPE)) dutb1 (clk,ceb,rstb,((wopmode[4])?Pre_Adder_Subtractor:wb0),wb1);
69      DSP48A1_Project_reg #(.WIDTH(18), .REGISTER(DREG), .RSTTYPE(RSTTYPE)) dutd (clk,ced,rstd,d,wd);
70      DSP48A1_Project_reg #(.WIDTH(48), .REGISTER(CREG), .RSTTYPE(RSTTYPE)) dutc (clk,cec,rstc,c,wc);
71      DSP48A1_Project_reg #(.WIDTH(1), .REGISTER(CARRYINREG), .RSTTYPE(RSTTYPE)) dutcarryin (clk,cecarryin,rstcarryin,carryin00,wcarryin);
72      DSP48A1_Project_reg #(.WIDTH(36), .REGISTER(MREG), .RSTTYPE(RSTTYPE)) dutm (clk,cem,rstm,wm00,wm);
73      DSP48A1_Project_reg #(.WIDTH(8), .REGISTER(OPMODEREG), .RSTTYPE(RSTTYPE)) dutopmode (clk,ceopmode,rstopmode,opmode,wopmode);
74      DSP48A1_Project_reg #(.WIDTH(48), .REGISTER(PREG), .RSTTYPE(RSTTYPE)) dutP (clk,cep,rstp,Post_Adder_Subtractor,p);
75      DSP48A1_Project_reg #(.WIDTH(1), .REGISTER(CARRYOUTREG), .RSTTYPE(RSTTYPE)) dutacarryout (clk,cecarryin,rstcarryin,wcarryout_prev,carryout);
76
77      assign b00=(B_INPUT=="DIRECT")? b:(B_INPUT=="CASCADE")? bcin: 0;
78      assign carryin00=(CARRYINSEL=="OPMODE5")? wopmode[5]:(CARRYINSEL=="CARRYIN")? carryin: 0;
79  //Pre_Adder_Subtractor
80      assign Pre_Adder_Subtractor=(wopmode[6])?(wd - wb0):(wd + wb0);
81  //Post_Adder_Subtractor
82      assign {wcarryout_prev,Post_Adder_Subtractor}=(wopmode[7])?(Z - (X + wcarryin)):(Z + X + wcarryin);
83      assign carryoutf=carryout;
84      assign pcout=p;
85      assign bcout=wb1;
86  //m_buffer
87      genvar i;
88      generate
89          for (i = 0;i <36;i=i+1) begin
90              buf (m[i],wm[i]);
91          end
92      endgenerate
93
94  //X
95      always @(*) begin
```

```
86  //m_buffer
87      genvar i;
88      generate
89          for (i = 0;i <36;i=i+1) begin
90              buf (m[i],wm[i]);
91          end
92      endgenerate
93
94  //X
95      always @(*) begin
96          case (wopmode[1:0])
97              2'b00:X=0;
98              2'b01:X=wm;
99              2'b10:X=p;
100             2'b11:X={d[11:0],a[17:0],b[17:0]};
101         endcase
102     end
103 //Z
104     always @(*) begin
105         case (wopmode[3:2])
106             2'b00:Z=0;
107             2'b01:Z=pcin;
108             2'b10:Z=p;
109             2'b11:Z=wc;
110         endcase
111     end
112
113 endmodule
```

The instantiated code:

DSP48A1_Project_reg.v | DSP48A1_Project.v | DSP48A1_Project_tb.v

```
module DSP48A1_Project_reg (clk,enable,rst,in,out);

    parameter REGISTER=1; //1 reg, 0 no reg
    parameter RSTTYPE="SYNC";
    parameter WIDTH=18;

    input clk,enable,rst;
    input [WIDTH-1:0] in;
    output reg [WIDTH-1:0] out;

    generate
        if (REGISTER==0) begin
            always @(*) begin
                out=in;
            end
        end
        else if (RSTTYPE=="ASYNC") begin
            always @(posedge clk or posedge rst) begin
                if(rst) begin
                    out<=0;
                end
                else if (enable) begin
                    out<=in;
                end
            end
        end
        else begin
            always @(posedge clk) begin
                if(enable) begin
                    if (rst) begin
                        out<=0;
                    end
                    else begin
                        out<=in;
                    end
                end
            end
        end
    endgenerate

endmodule
```

Testbench:

```
module DSP48A1_Project_tb ();
    reg [17:0]a,b,d;
    reg [47:0]c;
    reg carryin;
    wire [35:0]m;
    wire [47:0]p;
    wire carryout,carryoutf;
    reg clk;
    reg [7:0]opmode;
    reg cea,ceb,cec,cecarryin,ced,cem,ceopmode,cep; //cecarryin for carry in/out
    reg rsta,rstb,rstc,rstcarryin,rstd,rstm,rstopmode,rstp; //same in rstcarryin
    reg [17:0]bcin; //forgot bcin
    wire [17:0]bcout;
    reg [47:0]pcin;
    wire [47:0]pcout;

    reg [47:0]p_ex;
    reg [47:0]pcout_ex;
    reg [35:0]m_ex;
    reg [17:0]bcout_ex;
    reg carryout_ex;
    reg carryoutf_ex;

    reg [2:0] iteration;

    DSP48A1_Project tb0 (a,b,d,c,carryin,m,p,carryout,carryoutf,clk,opmode,cea,ceb,cec,cecarryin,ced,cem,ceopmode,cep,rsta,rstb,rstc,rstca

    initial begin
        clk=0;
        forever
        #2 clk=~clk;
    end

    initial begin
//0
```

```
    initial begin
//0
        iteration=0;
        rsta=1;rstb=1;rstc=1;rstcarryin=1;rstd=1;rstm=1;rstopmode=1;rstp=1;
        cea=1;ceb=1;cec=1;cecarryin=1;ced=1;cem=1;ceopmode=1;cep=1;
        a=1;b=10;d=100;c=400;carryin=0;opmode=8'b0011_0001;bcin=5000;pcin=2500;
        p_ex=0;pcout_ex=0;m_ex=0;bcout_ex=0;carryout_ex=0;carryoutf_ex=0;
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        if ((p_ex!=p)||(pcout_ex!=pcout)||(m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
//1
        iteration=1;
        rsta=0;rstb=0;rstc=0;rstcarryin=0;rstd=0;rstm=0;rstopmode=0;rstp=0;
        cea=1;ceb=1;cec=1;cecarryin=1;ced=1;cem=1;ceopmode=1;cep=1;
        a=10;b=100;d=1000;c=4000;carryin=0;opmode=8'b0011_0001;bcin=500;pcin=250;
        p_ex=11001;pcout_ex=11001;m_ex=11000;bcout_ex=1100;carryout_ex=0;carryoutf_ex=0;
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        if ((p_ex!=p)||(pcout_ex!=pcout)||(m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
//2
```

```
            $stop;
        end
//2
        iteration=2;
        rsta=0;rstb=0;rstc=0;rstcarryin=0;rstd=0;rstm=0;rstopmode=0;rstp=0;
        cea=1;ceb=1;cec=1;cecarryin=1;ced=1;cem=1;ceopmode=1;cep=1;
        a=1;b=10;d=100;c=400;carryin=0;opmode=8'b0011_0110;bcin=5000;pcin=2500;
        p_ex=13502/*pcin+p*/;pcout_ex=13502;m_ex=110;bcout_ex=110;carryout_ex=0;carryoutf_ex=0;
        @(negedge clk);
        @(negedge clk);
        if ((p_ex!=p)||(pcout_ex!=pcout)) begin //because P will continue to add with each clock cycle and m will not reach its real value
            $display("error");
            $stop;
        end
        @(negedge clk);
        if ((m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
//3
        iteration=3;
        rsta=0;rstb=0;rstc=0;rstcarryin=0;rstd=0;rstm=0;rstopmode=0;rstp=0;
        cea=1;ceb=1;cec=1;cecarryin=1;ced=1;cem=1;ceopmode=1;cep=1;
        a=500;b=120;d=1050;c=16000;carryin=0;opmode=8'b0101_1101;bcin=8000;pcin=5200;
        p_ex=481000/*c+m*/;pcout_ex=481000;m_ex=465000;bcout_ex=930/*d-b*/;carryout_ex=0;carryoutf_ex=0;
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        if ((p_ex!=p)||(pcout_ex!=pcout)||(m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
```

```
            $stop;
        end
//4
        iteration=4;
        rsta=0;rstb=0;rstc=0;rstcarryin=0;rstd=0;rstm=0;rstopmode=0;rstp=0;
        cea=1;ceb=1;cec=1;cecarryin=1;ced=1;cem=1;ceopmode=1;cep=1;
        a=1;b=120;d=0;c=16000;carryin=0;opmode=8'b0110_0111;bcin=8000;pcin=5200;
        p_ex=19'b1000001010011001001/*pcin+{D:A:B}+opmode5*/;pcout_ex=19'b1000001010011001001;m_ex=120/*b*A*/;bcout_ex=120/*b*/;
        carryout_ex=0;carryoutf_ex=0;
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        if ((p_ex!=p)||(pcout_ex!=pcout)||(m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
//5
        iteration=5;
        rsta=0;rstb=0;rstc=0;rstcarryin=0;rstd=0;rstm=0;rstopmode=0;rstp=0;
        cea=1;ceb=1;cec=1;cecarryin=1;ced=1;cem=1;ceopmode=1;cep=1;
        a=500;b=120;d=1050;c=16000;carryin=0;opmode=8'b0011_0000;bcin=8000;pcin=5200;
        p_ex=1/*opcode5*/;pcout_ex=1;m_ex=585000;bcout_ex=1170/*d-b*/;carryout_ex=0;carryoutf_ex=0;
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        if ((p_ex!=p)||(pcout_ex!=pcout)||(m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
```

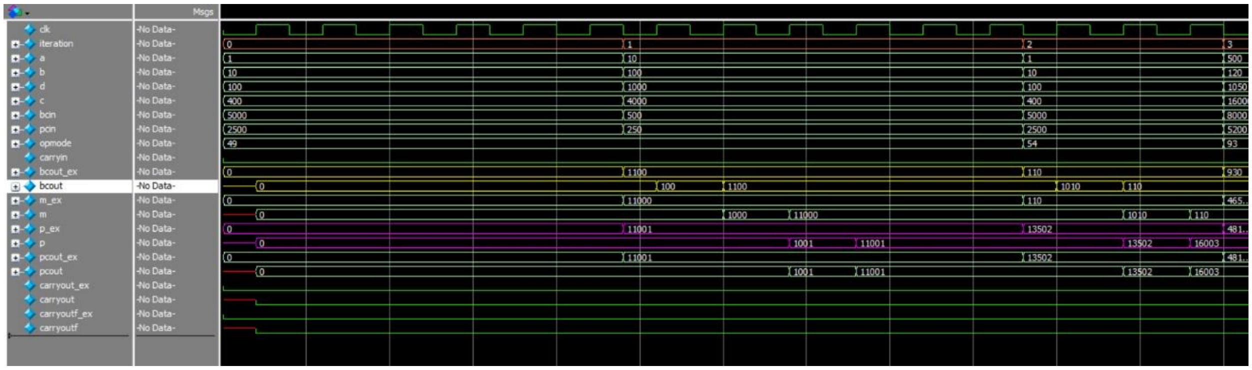
```
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        @(negedge clk);
        if ((p_ex!=p)||(pcout_ex!=pcout)||(m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
//6
        iteration=6;
        rsta=0;rstb=0;rstc=0;rstcarryin=0;rstd=0;rstm=0;rstopmode=0;rstp=0;
        cea=1;ceb=1;cec=1;cecarryin=1;ced=1;cem=1;ceopmode=1;cep=1;
        a=500;b=120;d=1050;c=16000;carryin=0;opmode=8'b0011_1010;bcin=8000;pcin=5200;
        p_ex=3/*p+p+opmode5*/;pcout_ex=3;m_ex=585000;bcout_ex=1170/*d-b*/;carryout_ex=0;carryoutf_ex=0;
        @(negedge clk);
        @(negedge clk); // no problem here because m still at the same value from the previous iteration
        if ((p_ex!=p)||(pcout_ex!=pcout)||(m_ex!=m)||(bcout_ex!=bcout)||(carryout_ex!=carryout)||(carryoutf_ex!=carryoutf)) begin
            $display("error");
            $stop;
        end
        $stop;
    end

    initial begin
        $monitor("iteration=%d,bcout=%d ,bcout_ex=%d ,m=%d ,m_ex=%d ,p=%d ,p_ex=%d ,pcout=%d ,pcout_ex=%d ,carryout=%d ,carryout_ex=%d",ite
    end

endmodule
```

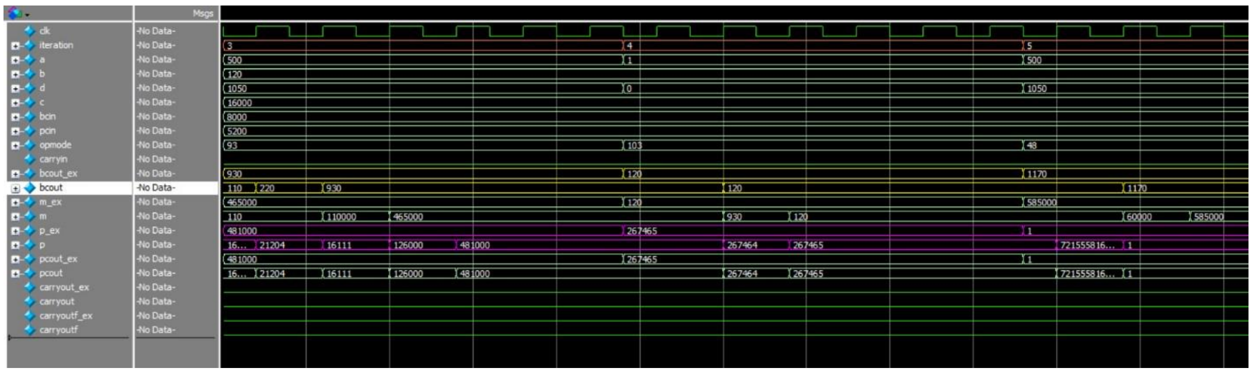
Run.do File:

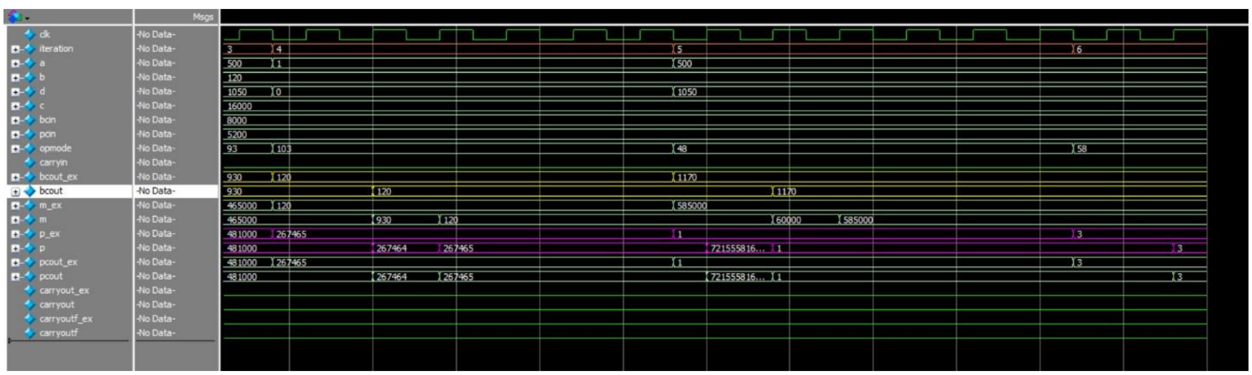
DSP48A1_Project_reg.v | DSP48A1_Project.v | DSP48A1_Project_tb.v | run_DSP.do

```
vlib work
vlog DSP48A1_Project_reg.v DSP48A1_Project.v DSP48A1_Project_tb.v
vsim -voptargs=+acc work.DSP48A1_Project_tb
add wave *
run -all
#quit -sim
```

Waveform: (removed all clock enables and resets)







Data from monitor:

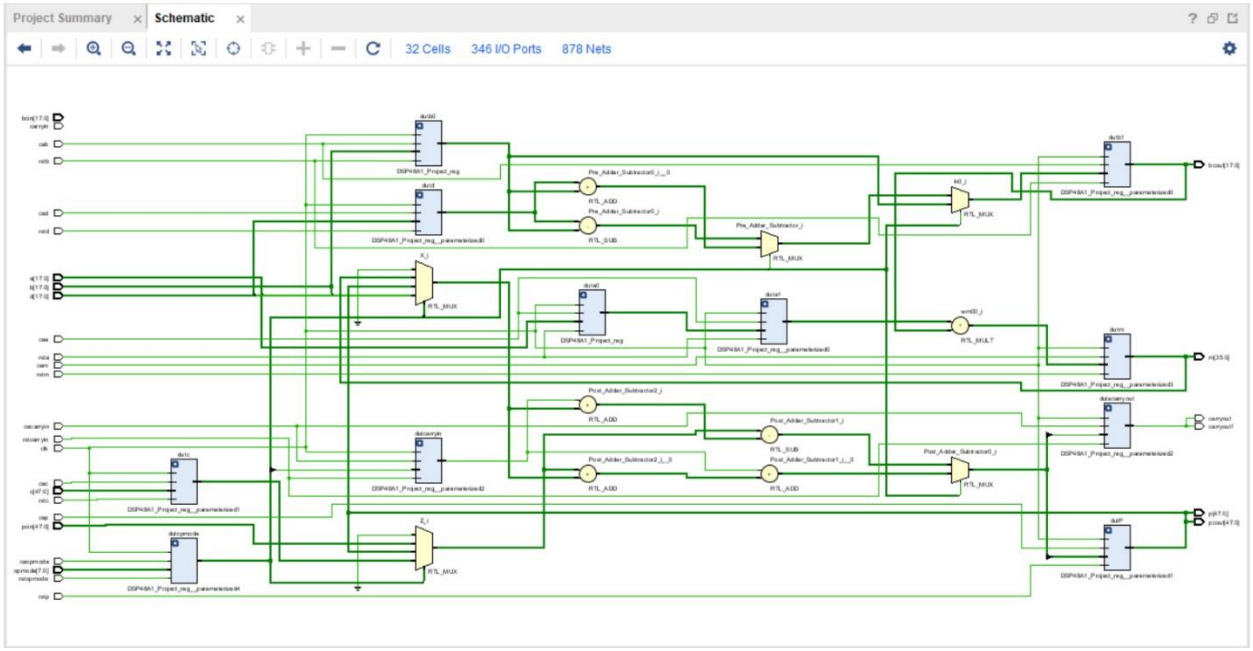
```
# Loading work.DSP48A1_Project_reg(fast__3)
# Loading work.DSP48A1_Project_reg(fast__4)
# Loading work.DSP48A1_Project_reg(fast__5)
# iteration= 0,bcout=     x ,bcout_ex=     0 ,m=         x ,m_ex=         0 ,p=             x ,p_ex=             0 ,pcout=             x ,pcout_ex=             0 ,carryout=x ,carryout_ex=0
# iteration= 0,bcout=     0 ,bcout_ex=     0 ,m=         0 ,m_ex=         0 ,p=             0 ,p_ex=             0 ,pcout=             0 ,pcout_ex=             0 ,carryout=0 ,carryout_ex=0
# iteration= 1,bcout=     0 ,bcout_ex=  1100 ,m=         0 ,m_ex=     11000 ,p=             0 ,p_ex=         11001 ,pcout=             0 ,pcout_ex=         11001 ,carryout=0 ,carryout_ex=0
# iteration= 1,bcout=   100 ,bcout_ex=  1100 ,m=         0 ,m_ex=     11000 ,p=             0 ,p_ex=         11001 ,pcout=             0 ,pcout_ex=         11001 ,carryout=0 ,carryout_ex=0
# iteration= 1,bcout=  1100 ,bcout_ex=  1100 ,m=      1000 ,m_ex=     11000 ,p=             0 ,p_ex=         11001 ,pcout=             0 ,pcout_ex=         11001 ,carryout=0 ,carryout_ex=0
# iteration= 1,bcout=  1100 ,bcout_ex=  1100 ,m=     11000 ,m_ex=     11000 ,p=          1001 ,p_ex=         11001 ,pcout=          1001 ,pcout_ex=         11001 ,carryout=0 ,carryout_ex=0
# iteration= 1,bcout=  1100 ,bcout_ex=  1100 ,m=     11000 ,m_ex=     11000 ,p=         11001 ,p_ex=         11001 ,pcout=         11001 ,pcout_ex=         11001 ,carryout=0 ,carryout_ex=0
# iteration= 2,bcout=  1100 ,bcout_ex=   110 ,m=     11000 ,m_ex=       110 ,p=         11001 ,p_ex=         13502 ,pcout=         11001 ,pcout_ex=         13502 ,carryout=0 ,carryout_ex=0
# iteration= 2,bcout=  1010 ,bcout_ex=   110 ,m=     11000 ,m_ex=       110 ,p=         11001 ,p_ex=         13502 ,pcout=         11001 ,pcout_ex=         13502 ,carryout=0 ,carryout_ex=0
# iteration= 2,bcout=   110 ,bcout_ex=   110 ,m=      1010 ,m_ex=       110 ,p=         13502 ,p_ex=         13502 ,pcout=         13502 ,pcout_ex=         13502 ,carryout=0 ,carryout_ex=0
# iteration= 2,bcout=   110 ,bcout_ex=   110 ,m=       110 ,m_ex=       110 ,p=         16003 ,p_ex=         13502 ,pcout=         16003 ,pcout_ex=         13502 ,carryout=0 ,carryout_ex=0
# iteration= 3,bcout=   110 ,bcout_ex=   930 ,m=       110 ,m_ex=    465000 ,p=         16003 ,p_ex=        481000 ,pcout=         16003 ,pcout_ex=        481000 ,carryout=0 ,carryout_ex=0
# iteration= 3,bcout=   220 ,bcout_ex=   930 ,m=       110 ,m_ex=    465000 ,p=         21204 ,p_ex=        481000 ,pcout=         21204 ,pcout_ex=        481000 ,carryout=0 ,carryout_ex=0
# iteration= 3,bcout=   930 ,bcout_ex=   930 ,m=    110000 ,m_ex=    465000 ,p=         16111 ,p_ex=        481000 ,pcout=         16111 ,pcout_ex=        481000 ,carryout=0 ,carryout_ex=0
# iteration= 3,bcout=   930 ,bcout_ex=   930 ,m=    465000 ,m_ex=    465000 ,p=        126000 ,p_ex=        481000 ,pcout=        126000 ,pcout_ex=        481000 ,carryout=0 ,carryout_ex=0
# iteration= 3,bcout=   930 ,bcout_ex=   930 ,m=    465000 ,m_ex=    465000 ,p=        481000 ,p_ex=        481000 ,pcout=        481000 ,pcout_ex=        481000 ,carryout=0 ,carryout_ex=0
# iteration= 4,bcout=   930 ,bcout_ex=   120 ,m=    465000 ,m_ex=       120 ,p=        481000 ,p_ex=        267465 ,pcout=        481000 ,pcout_ex=        267465 ,carryout=0 ,carryout_ex=0
# iteration= 4,bcout=   120 ,bcout_ex=   120 ,m=       930 ,m_ex=       120 ,p=        267464 ,p_ex=        267465 ,pcout=        267464 ,pcout_ex=        267465 ,carryout=0 ,carryout_ex=0
# iteration= 4,bcout=   120 ,bcout_ex=   120 ,m=       120 ,m_ex=       120 ,p=        267465 ,p_ex=        267465 ,pcout=        267465 ,pcout_ex=        267465 ,carryout=0 ,carryout_ex=0
# iteration= 5,bcout=   120 ,bcout_ex=  1170 ,m=       120 ,m_ex=    585000 ,p=        267465 ,p_ex=             1 ,pcout=        267465 ,pcout_ex=             1 ,carryout=0 ,carryout_ex=0
# iteration= 5,bcout=   120 ,bcout_ex=  1170 ,m=       120 ,m_ex=    585000 ,p= 72155581650121 ,p_ex=             1 ,pcout= 72155581650121 ,pcout_ex=             1 ,carryout=0 ,carryout_ex=0
# iteration= 5,bcout=  1170 ,bcout_ex=  1170 ,m=     60000 ,m_ex=    585000 ,p=             1 ,p_ex=             1 ,pcout=             1 ,pcout_ex=             1 ,carryout=0 ,carryout_ex=0
# iteration= 5,bcout=  1170 ,bcout_ex=  1170 ,m=    585000 ,m_ex=    585000 ,p=             1 ,p_ex=             1 ,pcout=             1 ,pcout_ex=             1 ,carryout=0 ,carryout_ex=0
# iteration= 6,bcout=  1170 ,bcout_ex=  1170 ,m=    585000 ,m_ex=    585000 ,p=             1 ,p_ex=             3 ,pcout=             1 ,pcout_ex=             3 ,carryout=0 ,carryout_ex=0
# iteration= 6,bcout=  1170 ,bcout_ex=  1170 ,m=    585000 ,m_ex=    585000 ,p=             3 ,p_ex=             3 ,pcout=             3 ,pcout_ex=             3 ,carryout=0 ,carryout_ex=0
# ** Note: $stop    : DSP48A1_Project_tb.v(144)
#    Time: 140 ns  Iteration: 1  Instance: /DSP48A1_Project_tb
# Break in Module DSP48A1_Project_tb at DSP48A1_Project_tb.v line 144
```

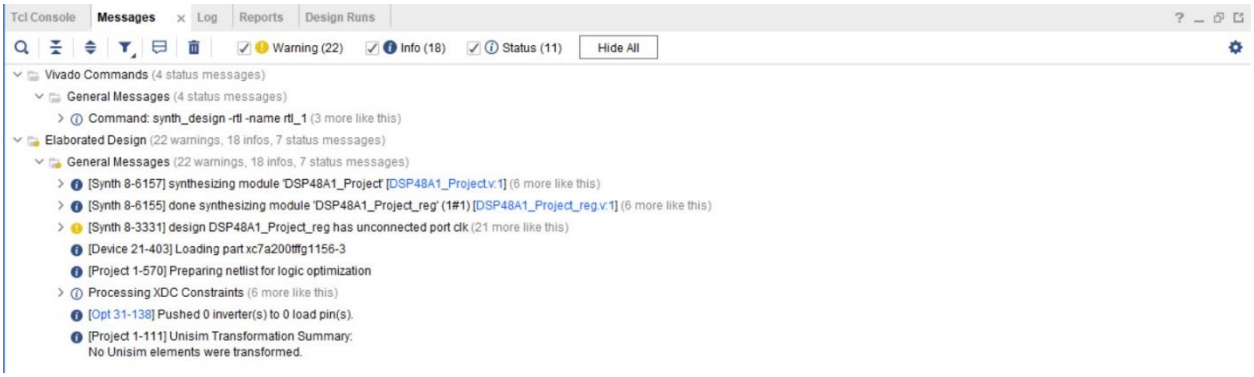
Constraint File:

```
4  ## - rename the used ports (in each line, after get_ports) according to the top level signal nam
5
6  # Clock signal
7  set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10
11 ## Switches
```

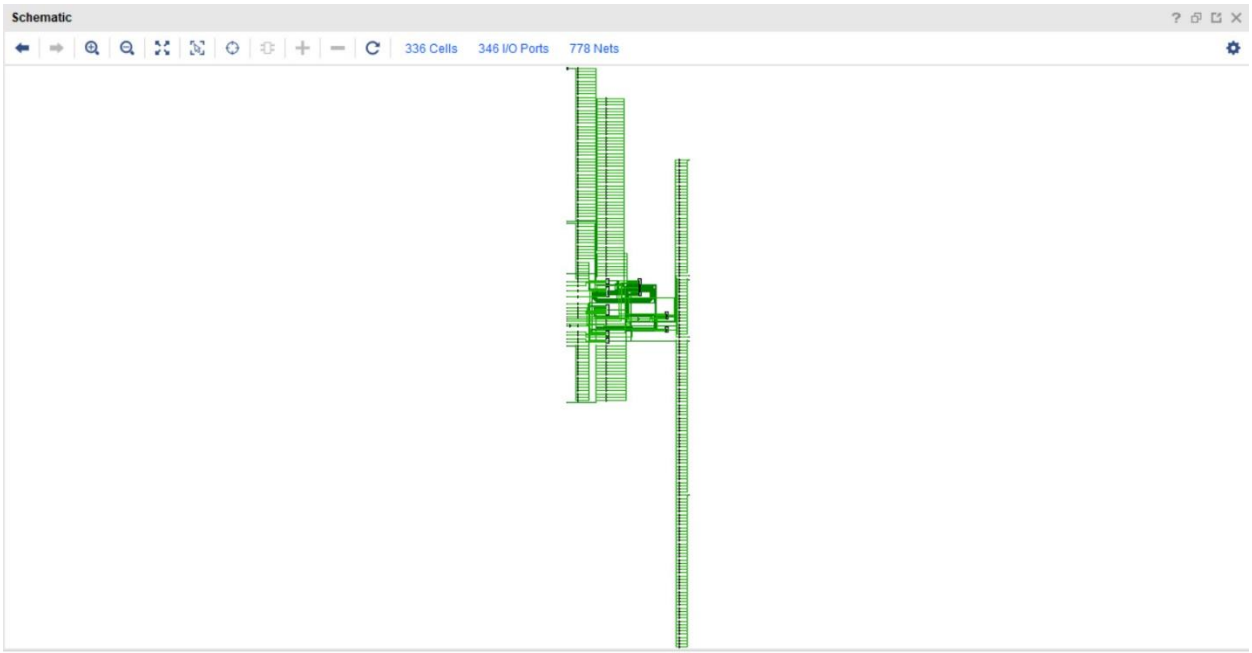
```
159 set_property CONFIG_MODE SPIx4 [current_design]
160
161 create_debug_core u_ila_0 ila
162 set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
163 set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
164 set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
165 set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
166 set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
167 set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
168 set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
169 set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
170 set_property port_width 1 [get_debug_ports u_ila_0/clk]
171 connect_debug_port u_ila_0/clk [get_nets [list clk_IBUF_BUFG]]
172 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
173 set_property port_width 8 [get_debug_ports u_ila_0/probe0]
174 connect_debug_port u_ila_0/probe0 [get_nets [list {opmode_IBUF[0]} {opmode_IBUF[1]} {opmode_IBUF[2]} {opmo
175 create_debug_port u_ila_0 probe
176 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
177 set_property port_width 48 [get_debug_ports u_ila_0/probe1]
178 connect_debug_port u_ila_0/probe1 [get_nets [list {pcin_IBUF[0]} {pcin_IBUF[1]} {pcin_IBUF[2]} {pcin_IBUF[
179 create_debug_port u_ila_0 probe
180 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
```

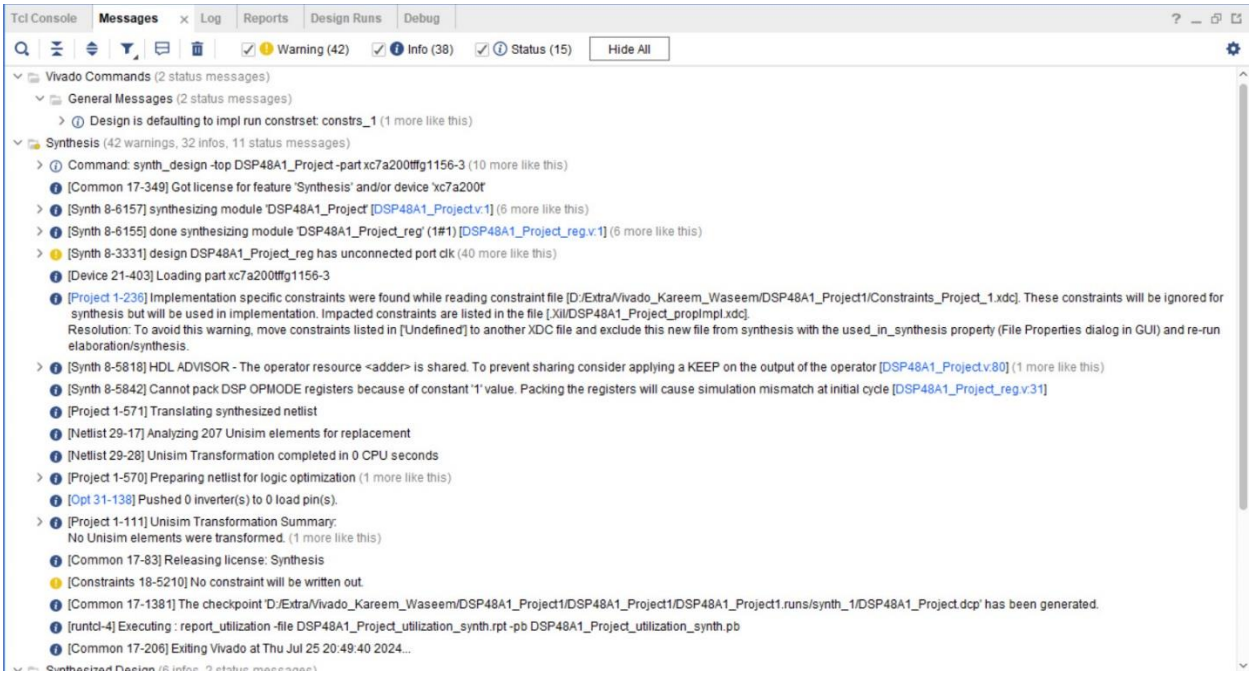
Elaboration:

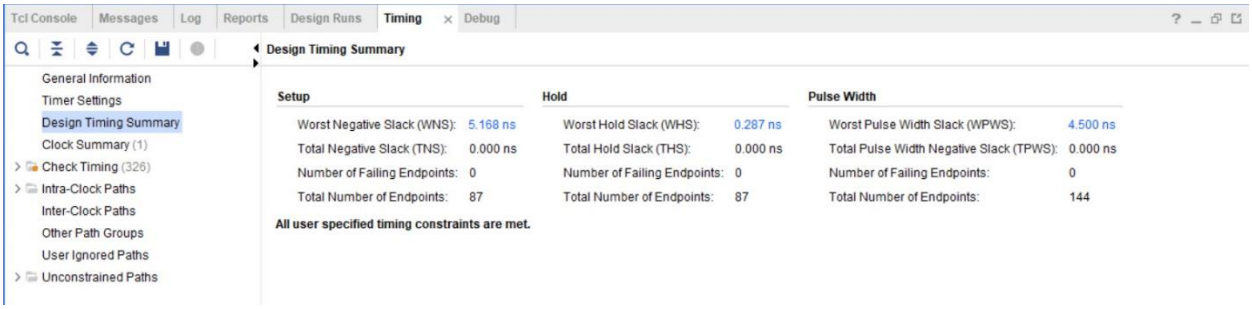


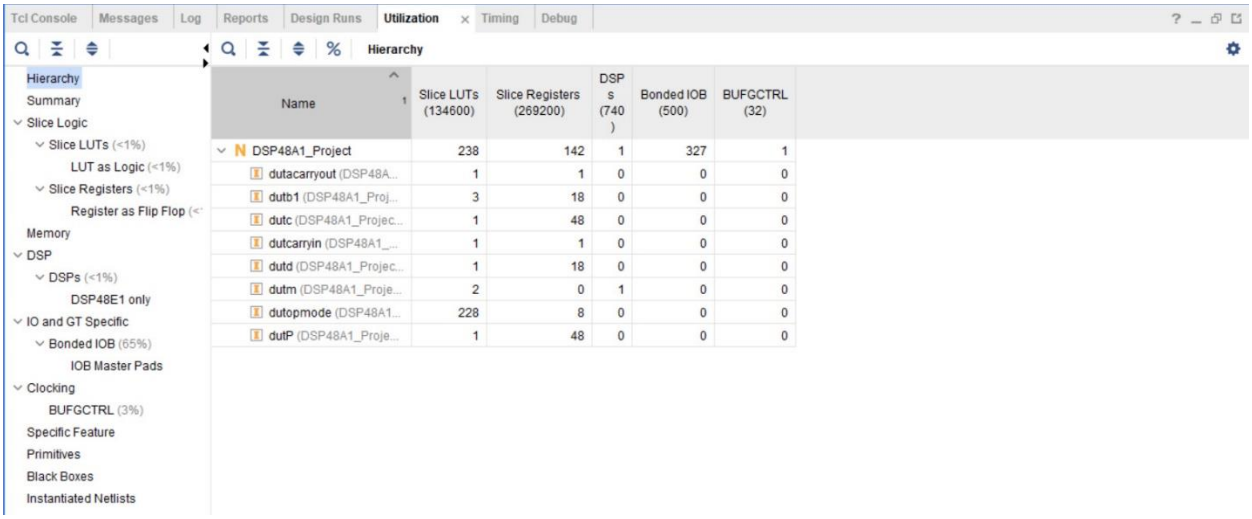


Synthesis:

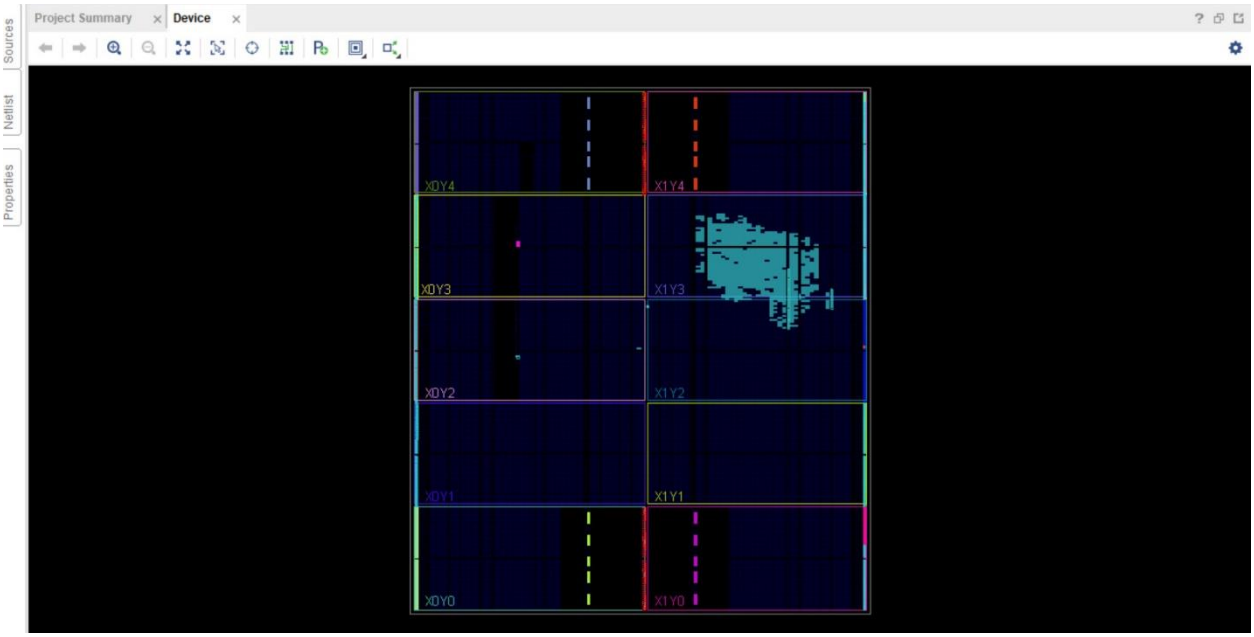

Schematic
336 Cells
346 I/O Ports
778 Nets

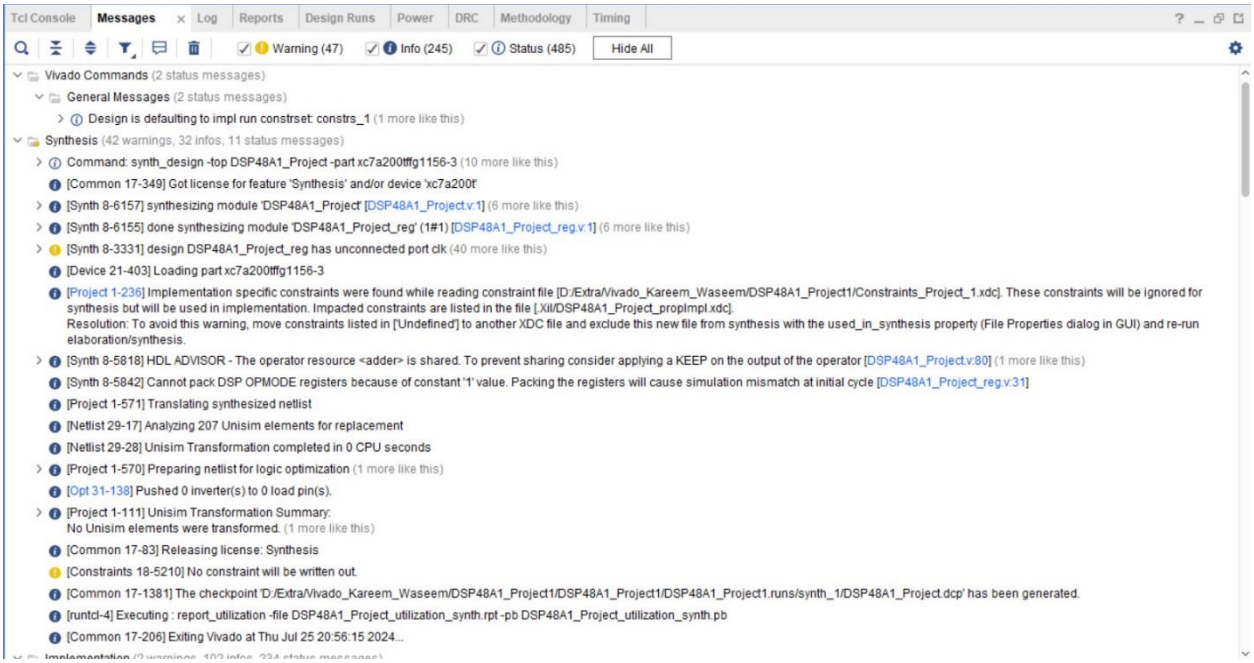

Tcl Console
Messages
Log
Reports
Design Runs
Debug
Warning (42)
Info (38)
Status (15)
Hide All
Vivado Commands (2 status messages)
General Messages (2 status messages)
Design is defaulting to impl run constrset: constrs_1 (1 more like this)
Synthesis (42 warnings, 32 infos, 11 status messages)
Command: synth_design -top DSP48A1_Project -part xc7a200tffg1156-3 (10 more like this)
[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
[Synth 8-6157] synthesizing module 'DSP48A1_Project' [DSP48A1_Project.v:1] (6 more like this)
[Synth 8-6155] done synthesizing module 'DSP48A1_Project_reg' (1#1) [DSP48A1_Project_reg.v:1] (6 more like this)
[Synth 8-3331] design DSP48A1_Project_reg has unconnected port clk (40 more like this)
[Device 21-403] Loading part xc7a200tffg1156-3
[Project 1-236] Implementation specific constraints were found while reading constraint file [D:/Extra/Vivado_Kareem_Waseem/DSP48A1_Project1/Constraints_Project_1.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/DSP48A1_Project_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
[Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [DSP48A1_Project.v:80] (1 more like this)
[Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [DSP48A1_Project_reg.v:31]
[Project 1-571] Translating synthesized netlist
[Netlist 29-17] Analyzing 207 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-570] Preparing netlist for logic optimization (1 more like this)
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
[Common 17-83] Releasing license: Synthesis
[Constraints 18-5210] No constraint will be written out.
[Common 17-1381] The checkpoint 'D:/Extra/Vivado_Kareem_Waseem/DSP48A1_Project1/DSP48A1_Project1/DSP48A1_Project1.runs/synth_1/DSP48A1_Project.dcp' has been generated.
[runtcl-4] Executing : report_utilization -file DSP48A1_Project_utilization_synth.rpt -pb DSP48A1_Project_utilization_synth.pb
[Common 17-206] Exiting Vivado at Thu Jul 25 20:49:40 2024...

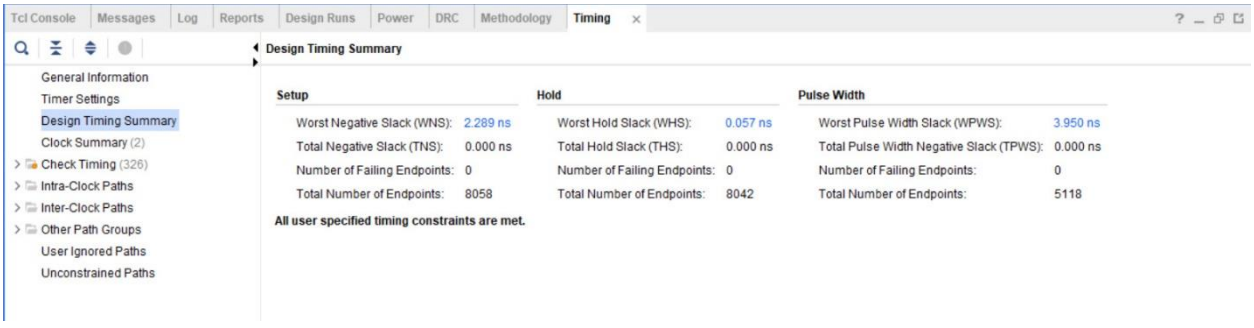

Tcl Console
Messages
Log
Reports
Design Runs
Timing
Debug
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Setup
Worst Negative Slack (WNS): 5.168 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87
Hold
Worst Hold Slack (WHS): 0.287 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 144
All user specified timing constraints are met.

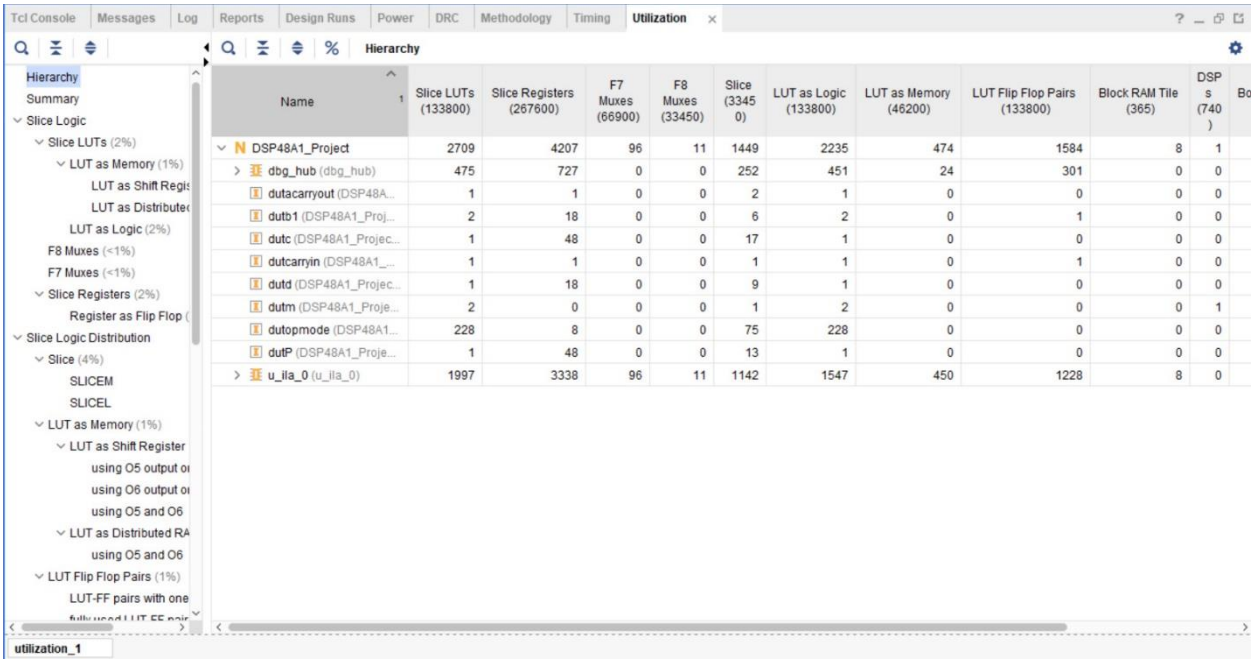

Tcl Console
Messages
Log
Reports
Design Runs
Utilization
Timing
Debug
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop (<
Memory
DSP
DSPs (<1%)
DSP48E1 only
IO and GT Specific
Bonded IOB (65%)
IOB Master Pads
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
Instantiated Netlists
Name
Slice LUTs (134600)
Slice Registers (269200)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
DSP48A1_Project 238 142 1 327 1
dutacarryout (DSP48A... 1 1 0 0 0
dutb1 (DSP48A1_Proj... 3 18 0 0 0
dutc (DSP48A1_Projec... 1 48 0 0 0
dutcarryin (DSP48A1_... 1 1 0 0 0
dutd (DSP48A1_Projec... 1 18 0 0 0
dutm (DSP48A1_Proje... 2 0 1 0 0
dutopmode (DSP48A1... 228 8 0 0 0
dutP (DSP48A1_Proje... 1 48 0 0 0

Implementation:









Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)	Bo
DSP48A1_Project	2709	4207	96	11	1449	2235	474	1584	8	1	
dbg_hub (dbg_hub)	475	727	0	0	252	451	24	301	0	0	
dutacarryout (DSP48A...	1	1	0	0	2	1	0	0	0	0	
dutb1 (DSP48A1_Proj...	2	18	0	0	6	2	0	1	0	0	
dutc (DSP48A1_Projec...	1	48	0	0	17	1	0	0	0	0	
dutcarryin (DSP48A1_...	1	1	0	0	1	1	0	1	0	0	
dutd (DSP48A1_Projec...	1	18	0	0	9	1	0	0	0	0	
dutm (DSP48A1_Proje...	2	0	0	0	1	2	0	0	0	1	
dutopmode (DSP48A1...	228	8	0	0	75	228	0	0	0	0	
dutP (DSP48A1_Proje...	1	48	0	0	13	1	0	0	0	0	
u_ila_0 (u_ila_0)	1997	3338	96	11	1142	1547	450	1228	8	0	