

SPI Slave with Single Port RAM

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Overview

- Objective

To design and implement an SPI communication protocol in Verilog HDL. The system features an SPI master, an integrated SPI wrapper module that combines the SPI slave and RAM functionalities.

- Applications

An SPI Slave with Single Port RAM is useful for applications in embedded systems, industrial automation, consumer electronics, IoT devices, networking, medical devices, memory expansion, and data storage. It provides efficient communication, real-time data buffering, and temporary storage in low-power, constrained environments.

- System Design

1. SPI Slave Module

Manages communication with the master device using the SPI protocol, receiving and transmitting data to and from the RAM module.

2. Single Port RAM Module

Provides memory storage, allowing for efficient read/write operations of data received via the SPI interface.

3. SPI Wrapper Module

Integrates the SPI Slave and RAM, managing data flow and ensuring seamless communication between them.

RTL design

- SPI slave

```
1 module SPI_Slave (mosi, ss_n, clk, rst_n, tx_valid, tx_data, miso, rx_valid, rx_data);
2
3 //State parameters
4 parameter IDLE=0;
5 parameter CHK_CMD=1;
6 parameter WRITE=2;
7 parameter READ_ADD=3;
8 parameter READ_DATA=4;
9
10 //Input ports
11 input mosi; //Master_out_slave_in input
12 input ss_n, clk, rst_n, tx_valid; //Control input signals
13 input[7:0] tx_data; //The parallel data sent from the RAM to SPI
14
15 //Output ports
16 output reg miso; //Master_in_slave_out output
17 output reg rx_valid; //Control signal
18 output reg[9:0] rx_data; //The parallel data sent to RAM
19
20 //Internal signals
21 reg[3:0] counter, counter_rd_data; //Counter for serial / parallel tranformations
22 reg[2:0] cs, ns; //State registers
23 reg end_counter_rd_data; //Internal control signals
24
25 //State memory
26 always @(posedge clk) begin
27     if(~rst_n)
28         cs<=IDLE;
29     else
30         cs<=ns;
31 end
```

```
32
33 //Next state combinational logic
34 always @(*) begin
35     case (cs)
36         IDLE: begin
37             if (ss_n == 0)
38                 ns = CHK_CMD;
39             else
40                 ns = IDLE;
41         end
42         CHK_CMD: begin
43             if ((ss_n == 0) && rx_valid && (rx_data[9] == 0))
44                 ns = WRITE;
45             else if ((ss_n == 0) && rx_valid && (rx_data[9:8] == 2'b10))
46                 ns = READ_ADD;
47             else if ((ss_n == 0) && rx_valid && (rx_data[9:8] == 2'b11))
48                 ns = READ_DATA;
49             else if (rx_valid == 0)
50                 ns = CHK_CMD;
51             else
52                 ns = IDLE;
53         end
54         WRITE: begin
55             if (ss_n == 1)
56                 ns = IDLE;
57             else
58                 ns = WRITE;
59         end
```

```
60     end
61     READ_ADD: begin
62         if (ss_n == 1)
63             ns = IDLE;
64         else
65             ns = READ_ADD;
66     end
67     READ_DATA: begin
68         if (ss_n == 1)
69             ns = IDLE;
70         else
71             ns = READ_DATA;
72     end
73     default: ns = IDLE;
74 endcase
75 end
```

```

75
76 //Serial mosi to parallel rx_data (from SPI to RAM)
77 always @(posedge clk) begin
78     if(~rst_n) begin
79         rx_data <= 0;
80         counter <= 0;
81         rx_valid <= 0;
82     end
83     else if (counter >= 10) begin
84         counter <= 0;
85         rx_valid <= 1;
86     end
87     else if((cs == CHK_CMD) && !rx_valid) begin
88         rx_data[9-counter] <= mosi;
89         counter <= counter + 1;
90     end
91     else if (cs == IDLE)
92         rx_valid <= 0;
93 end
94

```

```

94
95 //Parallel tx_data to serial miso (read data from RAM to SPI)
96 always @(posedge clk) begin
97     if(~rst_n) begin
98         miso <= 0;
99         counter_rd_data <= 0;
100         end_counter_rd_data <= 0;
101     end
102     else if (counter_rd_data >= 8) begin
103         counter_rd_data <= 0;
104         end_counter_rd_data <= 1;
105     end
106     else if ((cs == READ_DATA) && tx_valid && !end_counter_rd_data) begin
107         miso <= tx_data[7-counter_rd_data];
108         counter_rd_data <= counter_rd_data+1;
109     end
110     else if (cs == IDLE) begin
111         end_counter_rd_data <= 0;
112     end
113 end
114 endmodule

```

- Testbench for the SPI slave

```

1 module SPI_slave_tb ();
2
3     reg mosi,ss_n,clk,rst_n,tx_valid;
4     reg[7:0] tx_data;
5     wire miso,rx_valid; // rx_valid show the counter ends
6     wire[9:0] rx_data;
7
8     SPI_slave dut0 (mosi,ss_n,clk,rst_n,tx_valid,tx_data,miso,rx_valid,rx_data);
9
10    initial begin
11        clk=0;
12        forever
13            #2 clk=~clk;
14    end
15
16    initial begin
17 //1
18        rst_n=0; mosi=$random; ss_n=1; tx_valid=1; tx_data=$random;
19        @(negedge clk);
20 //2
21        rst_n=1; mosi=$random; ss_n=1; tx_valid=1; tx_data=$random;
22        @(negedge clk);
23 //3
24        ss_n=0; tx_data=$random; tx_valid=1;
25        repeat(30) begin
26            mosi=$random; ss_n=0;
27            @(negedge clk);
28        end
29        ss_n=1;
30        @(negedge clk);
31
32 //4
33        ss_n=0; tx_data=$random; tx_valid=1;
34        repeat(30) begin
35            mosi=$random; ss_n=0;
36            @(negedge clk);
37        end
38        ss_n=1;
39        @(negedge clk);
40
41 //5
42        ss_n=0; tx_data=$random; tx_valid=1;
43        repeat(30) begin
44            mosi=$random; ss_n=0;
45            @(negedge clk);
46        end
47        ss_n=1;
48        @(negedge clk);
49        $stop;
50    end
51
52    initial begin
53        $monitor("rst_n=%b ,ss_n=%b ,mosi=%b ,rx_valid=%b ,rx_data=%b ,tx_valid=%b ,tx_data=%b ,miso=%b",rst_n,ss_n,mosi,rx_vali
54    end
55
56
57 endmodule

```

- RAM

```

9  input clk, rst_n, rx_valid;    //Control input signals
10
11  //Output ports
12  output reg [ADDR_SIZE - 1 : 0] dout; //8-bits Output data from the RAM
13  output reg tx_valid;           //Control output signal
14
15  reg [ADDR_SIZE - 1 : 0] mem [MEM_DEPTH - 1 : 0]; //Memory
16  reg [ADDR_SIZE - 1 : 0] w_addr, r_addr;         //Internal registers to store the read and write addresses
17
18  //RAM sequential logic
19  always @(posedge clk) begin
20      //Active low async reset
21      if(~rst_n) begin
22          dout <= 0;
23          tx_valid <= 0;
24          w_addr <= 0;
25          r_addr <= 0;
26      end
27      //rx_valid refers to that there is data on din ready to be read
28      else if (rx_valid) begin
29          //The MSB 2-bits are control signals
30          case (din[9:8])
31              2'b00: w_addr <= din[ADDR_SIZE-1 : 0]; //Store the Write address
32              2'b01: mem[w_addr] <= din[ADDR_SIZE-1 : 0]; //Write the data in the stored write address
33              2'b10: r_addr <= din[ADDR_SIZE-1 : 0]; //Store the Read address
34              2'b11: begin //Read the data stored in memory at read address
35                  dout <= mem[r_addr];
36                  tx_valid <= 1;
37              end
38          endcase
39      end
40  end
41 endmodule

```

Module RAM, Line 41, Column 10

- Testbench for the RAM part

```

1  module RAM_tb ();
2      reg [9:0] din;
3      reg clk, rst_n, rx_valid;
4      wire [7:0] dout;
5      wire tx_valid;
6      RAM dut (clk, rst_n, din, rx_valid, dout, tx_valid);
7      initial begin
8          clk=0;
9          forever begin
10             #5; clk=~clk;
11         end
12     end
13     initial begin
14         $readmemh("mem.dat", dut.mem);
15         rst_n=0; rx_valid=0; din=$random();
16         @(negedge clk);
17         rst_n=1; rx_valid=1;
18         @(negedge clk);
19         repeat(1000) begin
20             din=$random();
21             @(negedge clk);
22         end
23         $stop;
24     end
25 endmodule

```

- Top module

```

1  module SPI_top_module (mosi, ss_n, clk, rst_n, miso);
2
3      //Input ports
4      input clk, rst_n, ss_n; //Control signals
5      input mosi;             //Master_out_slave_in input
6
7      //Output ports
8      output miso;            //Master_in_slave_out output
9
10     //Internal signals
11     wire [9:0] rx_data;      //The parallel data sent to RAM
12     wire rx_valid, tx_valid; //Control signals for the read and write
13     wire [7:0] tx_data;      //The parallel data sent from the RAM to SPI
14
15     //SPI module
16     SPI_Slave dut0 (mosi, ss_n, clk, rst_n, tx_valid, tx_data, miso, rx_valid, rx_data);
17
18     //RAM module
19     RAM dut1 (.clk(clk), .rst_n(rst_n), .rx_valid(rx_valid), .tx_valid(tx_valid), .din(rx_data), .dout(tx_data));
20 endmodule

```


Testbench

```
1 module SPI_top_module_tb ();
2
3 //Ports
4 reg mosi, ss_n, clk, rst_n;
5 wire miso;
6
7 //The SPI module
8 SPI_top_module dut (mosi, ss_n, clk, rst_n, miso);
9
10 //Initiate the clock
11 initial begin
12     clk=0;
13     forever
14         #2 clk=~clk;
15 end
16
17 integer i;
18 initial begin
19
20     //Test reset & initiate signals
21     mosi = 0; ss_n = 1;
22     rst_n = 0;
23     @(negedge clk);
24     if (miso != 0) begin
25         $display("there was an error");
26         $stop;
27     end
28
29     rst_n = 1; //Release the reset button
30
31     //Test write & its address
32     repeat (1000) begin
33         ss_n = 0; //Release the ss_n to start communication
34         @(negedge clk);
35
36         //Sends the Write address
37         for (i = 0; i < 10; i = i + 1) begin
38             if (i < 2) begin
39                 mosi = 0; //first 2 bits are 00 to initiate write address
40             end
41             else
42                 mosi = $random; //sends 8 bits to be stored in the write address
43             @(negedge clk);
44         end
45
46         repeat(2) @(negedge clk); //Wait for the write address to read din in 2 clocks
47
48         ss_n = 1; //Set ss_n to stop the communication and start new one
49         @(negedge clk);
50
51         ss_n = 0; //Release the ss_n to start new task
52         @(negedge clk);
53
54         //Sends the data to be stored
55         for (i = 0; i < 10; i = i + 1) begin
56             if (i == 0) begin
57                 mosi = 0; //first 2 bits are 01 to initiate write data
58             end
59             else if (i == 1) begin
60                 mosi = 1;
61             end
62             else
63                 mosi = $random; //sends 8 bits to be stored in the memory
64             @(negedge clk);
65         end
66
67         repeat(2) @(negedge clk); //Wait for the RAM to store din in 2 clocks
68
69         ss_n = 1; //Set ss_n to stop the communication and start new one
70         @(negedge clk);
71     end
72     $stop; //Pause the sim after writing the memory
73
74 end
```

```

4 //test Read & its address
5 repeat (1000) begin
6     ss_n = 0; //Release the ss_n to start communication
7     @(negedge clk);
8
9     // sends the Read address
10    for (i = 0; i < 10; i = i + 1) begin
11        if (i == 0) begin
12            mosi = 1; //first 2 bits are 10 to initiate Read address
13        end
14        else if (i == 1) begin
15            mosi = 0;
16        end
17        else
18            mosi = $random; //sends 8 bits to be stored in the Read address
19        @(negedge clk);
20    end
21
22    repeat(2) @(negedge clk); //Wait for the read address to store din in 2 clocks
23
24    ss_n = 1; //Set ss_n to stop the communication and start new one
25    @(negedge clk);
26
27    ss_n = 0; //Release the ss_n to start a new task
28    @(negedge clk);
29
30
31 //Receives the read data
32 for (i = 0; i < 10; i = i + 1) begin
33     if (i < 2) begin
34         mosi = 1; //first 2 bits are 11 to initiate read data
35     end
36     else
37         mosi = $random; //the rest of the 8 bits are dummy data
38     @(negedge clk);
39 end
40
41 repeat(2) @(negedge clk); //Wait for the RAM to send the data on TX_data from mem read address stored
42
43 repeat(9) @(negedge clk); //Wait for the SPI slave to transfer the TX_data from parallel to series on the mis
44
45 ss_n = 1; //Set ss_n to stop the communication and start new one
46 @(negedge clk);
47 end
48 $stop; //End of simulation
49 end
50 endmodule

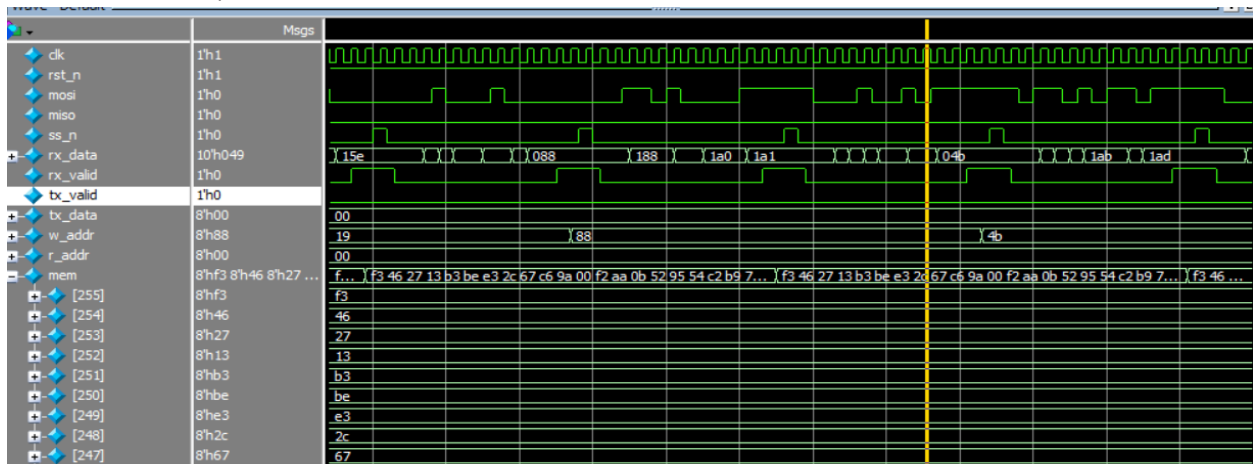
```

DO file.

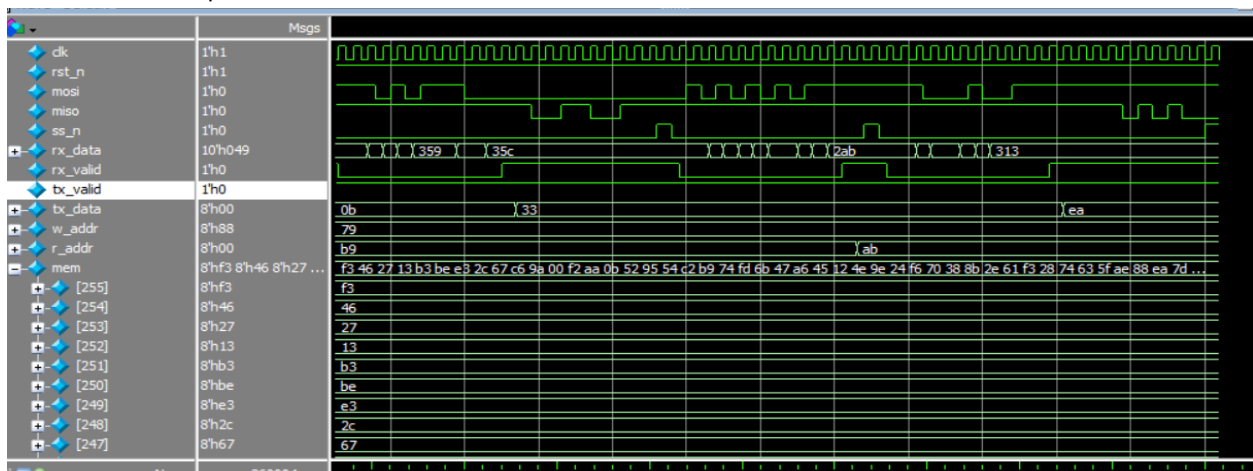
```
vlib work
vlog RAM.v SPI_Slave.v SPI_top_module.v SPI_tb.v
vsim -voptargs=+acc work.SPI_top_module_tb
add wave *
add wave -position insertpoint \
sim:/SPI_top_module_tb/dut/rx_data \
sim:/SPI_top_module_tb/dut/rx_valid \
sim:/SPI_top_module_tb/dut/tx_valid \
sim:/SPI_top_module_tb/dut/tx_data
add wave -position insertpoint \
sim:/SPI_top_module_tb/dut/dut1/mem \
sim:/SPI_top_module_tb/dut/dut1/w_addr \
sim:/SPI_top_module_tb/dut/dut1/r_addr
run -all
#quit -sim
```

Simulation

- Write operation.



- Read operation.



Constrain file.

```
## Clock signal
set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
```

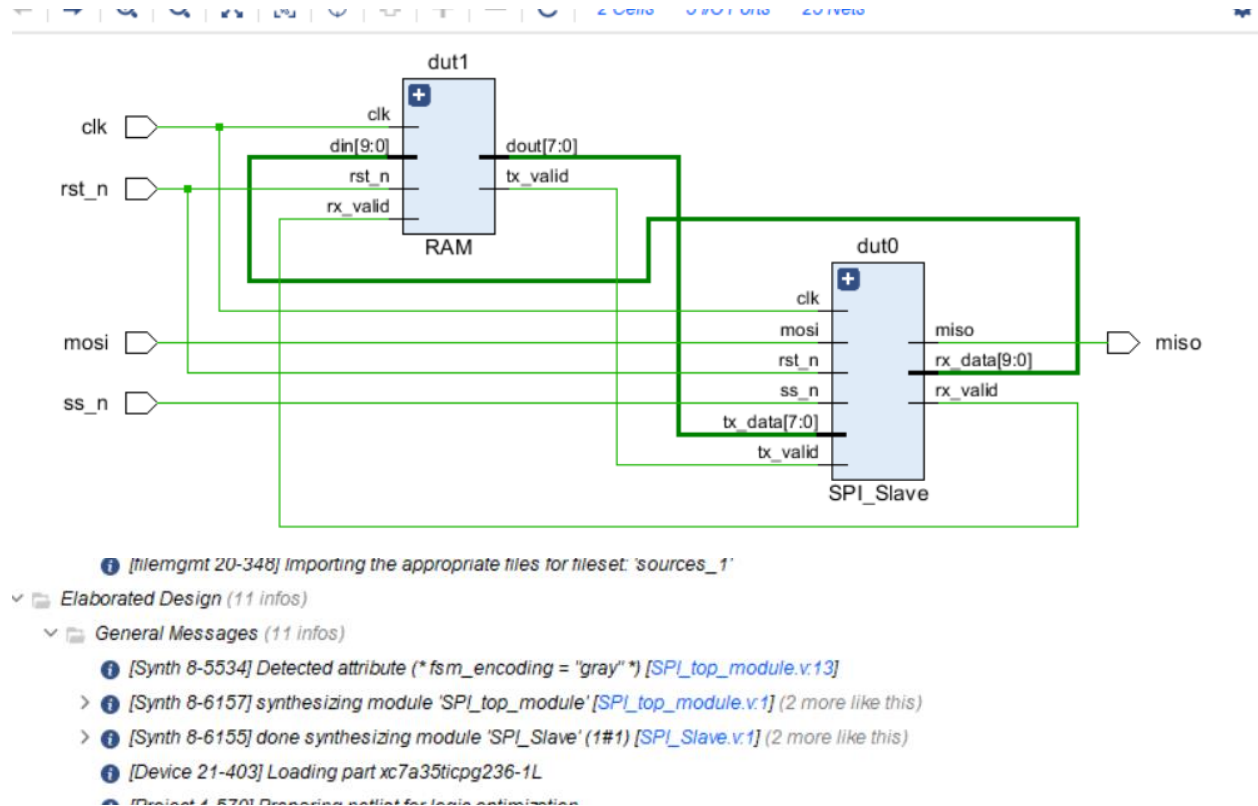
```
10
11 ## Switches
12 set_property -dict { PACKAGE_PIN V17  IOSTANDARD LVCMOS33 } [get_ports {rst_n}]
13 set_property -dict { PACKAGE_PIN V16  IOSTANDARD LVCMOS33 } [get_ports {ss_n}]
14 set_property -dict { PACKAGE_PIN W16  IOSTANDARD LVCMOS33 } [get_ports {mosi}]
15 #set_property -dict { PACKAGE_PIN W17  IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
16 #set_property -dict { PACKAGE_PIN W15  IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
17 #set_property -dict { PACKAGE_PIN V15  IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
18 #set_property -dict { PACKAGE_PIN W14  IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
```

```
9
0 ## LEDs
1 set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {miso}]
2 #set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {led[1]}]
```

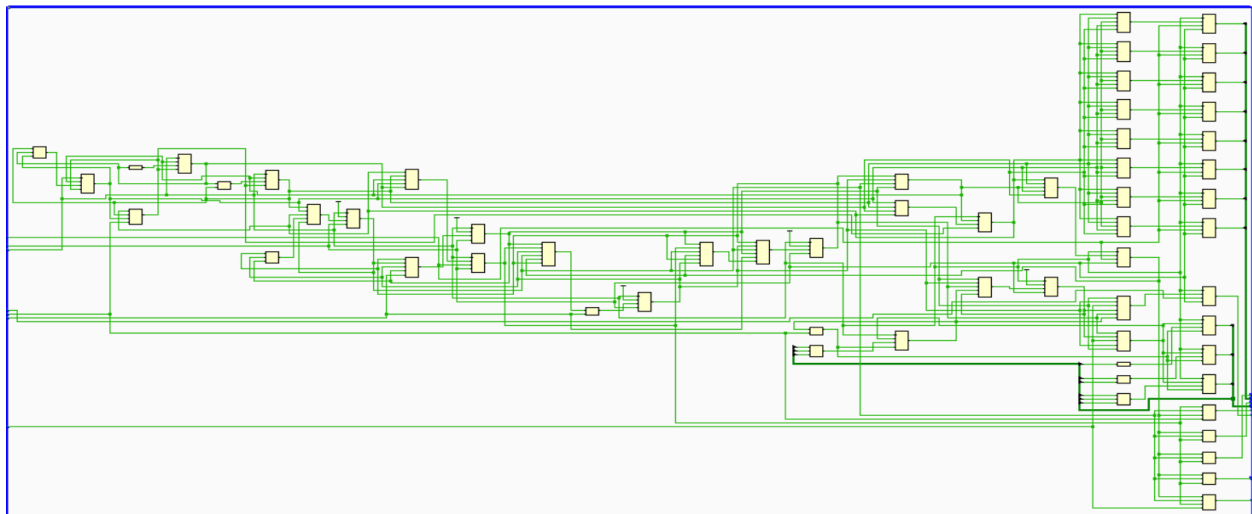
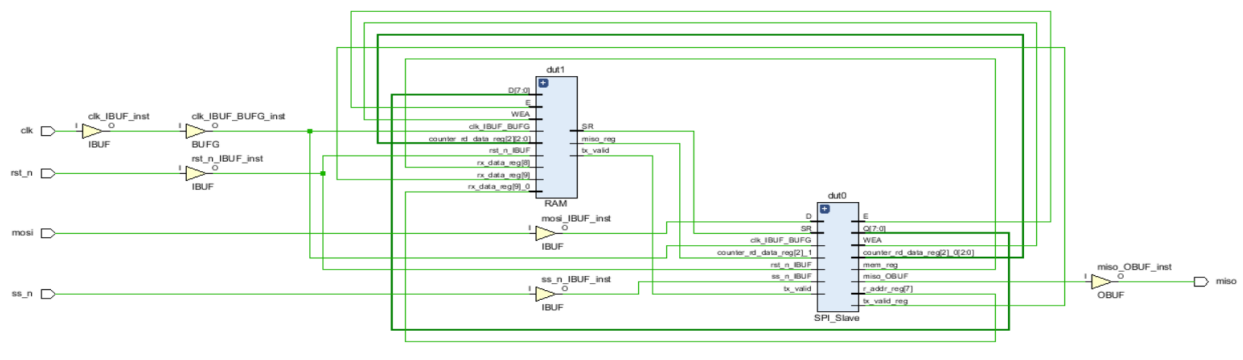
We will try Elaboration, Synthesis and Implementation using different encoding techniques.

Gray encoding: -

- Elaboration



- Synthesis
 - Schematic



- Messages

▼ **Synthesis** (30 infos)

- 1 [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
- > 1 [Synth 8-6157] synthesizing module 'SPL_top_module' [SPL_top_module.v:1] (2 more like this)
- 1 [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [SPL_Slave.v:23]
- > 1 [Synth 8-6155] done synthesizing module 'SPL_Slave' (1#1) [SPL_Slave.v:1] (2 more like this)
- 1 [Device 21-403] Loading part xc7a35ticipg236-1L
- 1 [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/elnor/Desktop/SPI/project_1/srcs/constrs_1/imports/SPI/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [X:/SPI_top_module_proprietary.xdc]
Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- 1 [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPL_Slave'
- > 1 [Synth 8-5544] ROM 'rx_valid' won't be mapped to Block RAM because address size (3) smaller than threshold (5) (3 more like this)
- 1 [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPL_Slave'

- Utilization

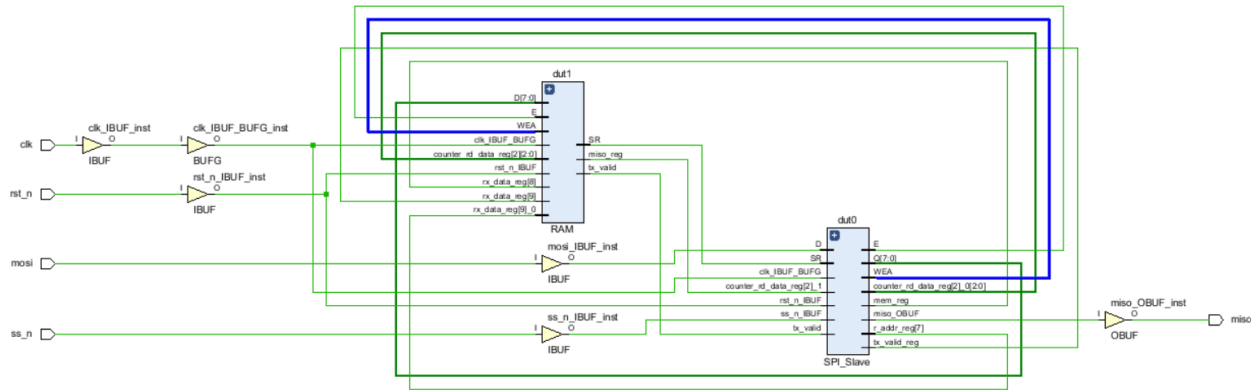
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_top_module	34	41	1	0.5	5	1
❏ dut0 (SPI_Slave)	31	24	0	0	0	0
❏ dut1 (RAM)	3	17	1	0.5	0	0

- Timing

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.261 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 101	Total Number of Endpoints: 101	Total Number of Endpoints: 44

All user specified timing constraints are met.

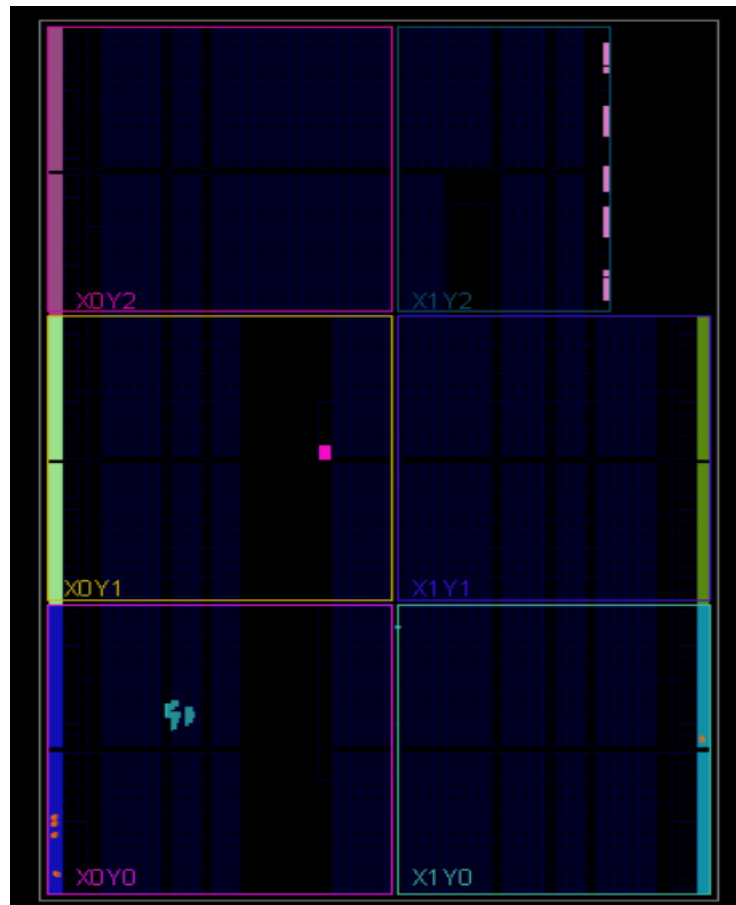
- Critical path



- Synthesis summary (encoding technique)

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

- Implementation
- Device



- Utilization

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPL_top_module	35	41	1	17	35	10	0.5	5	1
└ dut0 (SPL_Slave)	31	24	0	16	31	9	0	0	0
└ dut1 (RAM)	4	17	1	6	4	0	0.5	0	0

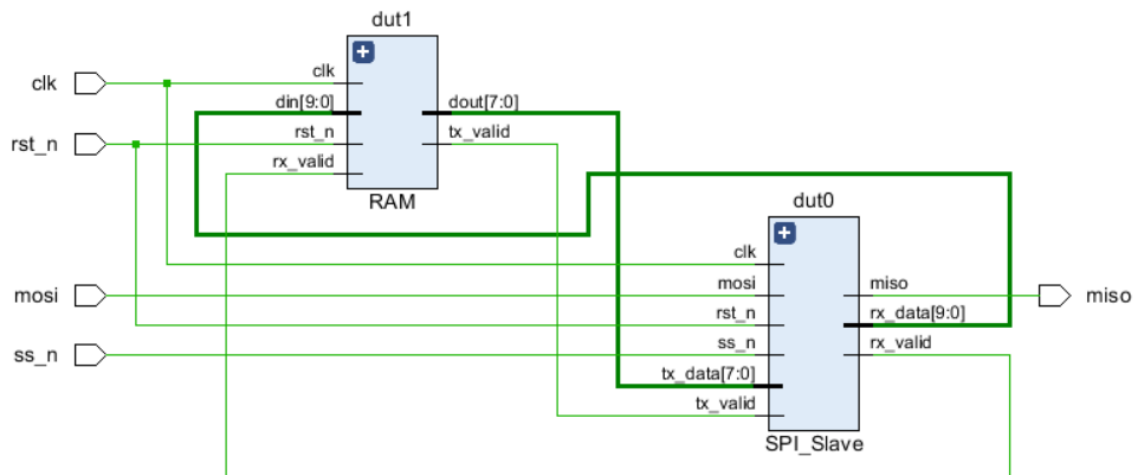
- Timing

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.049 ns	Worst Hold Slack (WHS): 0.110 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 102	Total Number of Endpoints: 102	Total Number of Endpoints: 44

All user specified timing constraints are met.

Seq encoding: -

- Elaboration

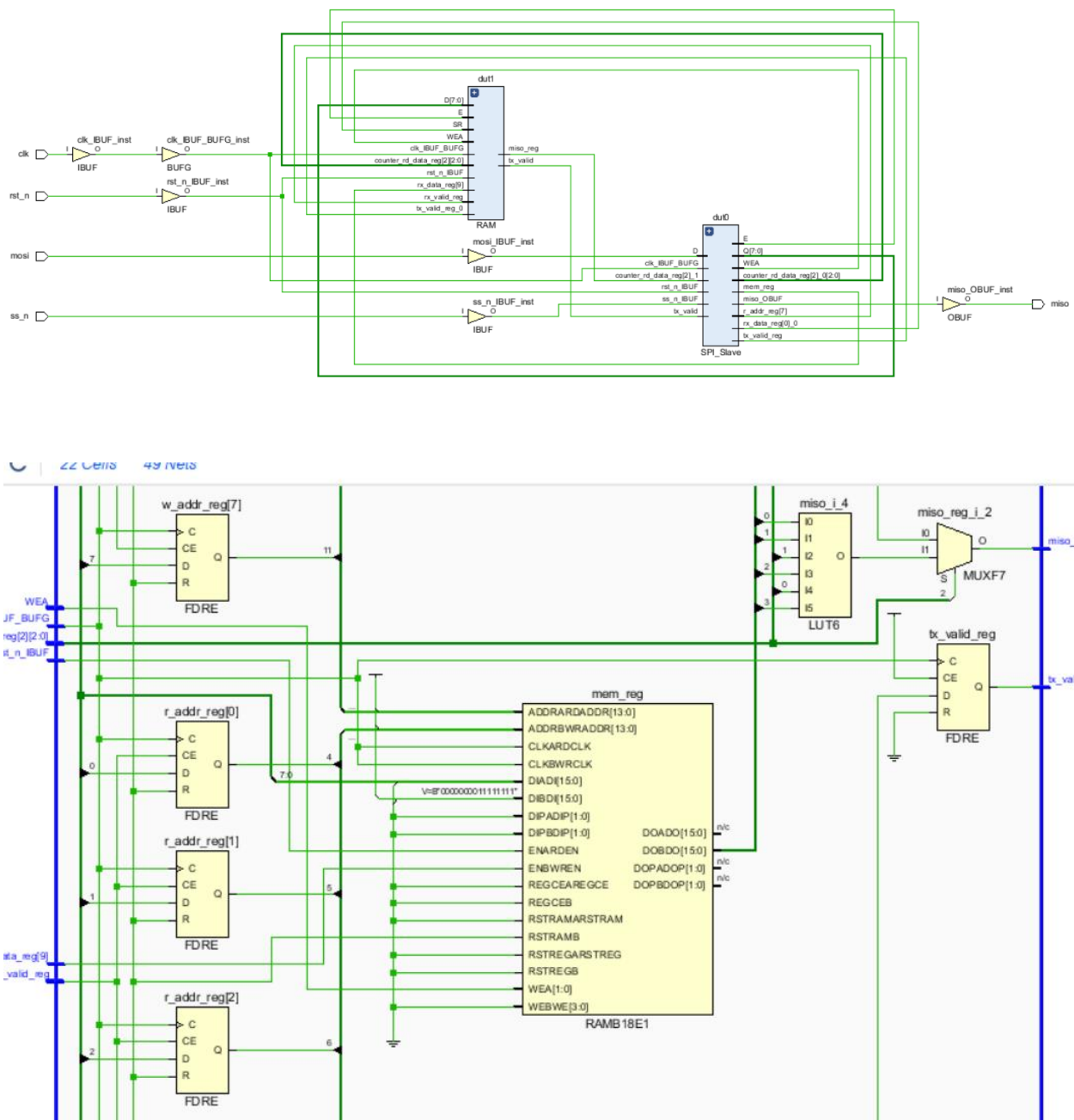


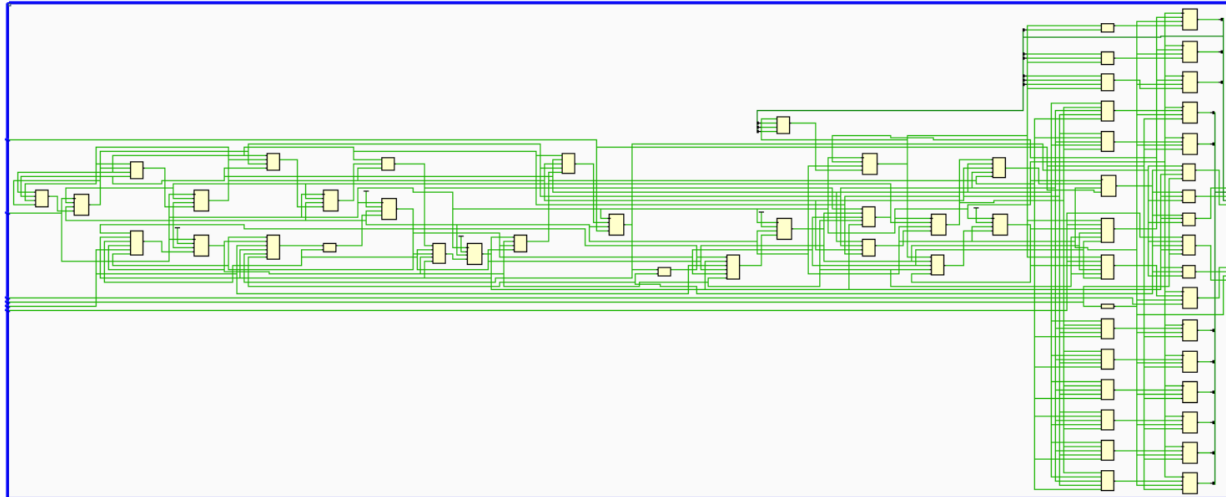
Elaborated Design (10 infos)

General Messages (10 infos)

- 1 [Synth 8-5534] Detected attribute (* fsm_encoding = "seq" *) [SPI_top_module.v:13]
- > 1 [Synth 8-6157] synthesizing module 'SPI_top_module' [SPI_top_module.v:1] (2 more like this)
- > 1 [Synth 8-6155] done synthesizing module 'SPI_Slave' (1#1) [SPI_Slave.v:1] (2 more like this)
- 1 [Project 1-570] Preparing netlist for logic optimization
- 1 [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- 1 [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

- Synthesis
- Schematic





- Messages

- ▼ Synthesized Design (6 infos)
 - ▼ General Messages (6 infos)
 - [Netlist 29-17] Analyzing 6 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

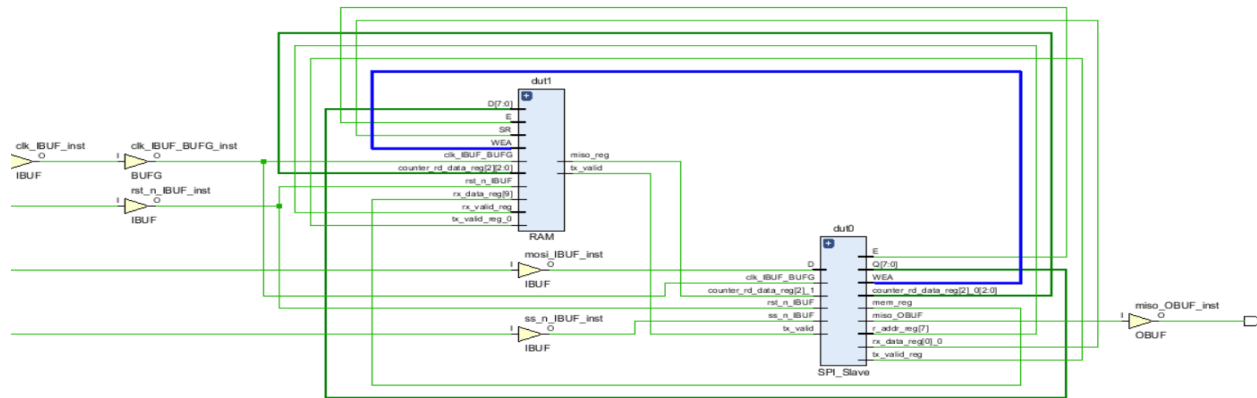
- Utilization

Hierarchy							
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFCTRL (32)	
▼ SPI_top_module	32	41	1	0.5	5	1	
▼ dbg_hub (dbg_hub_CV)	0	0	0	0	0	0	
▼ dut0 (SPI_Slave)	30	24	0	0	0	0	
▼ dut1 (RAM)	2	17	1	0.5	0	0	

- Timing

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.261 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 93	Total Number of Endpoints: 93	Total Number of Endpoints: 44
All user specified timing constraints are met		

- Critical path



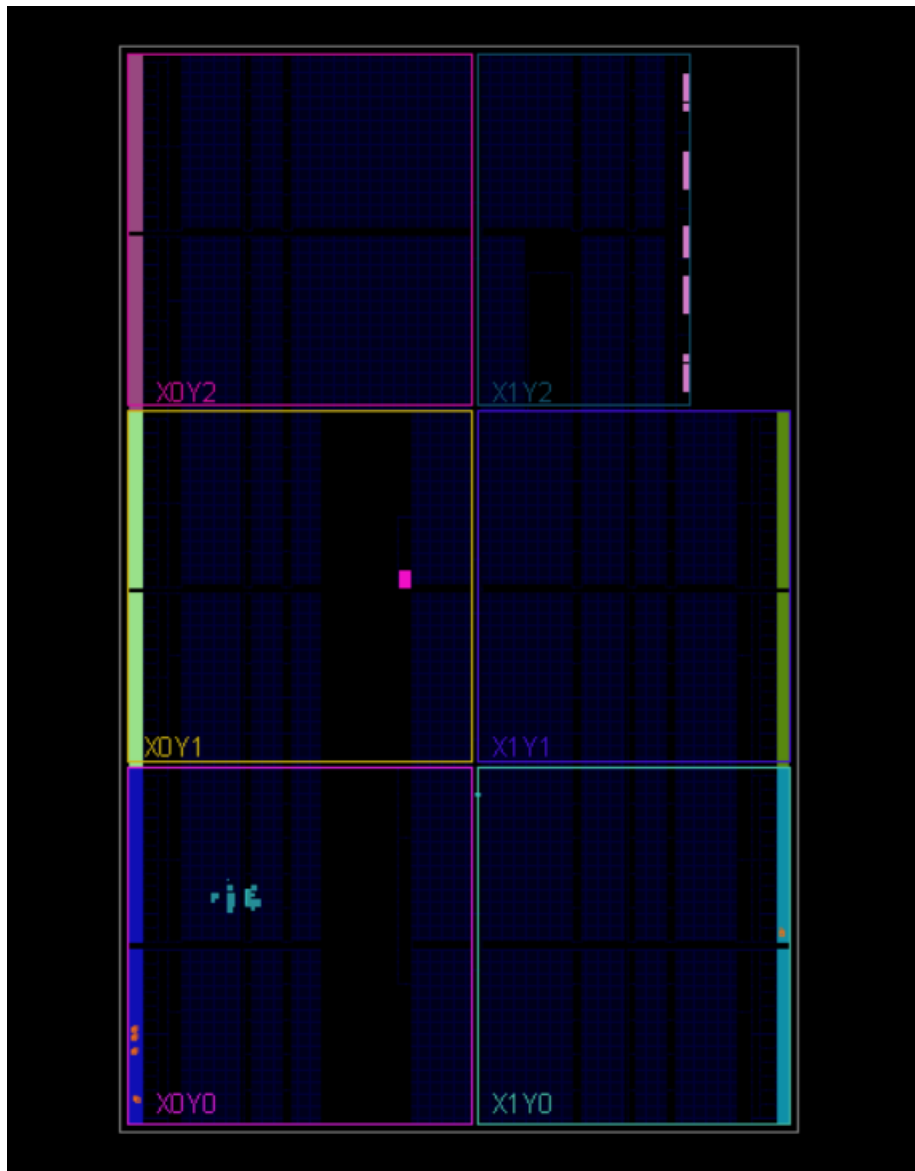
- Synthesis summary (encoding technique)

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI Slave'

- Implementation
- Device



▼ Implemented Design (9 infos)

▼ General Messages (9 infos)

- ① [Netlist 29-17] Analyzing 6 Unisim elements for replacement
- ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- ① [Project 1-479] Netlist was created with Vivado 2018.2
- ① [Project 1-570] Preparing netlist for logic optimization
- ① [Timing 38-478] Restoring timing data from binary archive.
- ① [Timing 38-479] Binary timing data restore complete.
- ① [Project 1-856] Restoring constraints from binary archive.

- Utilization

Q [] [] [] [] Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_top_module		32	41	1	0.5	5	1
dut0 (SPI_Slave)		30	24	0	0	0	0
dut1 (RAM)		2	17	1	0.5	0	0

- Timing

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Design Runs

Power

DRC

Methodology

Timing

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Design Timing Summary

Setup

Hold

Pulse Width

Worst Negative Slack (WNS): 6.052 ns

Worst Hold Slack (WHS): 0.102 ns

Worst Pulse Width Slack (WPWS): 4.500 ns

Total Negative Slack (TNS): 0.000 ns

Total Hold Slack (THS): 0.000 ns

Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Total Number of Endpoints: 94

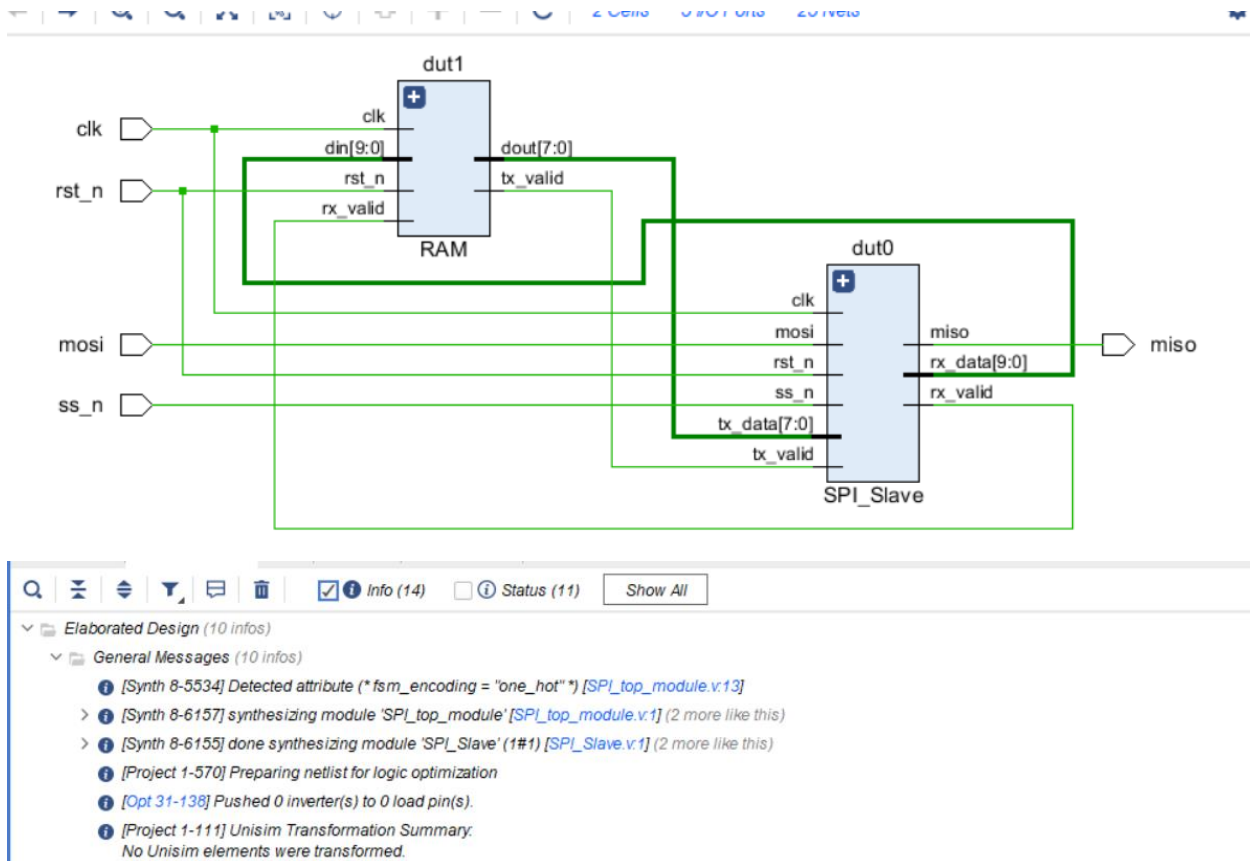
Total Number of Endpoints: 94

Total Number of Endpoints: 44

All user specified timing constraints are met.

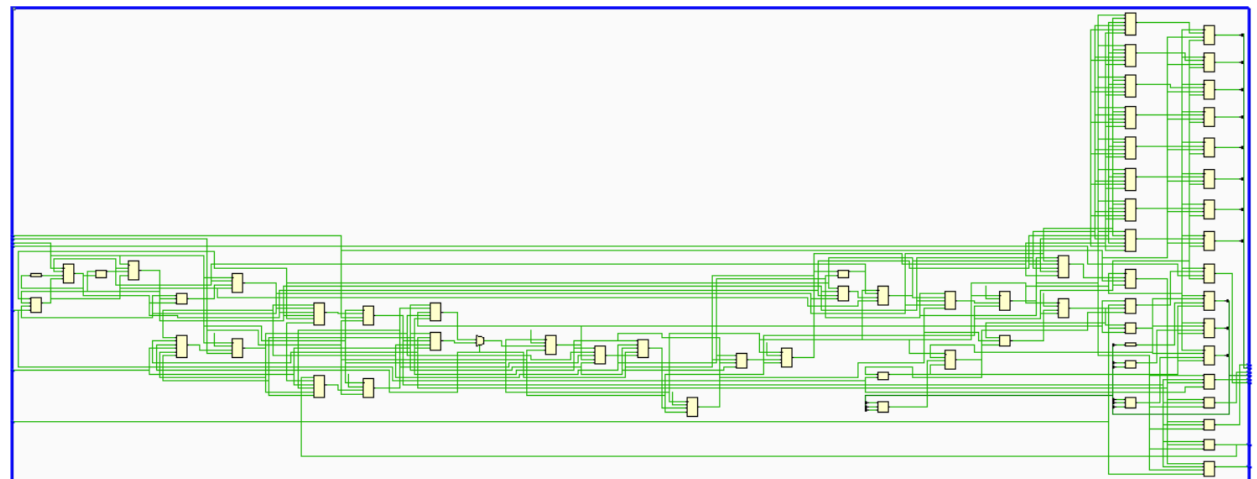
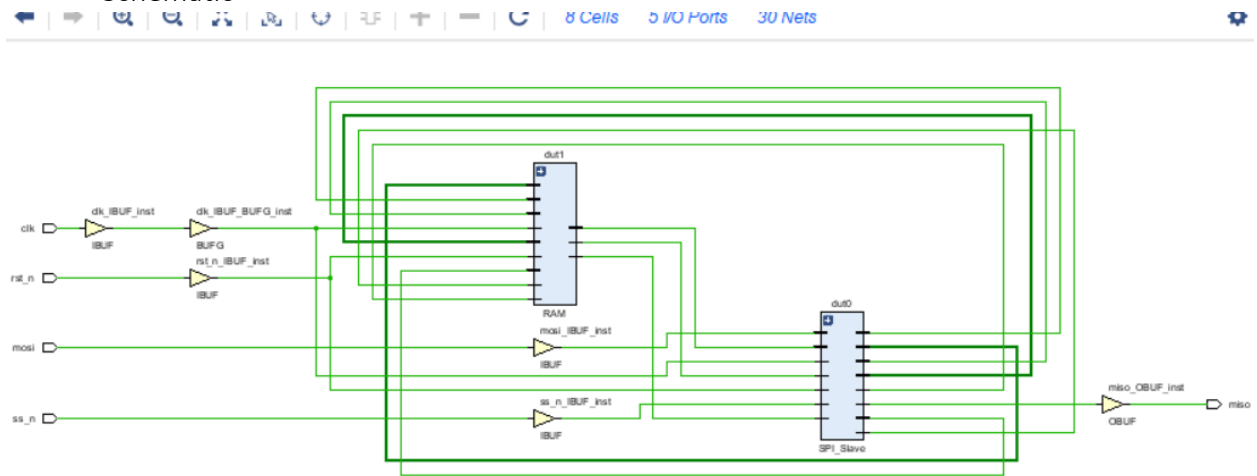
One_hot encoding: -

- Elaboration



- Synthesis

- Schematic



- Messages

[filemgmt 20-348] Importing the appropriate files for files: 'sources_1'

▼ Synthesis (1 warning, 31 infos)

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
- [Synth 8-6157] synthesizing module 'SPI_top_module' [SPI_top_module.v:1] (2 more like this)
- [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [SPI_top_module.v:13] (1 more like this)
- [Synth 8-6155] done synthesizing module 'SPI_Slave' (1#1) [SPI_Slave.v:1] (2 more like this)
- [Device 21-403] Loading part xc7a35ti:pg236-1L
- [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/elnor/Desktop/SPI/project_2/srcs/constrs_1/imports/SPI/Constraints_basys3.xdc]. 1 ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [V:/SPI_top_module_analysed.xdc]

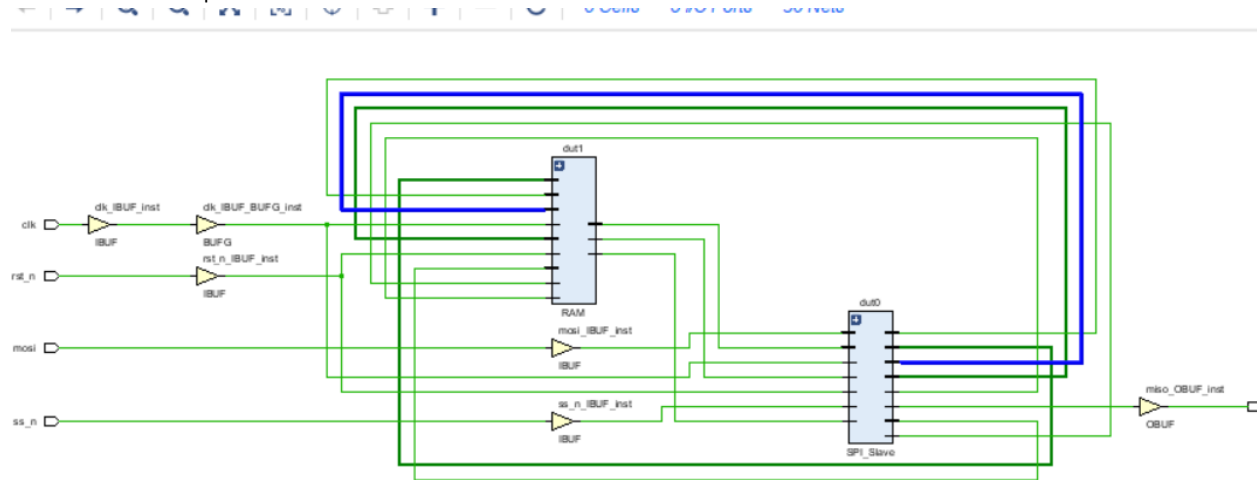
- Utilization

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ SPI_top_module	35	43	2	0.5	5	1
❏ dut0 (SPI_Slave)	32	26	1	0	0	0
❏ dut1 (RAM)	3	17	1	0.5	0	0

- Timing

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.261 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 103	Total Number of Endpoints: 103	Total Number of Endpoints: 46
All user specified timing constraints are met.		

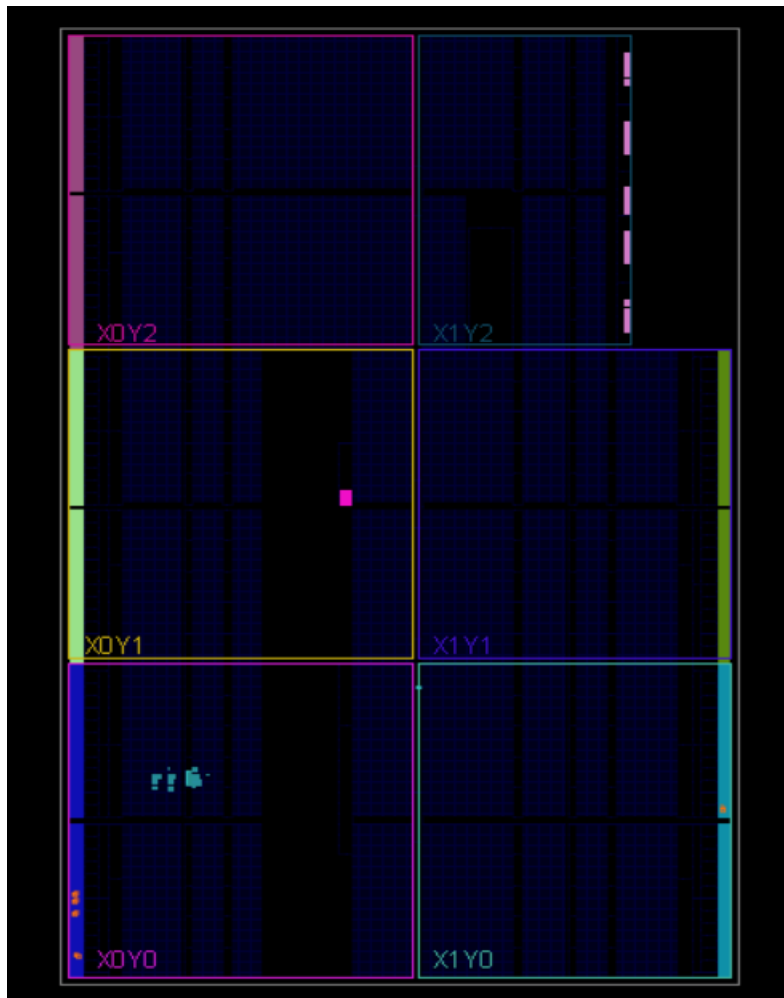
- Critical path



- Synthesis summary (encoding technique)

1 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
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- Implementation
- Device



▼ Implemented Design (10 infos)

▼ General Messages (10 infos)

- ❗ [Netlist 29-17] Analyzing 7 Unisim elements for replacement
- ❗ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- ❗ [Project 1-479] Netlist was created with Vivado 2018.2
- ❗ [Device 21-403] Loading part xc7a35ticpg236-1L
- ❗ [Project 1-570] Preparing netlist for logic optimization
- ❗ [Timing 38-478] Restoring timing data from binary archive.
- ❗ [Timing 38-479] Binary timing data restore complete.
- ❗ [Project 1-856] Restoring constraints from binary archive.
- ❗ [Project 1-853] Binary constraint restore complete.
- ❗ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

- Utilization

Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_top_module		36	43	2	19	36	12	0.5	5	1
dout0 (SPI_Slave)		32	26	1	16	32	11	0	0	0
dout1 (RAM)		4	17	1	6	4	0	0.5	0	0

- Timing

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.212 ns	Worst Hold Slack (WHS): 0.070 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 104	Total Number of Endpoints: 104	Total Number of Endpoints: 46

All user specified timing constraints are met.

Comparison between techniques

Technique	Setup slack	Hold slack
Gray	6.049 ns	0.110 ns
Seq	6.052 ns	0.102 ns
One_hot	6.212 ns	0.070 ns

So as we considered gray encoding gives the best in the worst hold slack and one_hot encoding gives the best in the worst setup slack.