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Computer Organization and Architecture Sheet

Part 1: Answer the following questions

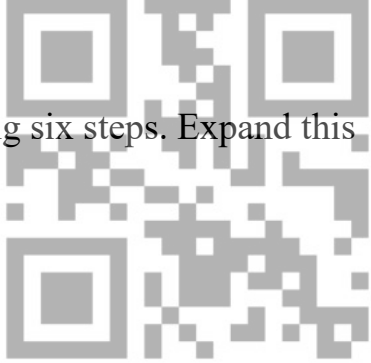
1. Given a hypothetical machine that has five memory and I/O instructions:

   0001 = Load AC from memory
   0010 = Store AC to memory
   0011 = Load AC from I/O
   0111 = Store AC to I/O
   0101 = Add to AC from memory

   In these cases, the 12-bit address identifies a particular I/O device. Show the content of IR for the following:

   1. Load AC from I/O device 5.
   2. Add contents of memory location 940.
   3. Store AC to I/O device 6.

2. The program execution of Figure 3-5 is described in the text using six steps. Expand this description to show the use of the MAR and MBR.



3. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.
   a. What is the maximum directly addressable memory capacity (in bytes)?
   b. Discuss the impact on the system speed if the microprocessor bus has
      i. a 32-bit local address bus and a 16-bit local data bus, or
      ii. a 16-bit local address bus and a 16-bit local data bus.
   c. How many bits are needed for the program counter (PC) and the instruction register (32)?

4. Consider a hypothetical microprocessor generating a 16-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus.
    a. What is the maximum memory address space that the processor can access directly if it is connected to a “16-bit memory”?
    b. What is the maximum memory address space that the processor can access directly if it is connected to an “8-bit memory”?
    c. What architectural features will allow this microprocessor to access a separate “I/O space”?
    d. If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support? How many 16-bit I/O ports? Explain.

5. Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor?

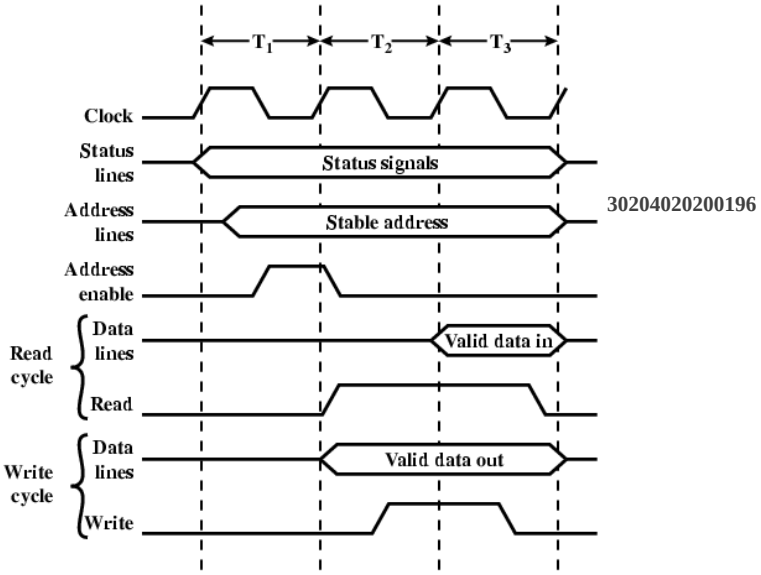
6. Consider a computer system that contains an I/O module controlling a simple keyboard/printer teletype. The following registers are contained in the processor and connected directly to the system bus:
    - INPR: Input Register, 8 bits
    - OUTR: Output Register, 8 bits
    - FGI: Input Flag, 1 bit
    - FGO: Output Flag, 1 bit
    - IEN: Interrupt Enable, 1 bit

Keystroke input from the teletype and printer output to the teletype are controlled by the I/O module. The teletype is able to encode an alphanumeric symbol to an 8-bit word and decode an 8-bit word into an alphanumeric symbol.

a. Describe how the processor, using the first four registers listed in this problem, can achieve I/O with the teletype.
b. Describe how the function can be performed more efficiently by also employing IEN.

7. Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.
    a. Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?
    b. Repeat assuming that half of the operands and instructions are one byte long.

8. A microprocessor has a memory write timing as shown in the following Figure. Its manufacturer specifies that the width of the Write signal can be determined by $T - 50$, where T is the clock period in ns.
    a. What width should we expect for the Write signal if bus clocking rate is 5 MHz?
    b. The data sheet for the microprocessor specifies that the data remain valid for 20 ns after the falling edge of the Write signal. What is the total duration of valid data presentation to memory?



9. A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (three cycles), add 1 to operand (three cycles), and store operand (three cycles).
    a. By what amount (in percent) will the duration of the instruction increase if we have to insert two bus wait states in each memory read and memory write operation?
    b. Repeat assuming that the increment operation takes 13 cycles instead of 3 cycles.

10. The Intel 8088 microprocessor has a read bus timing similar to that of the previous Figure but requires four processor clock cycles. The valid data is on the bus for an amount of time that extends into the fourth processor clock cycle. Assume a processor clock rate of 8-MHz.
    a. What is the maximum data transfer rate?
    b. Repeat but assume the need to insert one wait state per byte transferred.

11. The Intel 8086 is a 16-bit processor similar in many ways to the 8-bit 8088. The 8086 uses a 16-bit bus that can transfer 2 bytes at a time, provided that the lower-order byte has an even address. However, the 8086 allows both even- and odd-aligned word operands. If an odd-aligned word is referenced, two memory cycles, each consisting of four bus cycles, are required to transfer the word. Consider an instruction on the 8086 that involves two 16-bit operands. How long does it take to fetch the operands? Give the range of possible answers. Assume a clocking rate of 4 MHz and no wait states.

12. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

13. Represent the following decimal numbers in both binary sign/magnitude and twos complement using 16 bits:
    a. $+512$
    b. -29

14. Represent the following twos complement values in decimal:

a. 1101011

b. 0101101

Another representation of binary integers that is sometimes encountered is ones complement. Positive integers are represented in the same way as sign magnitude. A negative integer is represented by taking the Boolean complement of each bit of the corresponding positive number.

a. Provide a definition of ones complement numbers using a weighted sum of bits, similar to Equations (4.1) and (4.2).

b. What is the range of numbers that can be represented in ones complement?

c. Define an algorithm for performing addition in ones complement arithmetic.

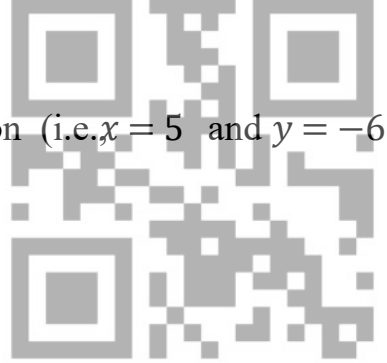
16. In Section 4.3, the twos complement operation is defined as follows. To find the twos complement of X, take the Boolean complement of each bit of X, and then add 1. Show that the following is an equivalent definition. For an n-bit integer X, the twos complement of X is formed by treating X as an unsigned integer and calculating $(2_n - X)$.

17. The r's complement of an n-digit number N in base r is defined as $r^n - N$ for $N \neq 0$ and 0 for $N = 0$. Find the tens complement of the decimal number 13250.

18. Assume numbers are represented in 8-bit twos complement representation. Show the calculation of the following:
    a. $6 + 13$
    b. $-6 + 13$
    c. $6 - 13$
    d. $-6 - 13$

19. Find the following differences using twos complement arithmetic:
    a. $111000 - 110011$
    b. $11001100 - 101110$
    c. $111100001111 - 110011110011$

20. Given $x = 0101$ and $y = 1010$ in twos complement notation (i.e. $x = 5$ and $y = -6$), compute the product $p = x \times y$ with Booth's algorithm.



Use the Booth algorithm to multiply 23 (multiplicand) by 29 (multiplier), where each number is represented using 6 bits.

22. Divide -145 by 13 in binary twos complement notation, using 12-bit words. Use the algorithm described in Section 4.3.

23. Assume that the exponent e is constrained to lie in the range $0 \leq e \leq X$ with a bias of q, that the base is b, and that the significand is p digits in length.
    a. What are the largest and smallest positive values that can be written?
    What are the largest and smallest positive values that can be written as normalized floating-point numbers?

24. Express the following numbers in IEEE 32-bit floating-point format:
    a. -5
    b. -6
    c. -1.5
    d. 384
    e. 1/16
    f. -1/32

25. The following numbers use the IEEE 32-bit floating-point format. What is the equivalent decimal value?
    a. 1 10000011 11000000000000000000000
    b. 0 01111110 10100000000000000000000
    c. 0 10000000 00000000000000000000000

26. Show how the following floating-point additions are performed (where significands are truncated to 4 decimal digits). Show the results in normalized form.
    a. $5.566 \times 10^2 + 7.777 \times 10^2$
    b. $3.344 \times 10^1 + 8.877 \times 10^{-2}$

27. Show how the following floating-point subtractions are performed (where significands are truncated to 4 decimal digits). Show the results in normalized form.
    a. $7.744 \times 10^{-3} - 6.666 \times 10^{-3}$
    b. $8.844 \times 10^{-3} - 2.233 \times 10^{-1}$

28. Show how the following floating-point calculations are performed (where significands are truncated to 4 decimal digits). Show the results in normalized form
    a. $(2.255 \times 10^{1}) \times (1.234 \times 10^{0})$
    b. $(8.833 \times 10^{2}) \div (5.555 \times 10^{4})$

29. Show in hex notation:
    a. a. The packed decimal format for 23
    b. b. The ASCII characters 23

30. For each of the following packed decimal numbers, show the decimal value:
    a. 0111 0011 0000 1001
    b. 0101 1000 0010
    c. 0100 1010 0110

31. A given microprocessor has words of 1 byte. What is the smallest and largest integer that can be represented in the following representations:
    a. Unsigned
    b. Sign-magnitude
    c. Ones complement
    d. Twos complement
    e. Unsigned packed decimal
    f. Signed packed decimal

32. Compare zero-, one-, two-, and three-address machines by writing programs to compute

$$X = (A + B \times C)/(D - E \times F)$$

for each of the four machines. The instructions available for use are as follows:

0 Address	1 Address	2 Address	3 Address
PUSH M	LOAD M	MOVE (X ← Y)	MOVE (X ← Y)
POP M	STORE M	ADD (X ← X + Y)	ADD (X ← Y + Z)
ADD	ADD M	SUB (X ← X − Y)	SUB (X ← Y − Z)
SUB	SUB M	MUL (X ← X × Y)	MUL (X ← Y × Z)
MUL	MUL M	DIV (X ← X/Y)	DIV (X ← Y/Z)
DIV	DIV M		

33. Given the following memory values and a one-address machine with an accumulator, what values do the following instructions load into the accumulator?
    - Word 20 contains 40.
    - Word 30 contains 50.
    - Word 40 contains 60.
    - Word 50 contains 70.

a) LOAD IMMEDIATE 20
b) LOAD DIRECT 20
c) LOAD INDIRECT 20
d) LOAD IMMEDIATE 30
e) LOAD DIRECT 30
f) LOAD INDIRECT 30

34. Let the address stored in the program counter be designated by the symbol X1. The instruction stored in X1 has an address part (operand reference) X2. The operand needed to execute the instruction is stored in the memory word with address X3. An index register contains the value X4. What is the relationship between these various quantities if the addressing mode of the instruction is (a) direct; (b) indirect; (c) PC relative; (d) indexed?

35. An address field in an instruction contains decimal value 14. Where is the corresponding operand located for
    a) immediate addressing?
    b) direct addressing?
    c) indirect addressing?
    d) register addressing?
    e) register indirect addressing?

36. Consider a 16-bit processor in which the following appears in main memory, starting at location 200:

200	Load to AC	Mode
201	500	
202	Next instruction	

The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R1, which has a value of 400. There is also a base register that contains the value 100. The value of 500 in location 201 may be part of the address calculation. Assume that location 399 contains the value 999, location 400 contains the value 1000, and so on. Determine the effective address and the operand to be loaded for the following address modes:

a) Direct
b) Immediate
c) Indirect
d) Register
e) Register Indirect

Part 2: Select the correct answer

1. Which of the following isn't an example of architectural attributes?
   a. instruction set
   b. control signal
   c. I/O mechanisms
   d. Techniques for addressing memory
2. The function called …….. means that computer can store data, even if the computer is processing data on the fly.
   a. Data processing
   b. Data storage
   c. Data movement
   d. control
3. ……. are used to provide storage internal to the CPU.
   a. Memory
   b. ALU
   c. Registers
   d. None of the above

Each location in memory contains a binary number that can be interpreted as ……..

   a. an instruction
   b. data
   c. either an instruction or data
   d. None of the above

5. Given a memory organized as 16-bit words with 4 bits for the opcode and 12-bit for address. How many different opcodes?
   a. 8
   b. 16
   c. 2048
   d. 4096

6. ……. contains the data to be written into memory or receives the data read from memory.
   a. MAR
   b. MBR
   c. IR
   d. P
7. Which of the following is an input to CPU module?
   a. Read/Write signals
   b. Interrupt signals
   c. Address
   d. None of the above
8. Which of the following is an output of memory module?
   a. Read/Write signals
   b. Interrupt signals
   c. Address
   d. None of the above

9. In …… bus, there are separate data and address lines in addition to control lines.
   a. Dedicated
   b. Multiplexed
   c. Indexed
   d. None of the above
10. What is the clock cycle of 32-bit microprocessor with 8-MHz input clock?
   a. 150 ns
   b. 125 ns
   c. 100 ns
   d. 75 ns

11. In …….. arbitration, only a single hardware device controlling bus access.
    a. Distributed
    b. Centralized
    c. Cached
    d. None of the above
12. Which of the following is a binary representation of decimal number -15 using sign magnitude?
    a. 10001111
    b. 11111111
    c. 11110000
    d. None of the above
13. Which of the following is a binary representation of decimal number -1 using two's complement?
    a. 10000001
    b. 11111111
    c. 00000001
    d. None of the above
14. Given a binary number 11111000 represented using two's complement. What is the corresponding decimal value?
    a. -7
    b. -248
    c. -8
    d. None of the above
15. Given a dividend= 10010011 and divisor=1011. What is the value of remainder?
    a. 100
    b. 110
    c. 101
    d. None of the above
16. What is the result of normalizing 111.110×2^2?
    a. 0.11111×2^3
    b. 1.11110×2^4
    c. 1.1111×2^3
    d. None of the above
17. To represent -0.75 using 32-IEEE floating point format, the biased exponent equals ……..
    a. 00000000000000000000000
    b. 00000000000000000000001
    c. 10000000000000000000000
    d. None of the above
18. To represent -0.75 using 32-IEEE floating point format, the fraction equals …….
    a. 01111111
    b. 10111111
    c. 11111111
    d. None of the above
19. To represent $X = A - B$ using three address instructions, it requires …….
    a. One instruction
    b. Two instruction
    c. Three instruction
    d. None of the above
20. To represent $A - B$ using one address instructions, it requires …….
    a. One instruction
    b. Two instruction
    c. Three instruction
    d. None of the above
21. What is the represent of representing 320 using packed decimal?
    a. 001100100000
    b. 0000001100100000

c. 00110010
d. None of the above

22. Each character in ASCII is represented by a unique ……. Pattern.
    a. 4-bit
    b. 7-bit
    c. 8-bit
    d. 16-bit

23. The data transfer instruction must specify …….
    a. length of data
    b. mode of addressing
    c. source and destination operands
    d. All the above

24. What is the result of logical right shift by 3-bits for 11110001?
    a. 11111110
    b. 00011110
    c. 00111110
    d. None of the above

25. What is the result of arithmetic right shift by 3-bits for 11110001?
    a. 11111110
    b. 00011110
    c. 00111110
    d. None of the above

26. What is the result of left rotate by 3-bits for 11110001?
    a. 11000111
    b. 11100011
    c. 00111110
    d. None of the above

27. In addressing modes notation, the symbol ……. means the content of memory location or register.
    a. A
    b. R
    c. EA
    d. (X)

28. The immediate addressing mode requires …… memory references to fetch data.
    a. no
    b. one
    c. two
    d. three

29. The relative addressing mode is called ……. relative addressing.
    a. AC
    b. PC
    c. IR
    d. MAR

30. The instruction length is affected by …….
    a. memory size
    b. bus structure
    c. processor speed
    d. All the above