```
time_End needs to be the largest number in cirInputs
while(time_End != clock_Sim)
{

//access the first element of cirInput and it's time is the time of the first input
//check the usedGates vector to see if it contains that input
// If an element of usedgates contains input, apply the expression (function) and store it in the
(cirinputs)
        //Wait until all gates are tested then run functions
        //You will add this new input with the current time + propagation delay
        //Update time_End with the last value of cirInputs if it is larger than the current value
//loop
//Know that the final output is the last value in cirInputs


}

write_To_sim
{
//Traverse cirInputs and write to file

}
```