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Project Report
Dr. Mohamed Shaalan
Digital Alarm Clock
Members:

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Abstract:

During the course, we got introduced to the FPGA and learned its applications, such as counters, clocks and others. However, adding an alarm with a buzzer into the clock system and an adjustment option for the clock helped us develop a more advanced system that is close to clock systems we use in our daily life in our mobile phones. In order to build this system, we used the Vivado integrated design environment utilizing its built in features, including a framework for

testing and verifying designs in addition to FPGA implementation. Throughout this report, we delve deep into the development process from system design to hardware selection and software implementation, we highlight the challenges we encountered during the process and how we find solutions to them. The system was comprehensively tested, and the results demonstrated a successful implementation, providing a robust basis for future improvements.

Project Objective:

The aim of the project is to create a digital alarm clock. There are two modes of operation, the clock/alarm mode and the adjust mode. During the clock operation, when the current time matches current alarm time, LD0 blinks, and hitting any button stops the blinking. Based on pressing buttons the user can adjust time hour, time minute, alarm hour, and alarm minute. Also, different buttons increment and decrement the selected values.

Tools and technologies used:

Logism was used to model the circuit. Visio was used to model the FSM, ASM, control unit(CU) and Datapath(DP). Verilog was used for implementation and for writing onto the FPGA.

System design:

In clock mode:

6 counters that count when in clock mode
When adjusting the clock in adjust mode we load them
In adjust mode:
4 counters that are used for loading and not counting
6 states
We count using behavioral design
We use a lot of control signals
7Seg Bcd

There are 6 states: clock, alarm, adjust 0, adjust 1, adjust 2, adjust 3. The clock mode consists of 6 counters that count when in clock mode. This consists of 2 modulo 10 counters and 2 modulo 6 counters. When adjusting the clock in adjust mode we load values into the counter. In adjust mode, 4 counters are used for loading and not for counting. Using behavioral design, we implement if conditions

Validation Activities:

Constraint Files:

In order to properly test Verilog code, we opted to use constraint files and test on the FPGA. This was used for each and every part of all the module files.

- LED FOR DEBUGGING:
  We used LED states to know which state we are in. For example, to make sure we are in clock mode, we made all the LEDS as 1s, and a change in the LEDs implied a transitioning of states, To add, we used LEDs to know whether or not we are i alarm mode where if the set alarm time was equal to current time, a LED state was used to blink. This was done as a preliminary step before connecting a buzzer.
- 7 SEGMENT FOR DEBUGGING:

The 7 segment was used to display the clock. It was also utilized for the purpose of displaying the adjust modes where they either increment or decrement

- Push button test module created on its own for testing:

We created a module to test the push buttons where we ensured that they worked correctly.

Logisim Evolution:

We constructed the datapath and the control unit of the system using the ASM. In order to validate their effectiveness and accuracy, we decided to simulate them using Logisim. Therefore, after each one of us constructed their parts in the datapath and control unit, we merged them and tested their outputs. This helped us confirm that our datapath and control unit were a solid foundation which we could use to implement the program.

Contributions:

FSM: All

ASM:
Ahmed AbdelKader: Clock and Alarm States
Ahmed Abdeen: The Adjust_0 and Adjust_1 states
Tony Gerges: The Adjust_2 and Adjust_3 states

Control unit:
Ahmed AbdelKader: Clock and Alarm control unit states circuit
Ahmed Abdeen: The Adjust_0 and Adjust_1 states control unit circuit
Tony Gerges**:** The Adjust_2 and Adjust_3 states control unit circuit

Challenges faced:

Incrementing/decrementing the clock time:
During the system design process, we represented the increment and decrement feature in the ASM as increasing the register storing the clock time by one rather than using the up/down input of the counters. In order to stick to our ASM design, we chose to load the counters of the clock with the incremented/decremented value from the clock register and we added logic that accounted for all the cases in the incrementing/decrementing process, such as when reaching 59 minutes, incrementing will return the clock to zero.

Coordinating our work during the design process:
As mentioned above we used visio to design the control unit ,datapath, ASM and the FSM. First we constructed an FSM together on Zoom and then the ASM using visio. After that we used the ASM to construct the datapath and control unit. Each one of us took two states to construct their respective circuits using logisim and then we merged our work using visio. To implement the system using Vivado, we would meet in the lab to work on the implementation and testing together.

References:

https://github.com/Ahmed-Fawzy14/Project-2-Digital-Alarm-Clock.git

Appendices: