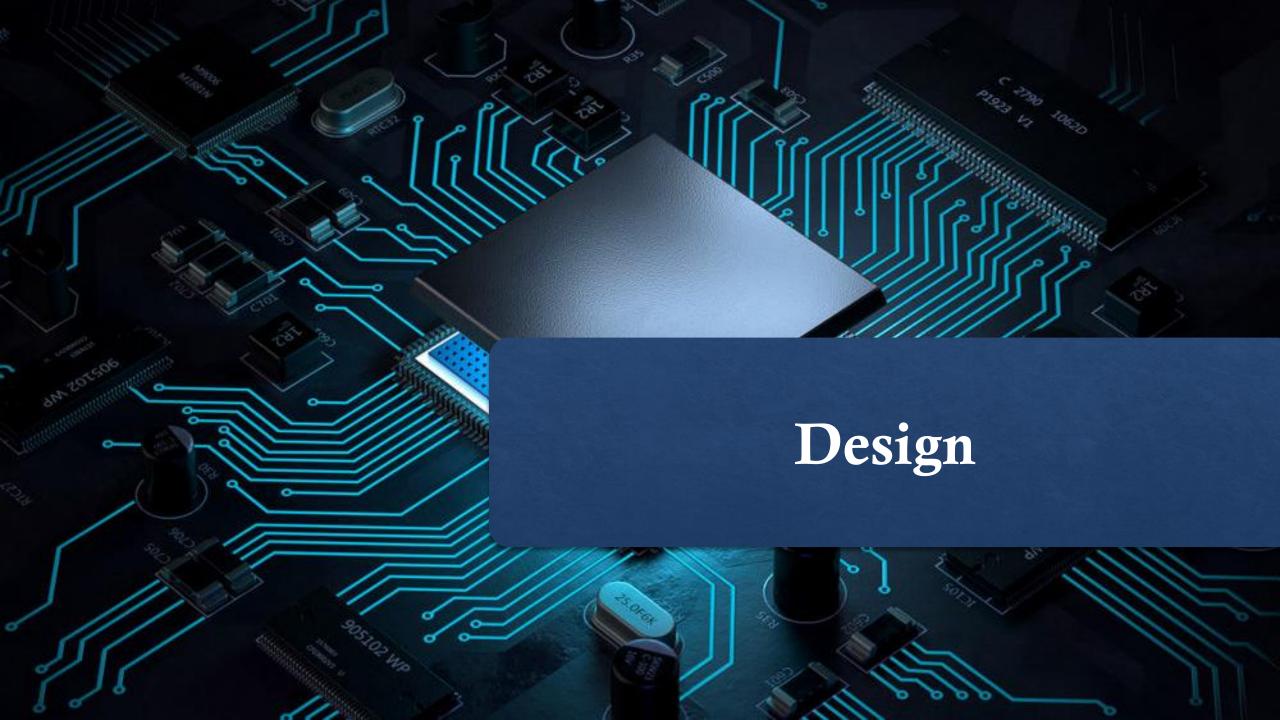
بسم الله الرحمن الرحيم

# Logic Design Project

**Eng \ Ahmed Hamed Mohamed** 

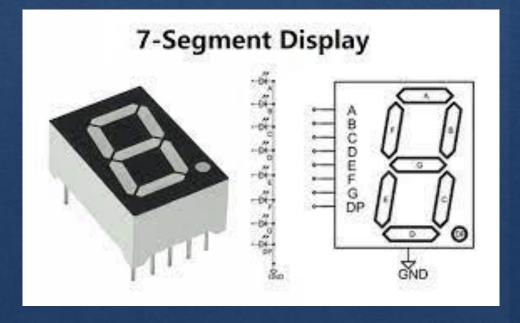


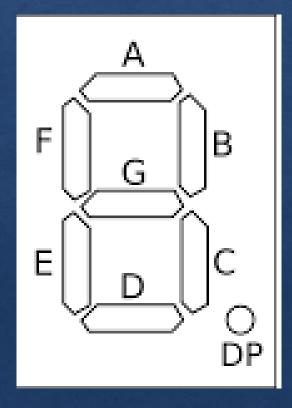
#### Logic Design Project\_Design

In this project you are required to design and implement a digital system that controls three sevensegment displays to show the acronyms ASU, FOE, CSE, and FUN. This system will switch between these displays sequentially with a one second interval between them

- 00: ASU
- 01: FOE
- 10: CSE
- 11: FUN



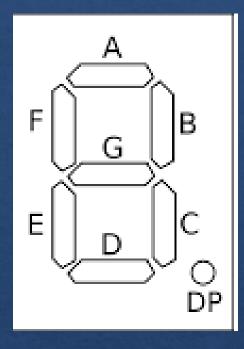




#### 1<sup>st</sup> 7-Segment

## Logic Design Project\_Design

	X	y	a	ь	С	d	e	f	g
8	0	0	1	1	1	0	1	1	1
8	0	1	1	0	0	0	1	1	0
8	1	0	1	0	0	1	1	1	1
٤	1	1	1	0	0	0	1	1	0

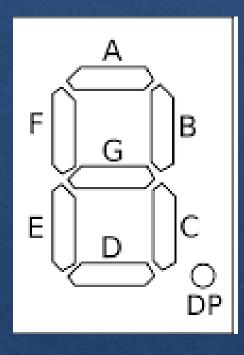


a=e=f=1	
b=c=x'.y'	
d=x.y'	
g=(x.y')'=d'	

#### 2<sup>nd</sup> 7-Segment

## Logic Design Project\_Design

	Х	y	a	ь	С	đ	e	f	g
5	0	0	1	0	1	1	0	1	1
8	0	1	1	1	1	1	1	1	0
S	1	0	1	0	1	1	0	1	1
U	1	1	0	1	1	1	1	1	0

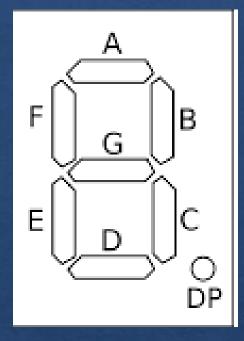


a=(x.y)'	
h=e=v	
f=c=d=1	
g=y'=b'	

#### 3<sup>rd</sup> 7-Segment

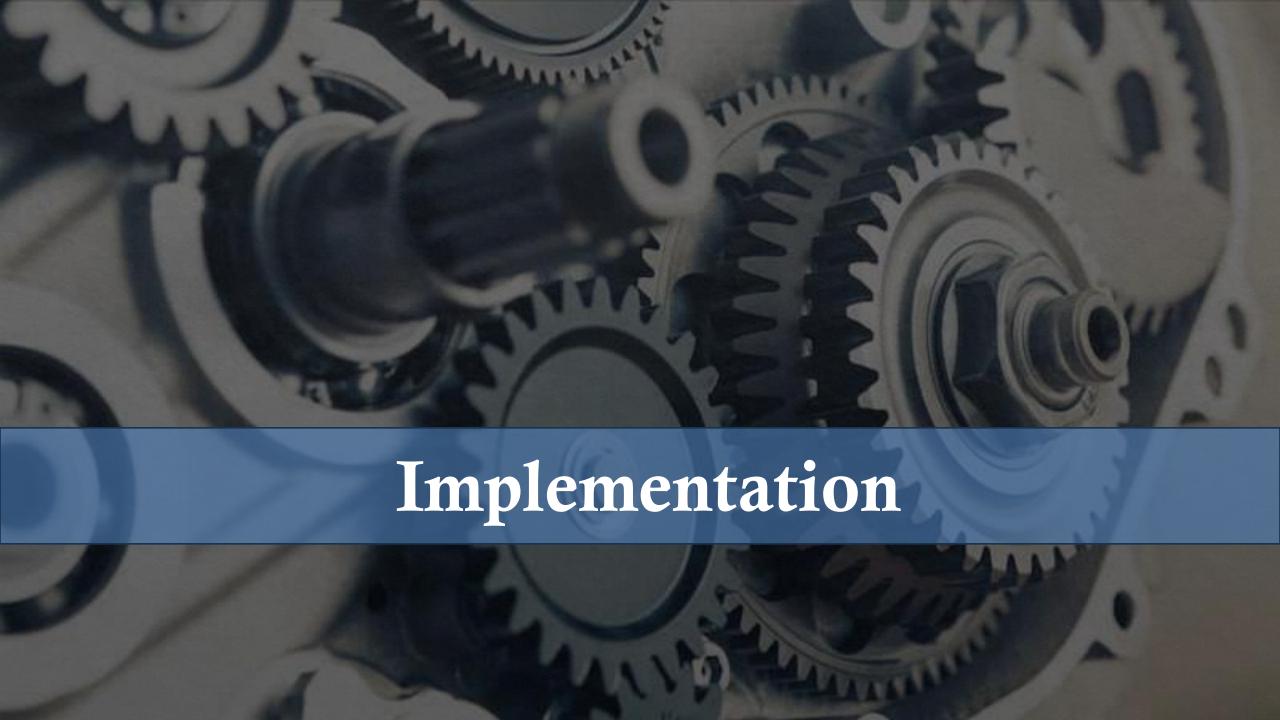
## Logic Design Project\_Design

	Х	y	a	ь	С	d	e	f	g
U	0	0	0	1	1	1	1	1	0
8	0	1	1	0	0	1	1	1	1
8	1	0	1	0	0	1	1	1	1
8	1	1	1	1	1	0	1	1	0



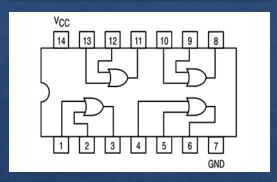
To minimize the number of ICs

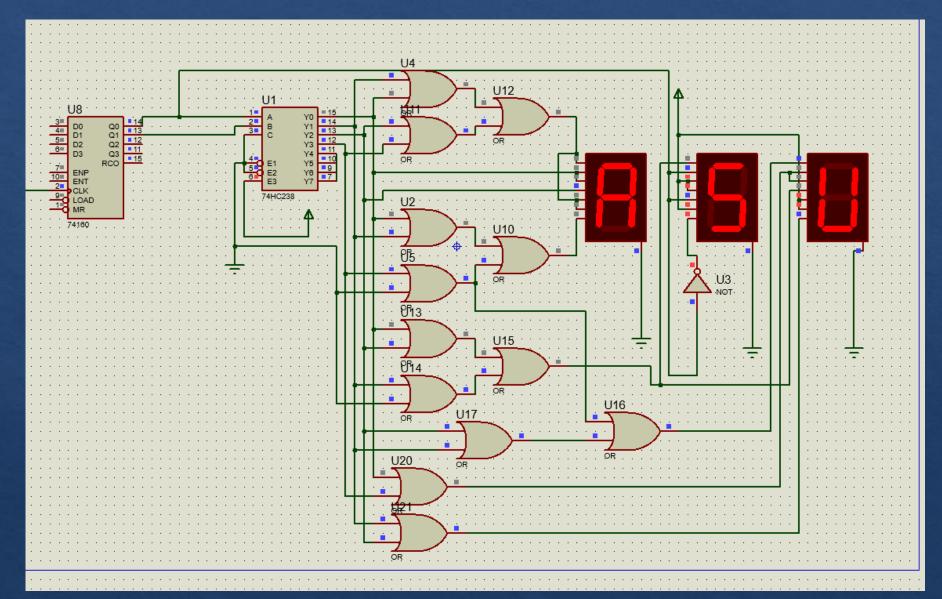
$$c=b=(x'.y'+x.y)'=((x'.y')'.(x.y)')'$$



# Design\_1 if we use decoder

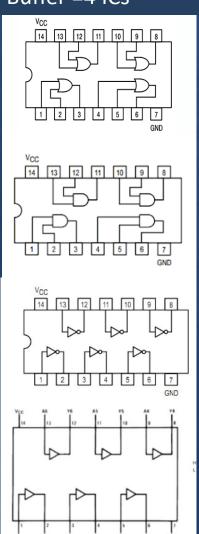
#### 13 OR gate =5 ICs

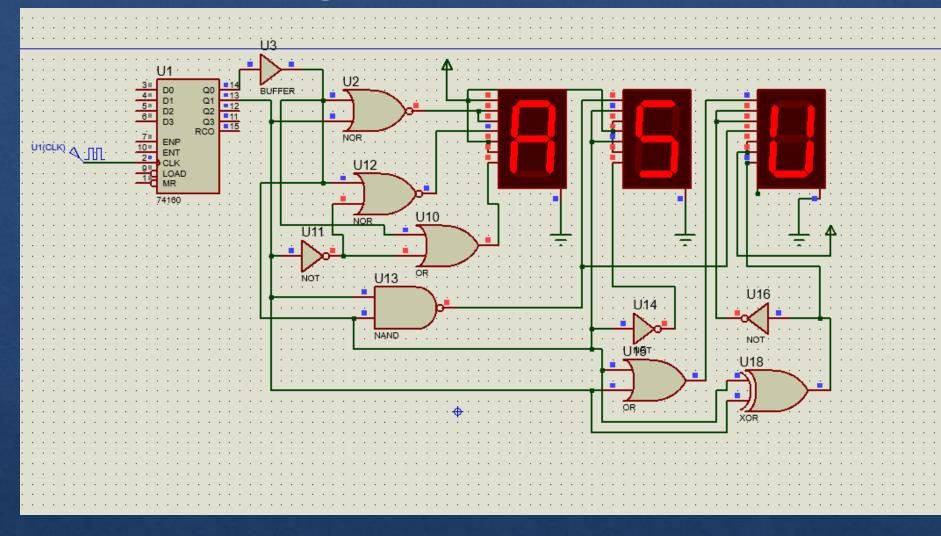




## Design\_2

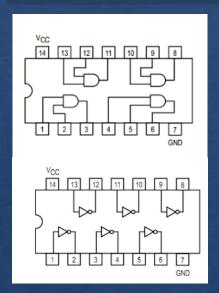
3 OR + 3NOT +1XOR +1 Buffer =4 ICs

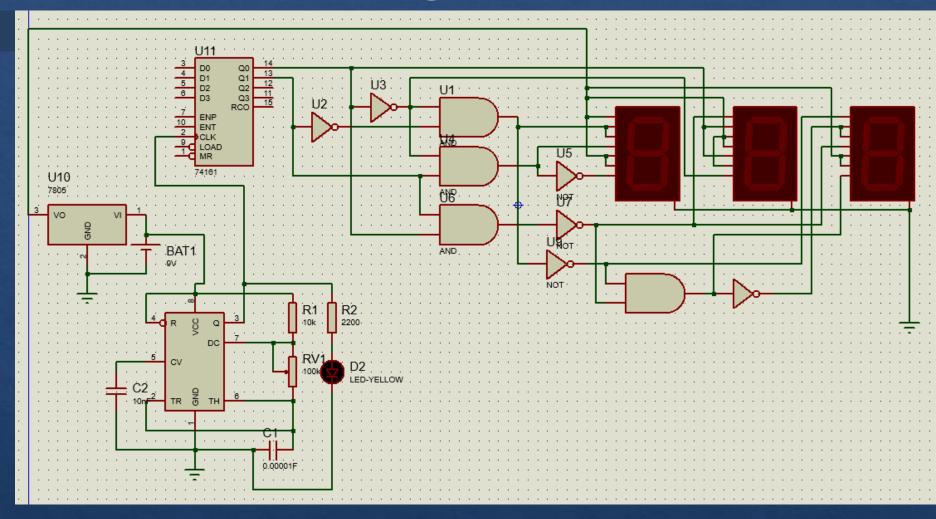




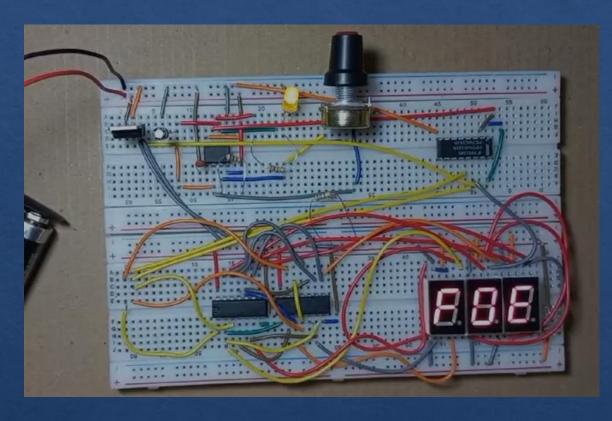
## The best Design

#### 6 Not + 4 AND = 2IC only





## The best Design







#### Cost

Product	quantity	Amount
IC 7408 – Quad 2 (AND)	1	10.00
IC 7404 – Quad 2 (NOT)	1	10.00
NE555N	1	6.50
IC 74161 – (counter_4-bit)	1	18.00
7 Segment 0.5 Common cathode	3	18.00
7805 (regulator)	2	10.00
Bread Board	2	70.00
Jumper wires	1	35.00
Mixed resistance	5	1.00
Mixed capacitors	4	1.50
Mixed Leds	4	2.00
500 K Potentiometer	1	4.50
9v Battery + clip	1	87.5
cover	1	16
Total	290.00	