

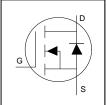
IR MOSFET Strong IRFET™ IRF60B217

Application

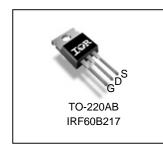
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free*
- RoHS Compliant, Halogen-Free



V _{DSS}	60V	
R _{DS(on)} typ.	7.3mΩ	
max	9.0mΩ	
I _D	60A	



G	D	S
Gate	Drain	Source

Dage next number	Deelse ve Tyree	Standard Pack Form Quantity		Standard Pack		Orderskie Dort Number
Base part number	Package Type			Orderable Part Number		
IRF60B217	TO-220	Tube	50	IRF60B217		

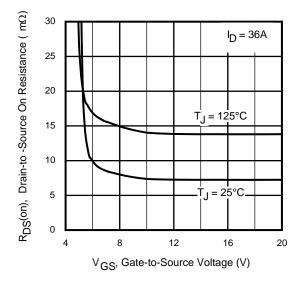


Fig 1. Typical On-Resistance vs. Gate Voltage

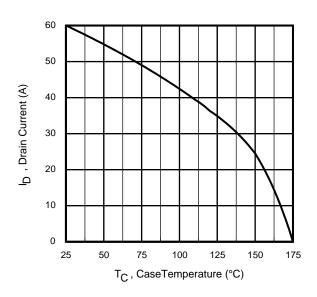


Fig 2. Maximum Drain Current vs. Case Temperature



Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, VGS @ 10V (Silicon Limited)	60	
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	42	Α
I _{DM}	Pulsed Drain Current ①	225	
$P_D @ T_C = 25^{\circ}C$	Maximum Power Dissipation	83	W
	Linear Derating Factor	0.56	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
Operating Junction and Storage Temperature Range		-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf∙in (1.1 N⋅m)	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	85	1
E _{AS (Thermally limited)}	Single Pulse Avalanche Energy ®	124	mJ
I _{AR}	Avalanche Current ①	Soo Fig 45, 46, 220, 22h	Α
E _{AR}	Repetitive Avalanche Energy ①	See Fig 15, 16, 23a, 23b	mJ

Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦		1.8	
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50		°C/W
$R_{\theta JA}$	Junction-to-Ambient		62	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{c}$	Breakdown Voltage Temp. Coefficient		0.047		V/°C	Reference to 25°C, I _D = 1mA ①
D	Static Drain-to-Source On-Resistance		7.3	9.0	m()	$V_{GS} = 10V, I_D = 36A \oplus$
$R_{DS(on)}$	atic Drain-to-Source On-Resistance		9.0		mΩ	$V_{GS} = 6.0V, I_D = 18A $ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.1		3.7	V	$V_{DS} = V_{GS}$, $I_D = 50\mu A$
ı	Drain to Source Lookage Current			1.0		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$
I _{DSS}	Drain-to-Source Leakage Current			150	μA	$V_{DS} = 40V, V_{GS} = 0V, T_{J} = 125$ °C
	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
I _{GSS}	Gate-to-Source Reverse Leakage			-100	IIA	$V_{GS} = -20V$
R_{G}	Gate Resistance		2.0		Ω	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- $\ \ \, \text{$\mathbb{Q}$ Limited by T_{Jmax}, starting $T_{J}=25^{\circ}$C, $L=0.131$mH, $R_{G}=50\Omega$, $I_{AS}=36$A, $V_{GS}=10$V.}$
- $\label{eq:local_spin_spin} \mbox{\ensuremath{\mbox{3}}} \quad I_{SD} \leq 36 A, \ di/dt \leq 630 A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \ T_J \leq 175^{\circ} C.$
- 4 Pulse width $\leq 400 \mu s$; duty cycle $\leq 2\%$.
- \circ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- © Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while VDS is rising from 0 to 80% VDSS.
- $\ensuremath{\mathfrak{D}}$ R₀ is measured at T_J approximately 90°C.



Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
gfs	Forward Transconductance	150			S	$V_{DS} = 10V, I_{D} = 36A$
Q_g	Total Gate Charge		44	66		$I_D = 36A$
Q_{gs}	Gate-to-Source Charge		12		nC	$V_{DS} = 30V$
Q_{gd}	Gate-to-Drain Charge		14		IIC	V _{GS} = 10V4
Q _{sync}	Total Gate Charge Sync. (Qg- Qgd)		30			
$t_{d(on)}$	Turn-On Delay Time		8.3			$V_{DD} = 30V$
t _r	Rise Time		37			$I_D = 36A$
$t_{d(off)}$	Turn-Off Delay Time		24		ns	$R_G = 2.7\Omega$
t _f	Fall Time		20			V _{GS} = 10V④
C _{iss}	Input Capacitance		2230			$V_{GS} = 0V$
Coss	Output Capacitance		215			$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance		140		pF	f = 1.0MHz, See Fig.7
C _{oss eff.(ER)}	Effective Output Capacitance (Energy Related)		230		PF	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V$
C _{oss eff.(TR)}	Output Capacitance (Time Related)		295			$V_{GS} = 0V$, $V_{DS} = 0V$ to $48V$ \bigcirc

Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)			60		MOSFET symbol showing the
I _{SM}	Pulsed Source Current (Body Diode) ①			225	l	integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage		0.9	1.2	V	$T_J = 25^{\circ}C, I_S = 36A, V_{GS} = 0V $ ④
dv/dt	Peak Diode Recovery dv/dt3		12		V/ns	$T_J = 175^{\circ}C, I_S = 36A, V_{DS} = 40V$
t _{rr}	Reverse Recovery Time		26		ns	$T_{J} = 25^{\circ}C \qquad V_{DD} = 51V$
rr .	Treverse recovery fillie		27		113	$T_J = 125^{\circ}C$ $I_F = 36A$,
0	Dayoroa Dagayary Charge		24		nC	$T_J = 25^{\circ}C$ di/dt = 100A/µs @
Q _{rr}	Reverse Recovery Charge		25		110	$T_J = 125^{\circ}C$
I _{RRM}	Reverse Recovery Current		1.7		Α	$T_J = 25^{\circ}C$



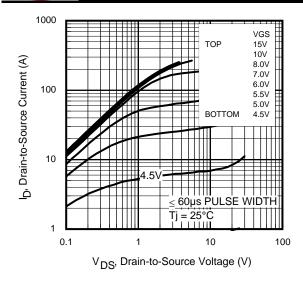


Fig 3. Typical Output Characteristics

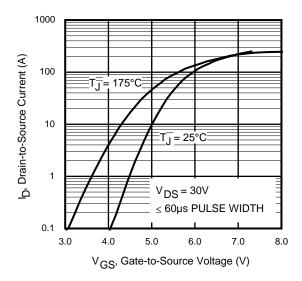


Fig 5. Typical Transfer Characteristics

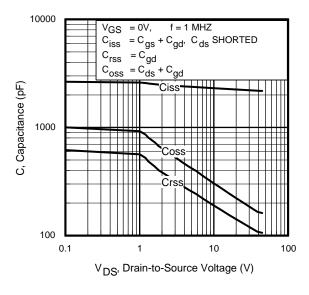


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

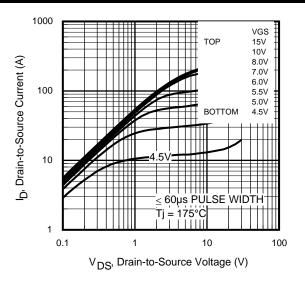


Fig 4. Typical Output Characteristics

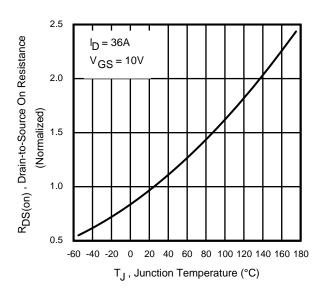


Fig 6. Normalized On-Resistance vs. Temperature

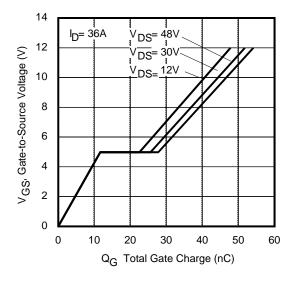


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage



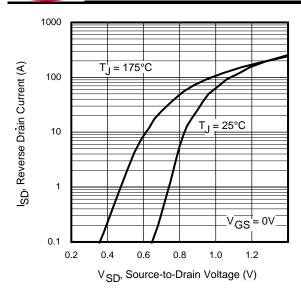


Fig 9. Typical Source-Drain Diode Forward Voltage

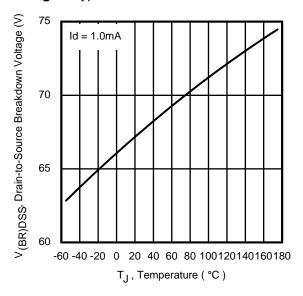


Fig 11. Drain-to-Source Breakdown Voltage

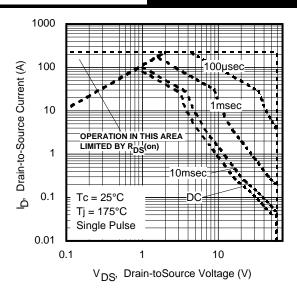


Fig 10. Maximum Safe Operating Area

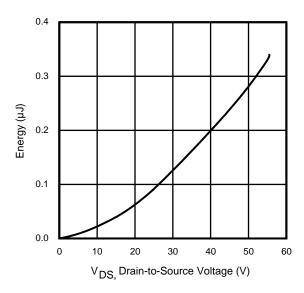


Fig 12. Typical Coss Stored Energy

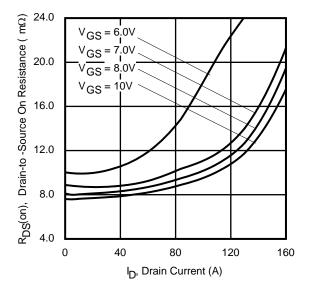


Fig 13. Typical On-Resistance vs. Drain Current



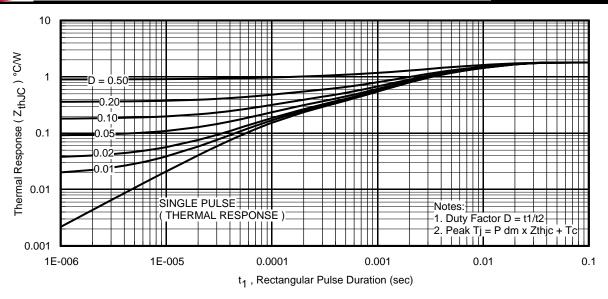


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

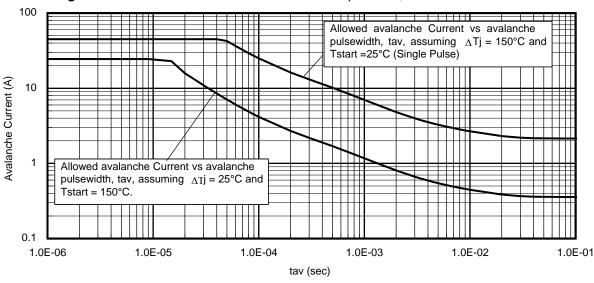


Fig 15. Avalanche Current vs. Pulse Width

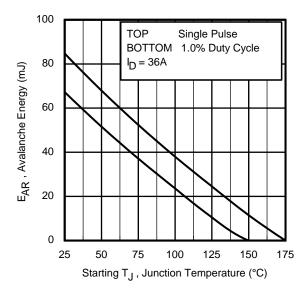


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:

Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.

- 2. Safe operation in Avalanche is allowed as long asT_{imax} is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures
- 4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
- 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. I_{av} = Allowable avalanche current.
- 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14) PD (ave) = 1/2 ($1.3 \cdot BV \cdot I_{av}$) = $\Delta T / Z_{thJC}$

 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

 $E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$



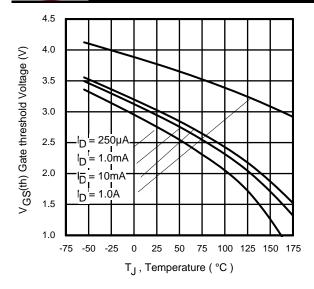


Fig 17. Threshold Voltage vs. Temperature

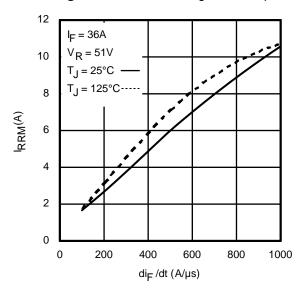


Fig 19. Typical Recovery Current vs. dif/dt

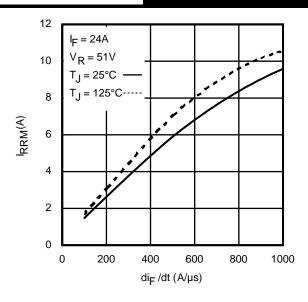


Fig 18. Typical Recovery Current vs. dif/dt

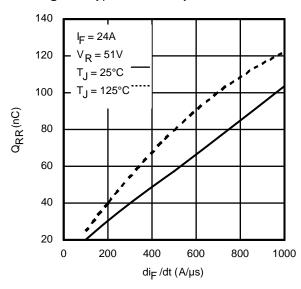


Fig 20. Typical Stored Charge vs. dif/dt

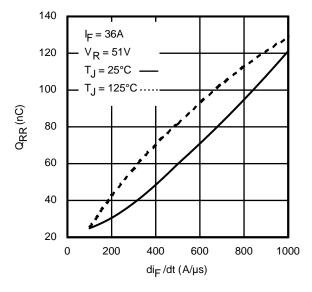


Fig 21. Typical Stored Charge vs. dif/dt

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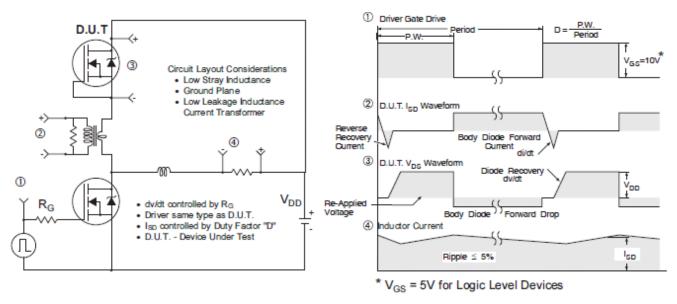


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

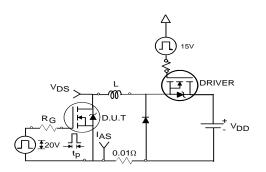


Fig 23a. Unclamped Inductive Test Circuit

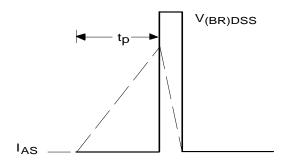


Fig 23b. Unclamped Inductive Waveforms

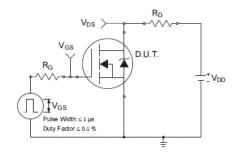


Fig 24a. Switching Time Test Circuit

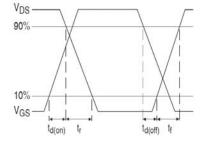


Fig 24b. Switching Time Waveforms

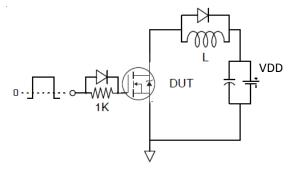


Fig 25a. Gate Charge Test Circuit

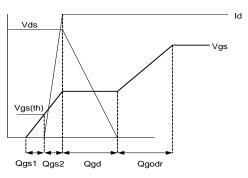
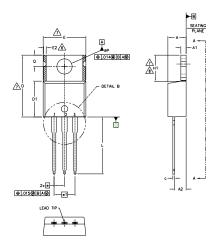


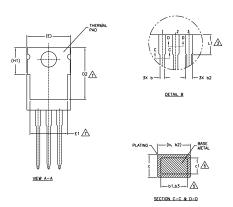
Fig 25b. Gate Charge Waveform

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TO-220AB Package Outline (Dimensions are shown in millimeters (inches))





NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- LEAD DIMENSION AND FINISH UNCONTROLLED IN LI
- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5. DIMENSION 61, 63 & c1 APPLY TO BASE METAL ONLY.
 - CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	MILLIM	ETERS	INC	HES	
	MIN.	MAX.	MIN.	MAX.	NOTES
Α	3.56	4.83	.140	.190	
A1	1,14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
ь	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1,14	1.78	.045	.070	
b3	1,14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	_	.030	8
e	2.54		.100		
e1	5.08	BSC	.200		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØΡ	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

<u>HEXFET</u>

1.- GATE 2.- DRAIN 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE 2.- COLLECTOR 3.- EMITTER

DIODES

1.- ANODE 2.- CATHODE 3.- ANODE

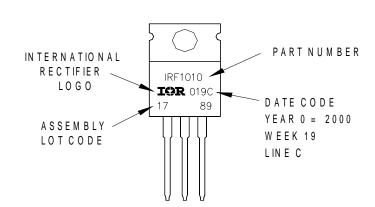
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010

LOTCODE 1789

ASSEMBLED ON WW 19,2000 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

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Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ††			
Moisture Sensitivity Level	TO-220 N/A			
RoHS Compliant	Yes			

- † Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/
- †† Applicable version of JEDEC standard at the time of product release.

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