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Report about Single Phase Inverter

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Abstract

This project details the design and construction of a single-phase inverter for educational purposes. The key aspect lies in the implementation of Pulse-Width Modulation (PWM) control digitally using a microcontroller.

While integrated circuits offering single-phase inverters exist, a discrete component approach is chosen to enhance the learning experience. This allows for a deeper understanding of each component's function and the visualization of internal signal waveforms.

The project begins with a comprehensive theoretical analysis covering inverter applications and fundamental components. Following this, the desired inverter specifications are defined, enabling the calculation and selection of necessary components.

A crucial aspect involves programming the microcontroller to generate the PWM signal. This section explores the microcontroller's capabilities, develops various code options, and selects the most suitable one for the application.

Subsequent to the theoretical groundwork, the complete circuit is first simulated using LTSpice software and then built on a breadboard. Performance and efficiency are evaluated through measurements. Finally, the project culminates in the design and development of a Printed Circuit Board (PCB) for the complete inverter.

Contents

Chapter 1

Single – Phase Inverter

This chapter presents the general topic of this work: the **single phase inverter**. Not only definition, but applications and components are described in those pages.

The main **topologies** available for inverters will also be discussed, in order to justify the final decision of a Full Bridge configuration. Also, an insight into its main component, the **elementary switching cell**, is given.

Within the elementary switching cell, **semiconductors** are the devices responsible for its operation. Due to their importance, a brief description of the main types, covering structures and schematics is included. Also, a final comparison depending on frequency and power can be found.

An important block in this chapter is the **PWM modulation**. After a first definition and explanation, the two main options for modulation are described: bipolar and unipolar.

Finally, other parts of the inverter are commented, as the **driver** and the **filter**.

2.1 Definition

A power inverter, or inverter, is an electronic device or circuitry that changes **direct current** (DC) into **alternating current** (AC).

Depending on the number of phases of the AC output, there are several types of device. **Single- phase** and **three-phase** inverters are the most common configurations. Figure 2.1 shows a schematic of their basic performance.

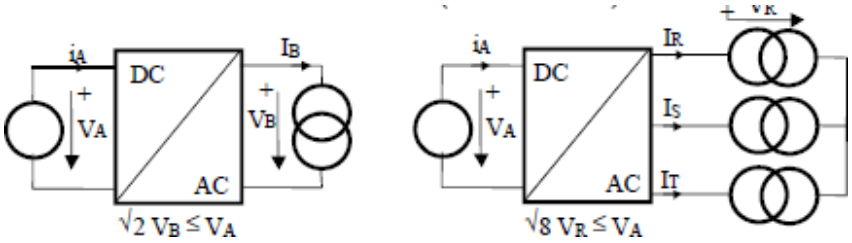


Figure 2.1: Single - phase and three – phase voltage inverters

2.2 DC - AC current

Technically, there are two ways in which electricity can be transmitted: direct current and alternating current.

Direct Current (DC) is the unidirectional flow of electric charge. If a constant voltage is applied across a circuit, it results in a constant current. DC can be produced by different sources, being batteries the most common ones. Also dynamos, power supplies or solar cells are examples of DC generators.

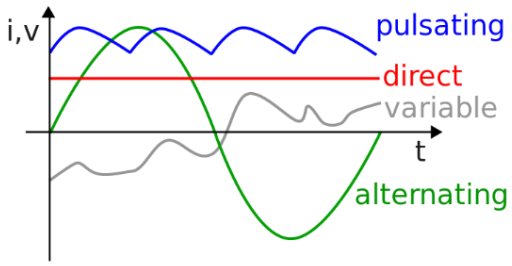


Figure 2.2: Direct and alternating current and voltage

On the other hand, in **Alternating Current (AC)** the flow of electric charge periodically reverses its direction. The most usual waveform of AC is a sine wave, but it can also be triangular or square wave.

In order to transfer electrical power into different kinds of current, special devices are required. Converters AC/DC are called **rectifiers** and **inverters** are DC/AC converters. It is important to do this transformation in the most efficient way in order not to lose energy.

Another important issue to consider is **frequency**. In a DC voltage, given that the voltage value is constant, frequency is zero. However, when AC voltage is involved, it is necessary to define the number of repetitions per unit of time of a periodic event, that is to say, the frequency. **Period** is the inverse of frequency, and it can be defined as the amount of time required in order to complete a repetitive cycle.

2.3 Applications

When it comes to transform a source of Direct Current into an Alternating Current, the amplitude of output and input do not need to be the same. The most widespread converters are the **voltage inverters**, also called power-reducers, as the output voltage is lower than the input.

Sometimes combined with boost converters, inverters are used in a wide range of applications, as injection of energy to the grid on renewable energies, isolated generation or electric drives.

An example for this is electricity generation with solar cells. When sun light reaches a cell, electrons are released. Applying an electric field, they can be taken out and result in a DC current. In order to put this electricity on the grid, an inverter is needed. Another example is an AC device connected to a battery as power source. Given that direct connection is not possible, an inverter is required as an intermediate device.



Figure 2.3: Examples of applications

2.4 Output: modified sine wave and pure sine

With regard to their output, two different types of power inverters can be found: modified sine wave and pure sine wave.

On **modifying sine wave** inverters, the output waveform is similar to a square but with a null period between positive and negative values. Due to its high distortion levels, it is not commonly used, as some devices do not work properly with it.

On the other hand, a **pure sine inverter** provides a sinusoidal waveform, requiring more complicated circuitry but assuring better efficiency and lower distortion than the previous type. The majority of the inverters are pure sine inverters, given that their output can be applied to all loads.

The differences between both waveforms can be appreciated in Figure 2.4. Also, a square wave is included in order to establish a reference for comparison. It can be seen that the modified sine is the intermediate waveform between the square and the sine. While modified sine rises or falls instantaneously after sitting at zero for a moment, the pure sine waveform passes through all values between minimum and maximum, resulting in a smoother input for the load.

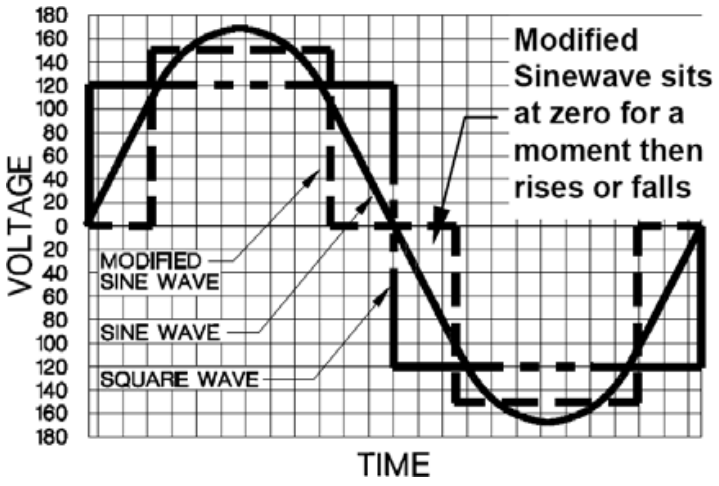


Figure 2.4: Square, modified and sine wave

2.5 Semiconductors. Selection of interrupters

Power semiconductors are the main part of the switching cell. The inverter's features depend largely on their performance and characteristics.

Basically, all semiconductors consist of **PN junctions**. Those are achieved doping silicon with boron (P layer) or phosphorus (N layer). When a certain voltage is applied to the junction, the internal charges move, letting the current flow through it. If the voltage is not enough, the charges do not flow and therefore the semiconductor acts like a blocker. An ideal semiconductor would perform as an **ideal switch**, being its main characteristics on- and off-control, instantaneous switching, null impedance in conducting and infinite impedance in cut-off. Also, reversibility regarding current and voltage and the voltage range in conducting are issues that define a semiconductor.

In this section, a brief insight into different semiconductors will be given.

2.5.1 Types of semiconductors

- **DIODE**

A diode consist of a single PN junction. It is the simplest semiconductor and has no on- and off- control. Its symbol and structure are reflected in Figure 2.7.

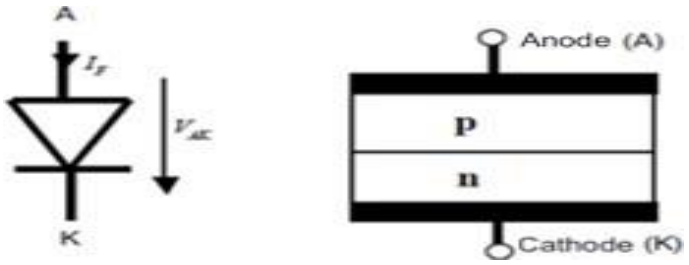


Figure 2.7: Symbol and structure of a diode

When a positive voltage over a specific value (Threshold voltage) is applied between P (anode) and N (cathode) it conducts, whereas a negative voltage results in the cut-off of the diode. However, there is a limit for negative voltage applied, as the PN junction can be broken. Figure

2.8 shows the **static characteristic** of a diode. Three main areas can be observed: forward direction (diode conducting), blocking area (diode cut) and break through (diode destroyed).

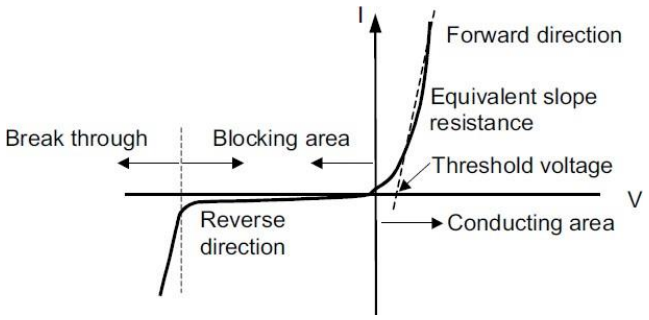


Figure 2.8: Current-voltage characteristics for a diode

- **BJT**

Two PN junctions result in a **Bipolar Junction Transistor** (BJT). The basis of this semiconductor is to amplify current. Applying a positive voltage between collector (C) and emitter

(E) is not enough to make it conduct. Therefore, it is required to introduce a positive current on the base in order to achieve current circulation, with a base-to emitter voltage (V_{BE}) over the threshold value.

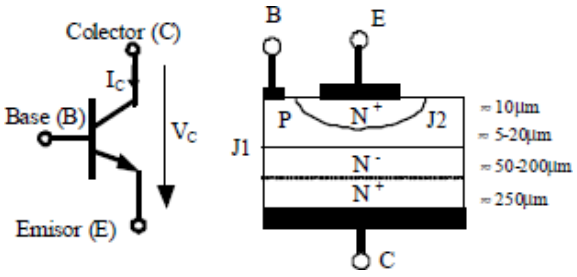


Figure 2.9: BJT symbol and structure

BJTs have current gains in the order of 10 for comparatively high voltage drops. As one of their drawbacks, it is necessary to introduce high currents on the base in order to make the device work in the forward-active area (amplification of current). Also, high reverse base drive currents are required to obtain a fast turn-off. For these reasons, they are not commonly used in power electronics.

- **MOSFET**

The **Metal Oxide Semiconductor Field Effect Transistor** or MOSFET is a voltage controlled semiconductor, unlike BJT, that is current controlled.

There are two types of MOSFETs: channel N and channel P, but this last one is not commonly used in power electronics. The voltage control is between gate and source, and normally must be above 10 Volts in order to switch on the semiconductor. Structure and symbol of an N-Channel MOSFET are shown in Figure 2.10.

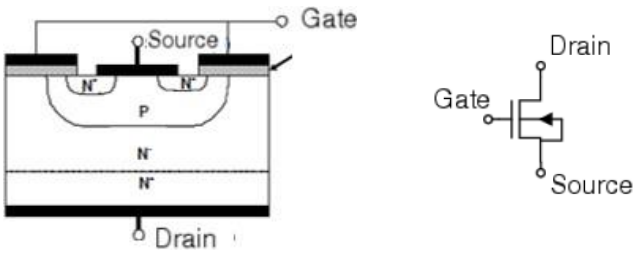


Figure 2.10: Structure and symbol of an N-Channel MOSFET

Basically, in order to turn it on, a voltage between gate and source (V_{GS}) must be applied. This fact, together with a positive voltage between drain and source (V_{DS}), result in an electron channel that allows a current flow in the drain (I_D).

This semiconductor is commonly used in low voltage and low power applications, as microelectronics. Also, when a high switching frequency is required.

Regarding their static behaviour, reflected in figure 2.11, MOSFETs can operate between the breakdown voltage and the maximum direct voltage. Below and over these values, the semiconductor gets into avalanche and the junctions are destroyed. When conducting in the ohmic region, MOSFETs behave as a resistor, amplifying the current. On the other hand, in the active region the current is linear.

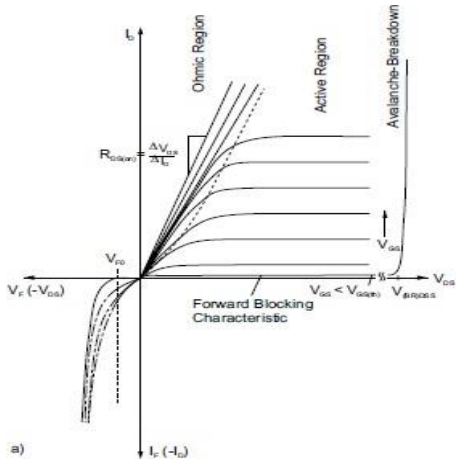


Figure 2.11: Static behaviour of an N-Channel MOSFET

- **POWER-MOSFET**

As a concrete type of MOSFETs, Power MOSFETs are specially designed to handle higher power levels. Due to their low gate drive power, fast switching speed and good paralleling capability, they are commonly used in power electronics.

The most common structure in Power MOSFETs is the **Vertical Diffused MOS (VDMOS)**, with the source electrode over the drain, which results in a vertical current when the device is conducting. Whereas Lateral Diffused MOS (LDMOS) are mainly used in high-end audio amplifiers, VDMOS are the option normally selected for switching applications.

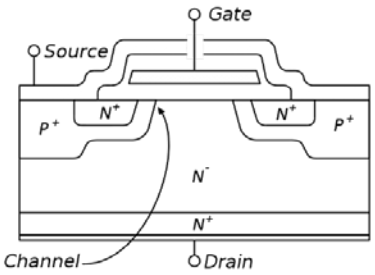


Figure 2.12: Cross section of a VDMOS, showing an elementary cell

The source metallization connects N^+ and P implantations, creating a diode between the drain (cathode) and the source (anode) of the MOSFET. This **body diode** can be employed as freewheeling diode in H-Bridge configurations.

The main difference between Power MOSFETs and normal MOSFETs is the current capacity and the gate capacitance. Whereas normal MOSFETs perform better in higher frequencies, Power MOSFETs are a better option regarding high current and voltage applications. Also, power MOSFETs have much lower resistance while conducting, minimising conducting losses.

- **IGBT**

The **Insulated Gate Bipolar Transistor** is similar to a MOSFET but with a third PN-junction. This allows controlling it with voltage, as a MOSFET, but with output characteristics similar to a BJT regarding high loads and low saturation voltage. Its schematic structure and symbol are reflected in Figure 2.13.

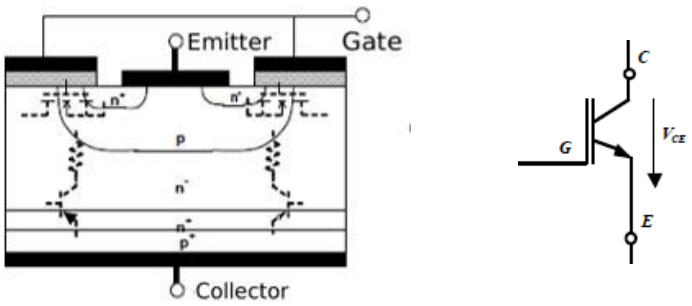


Figure 2.13: Structure and symbol of an IGBT

Four main regions can be observed on its **static behaviour**. From the left to the right in figure 2.14, the avalanche region is the area when a voltage below breakdown voltage is applied, resulting in the destruction of the IGBT. The **cut area** includes values from breakdown voltage up to threshold voltage. The IGBT does not conduct in this region. On the **saturation** region, the IGBT behaves as a voltage source and a series resistance. With low variations of voltage, high amplification of current can be achieved. This area is the most desirable for working. If the voltage is augmented, the IGBT enters in **active** region, and current remains constant. There is a maximum voltage applied in order the IGBT not to enter in avalanche.

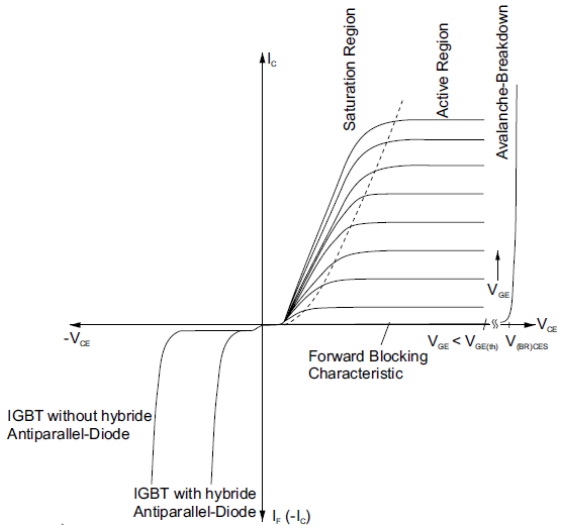


Figure 2.14: Static behaviour of an IGBT

It is the most used semiconductor in power electronics, given that it can support a wide range of voltage from few volts to kV and powers between kW and MW. Also, in applications with switching frequencies lower than 20 kHz, it is the semiconductor commonly selected.

2.5.2 Selection of semiconductors for an inverter

The selection of the interrupters depends on the reversibility required for the voltage and the current source. On an inverter, it is only necessary current reversibility. Hence, an interrupter of **three segments** must be chosen.

Selecting a **transistor and a diode in antiparallel**, the turning-on of the transistor can be controlled with voltage. When the voltage applied is positive and an on-order is given, the transistor conducts and the current is positive. If the voltage is negative, the diode conducts and the current is negative.

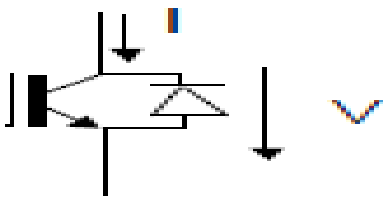


Figure 2.16: Semiconductors chosen

Whereas the diode is always in a switching cell, different **transistors** can be chosen. Criteria applied for the decision regards applications, switching frequency, velocity and voltage required. On Chapter 3, a discussion about the best semiconductor to choose will be held.

2.6 Inverter topologies: Half - Bridge and Full - Bridge

Regarding inverters, there are several topologies available, being the most common ones Half Bridge and Full Bridge. This section collects a brief explanation of them.

2.6.1 Half - Bridge

In this topology, only **two switchers are required**. The DC input is divided in two identical sources and the output is referenced to the middle point.

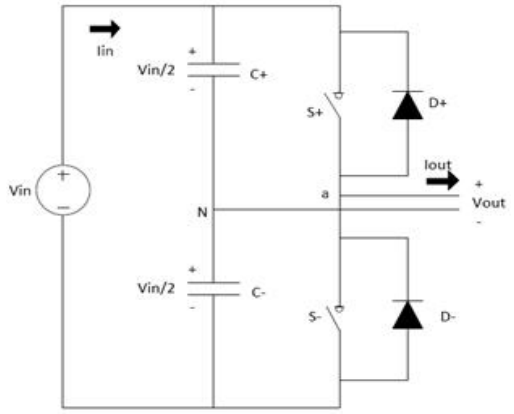


Figure 2.17: Single-phase Half-Bridge voltage inverter

A **capacitor divisor** is used to achieve the medium voltage point (N). By controlling the voltage in N, direct current injected in the alternate side is assured to be zero.

In addition to this, only one switching cell is required. Therefore, it is a cheap alternative and the conducting losses are not excessively high.

On the other hand, in order to obtain the same value of power, higher currents are required, as voltage is lower. In case a high voltage is needed in the output, an elevator is commonly used as first step, as the input voltage must be double than the output desired. Regarding switching losses, the semiconductors must be designed for 2Vout. This fact makes this topology the **worst in performance**, as switching losses become excessively high.

2.6.2 Full H-Bridge

In a Full H-Bridge, the alternate output voltage (Vab in Figure 2.18) is obtained by the difference between two branches of switching cells. Therefore, **four switchers** are needed. To maximize the fundamental component of the output voltage, the fundamental component of the voltage on each branch (Vao and Vbo) must be 180º out of phase. The semiconductors of each branch are complementary in performance, which is to say when one is conducting the other is cut-off and vice versa. This topology is the most widely used for inverters.

The semiconductors must be designed only for Vout, but as a disadvantage, four switchers are required and therefore, losses can become elevate.

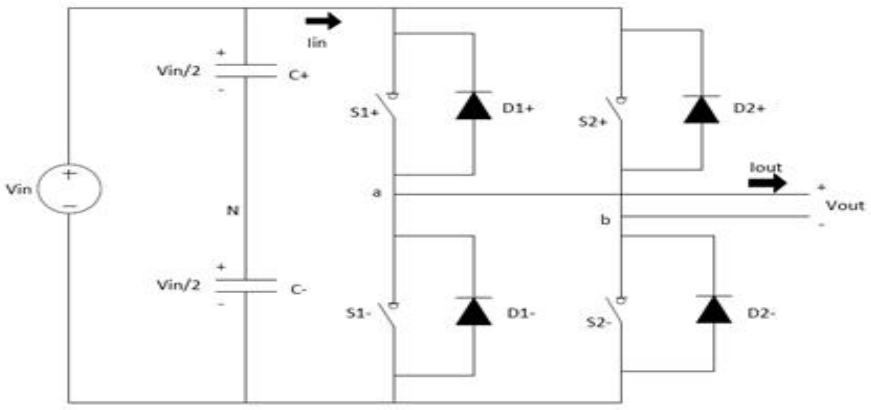


Figure 2.18: Single-phase Full H-Bridge voltage inverter

2.7 PWM Modulation

In order to obtain the connection function for the semiconductors, a modulation technique called PWM is employed. The basics of **Pulse Width Modulation** (PWM) is the variation of the duty cycle of a periodic signal. The duty cycle (D) is defined as the variation of the positive part of the signal (T_{on}) related to the period (T).

$$D = \frac{T_{on}}{T}$$

In analog circuitry, a PWM is obtained comparing a signal control (V_{con}) with a triangular wave. For this purpose, normally a comparator is used. Thus, the output will be 1 if the positive leg of the comparator is higher than the negative one and 0 if it is lower. Figure 2.19 reflects schematic and waveforms obtained in an analogical PWM circuit.

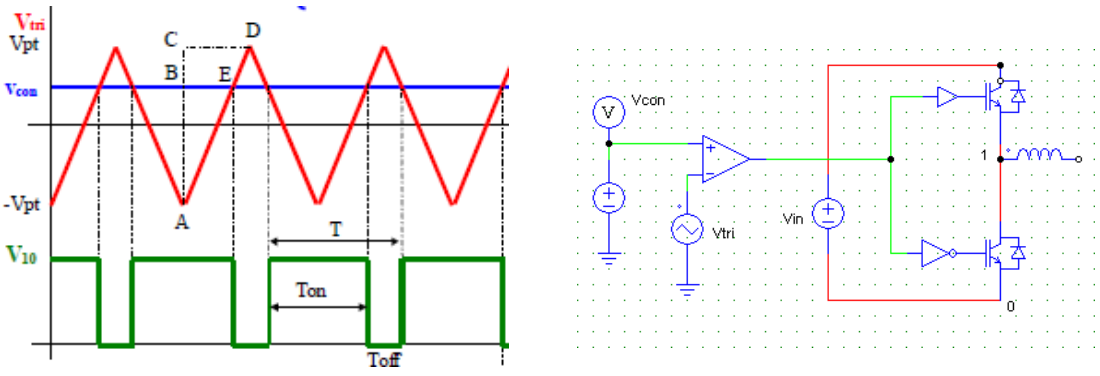


Figure 2.19: PWM waveforms and schematic.

It must be pointed out that with constant Vcon only a fixed duty cycle can be obtained. For the purpose of having a **varying duty cycle**, the signal control must be **sinusoidal**. This way, as Vcon is not constant, the positive part relating to the period changes. Hence, two frequencies must be considered. Vcon oscillates normally at the **output desired frequency**, which is usually a low value, 50 or 60 Hz. Also, it is necessary to determine the frequency of the triangular wave. This frequency is directly related to the **switching frequency** of the semiconductors, and must be carefully chosen. Normally, the value selected is over 20 kHz, in order to overcome the human hearing threshold.

Basically, there are two main techniques to obtain a PWM: bipolar and unipolar modulation. Both can be applied to a Full H-Bridge, and will be studied in the following section. The high-side interrupters are named K1 and K3 and the low-side are K2 and K4.

2.7.1 Bipolar Modulation.

In bipolar modulation, the output voltage oscillates between two values (Vdc and –Vdc in Figure 2.20), hence its name.

A basic schematic of a Full H-Bridge with bipolar modulation is collected in Figure 2.20. It can be seen how in this modulation, the connection function is the same for K1 and K4 and for K2 and K3. This means, only **one signal control is required**. As the switchers are complementary in performance on each branch, the connection function must be inverted in order to achieve this.

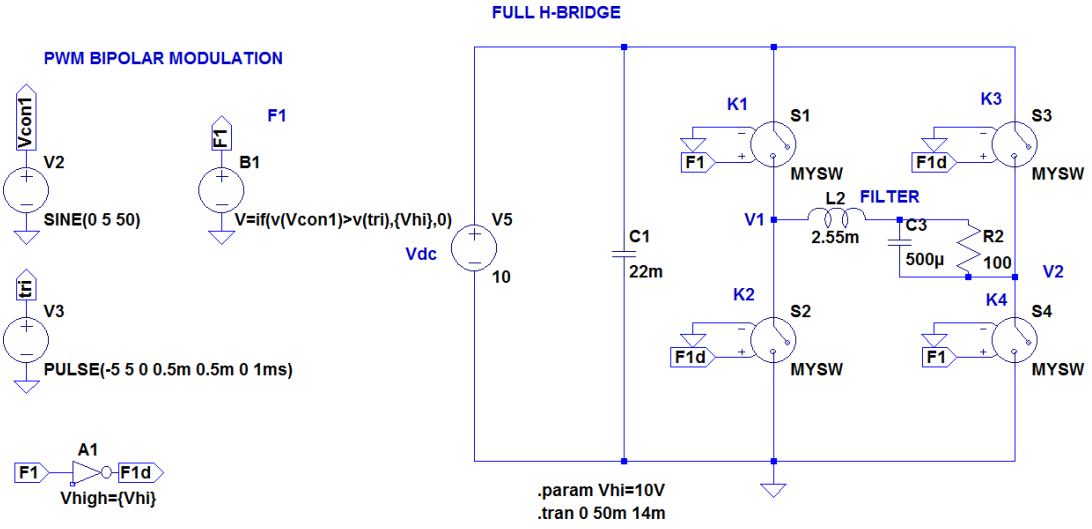


Figure 2.20: Analogic circuitry for bipolar modulation in LTSpice software

The connection function, and therefore the switching of the MOSFETs depend on the difference between the

control voltage (Vcon) and the triangular wave (Vtr). The following schematic resumes the performance of bipolar modulation.

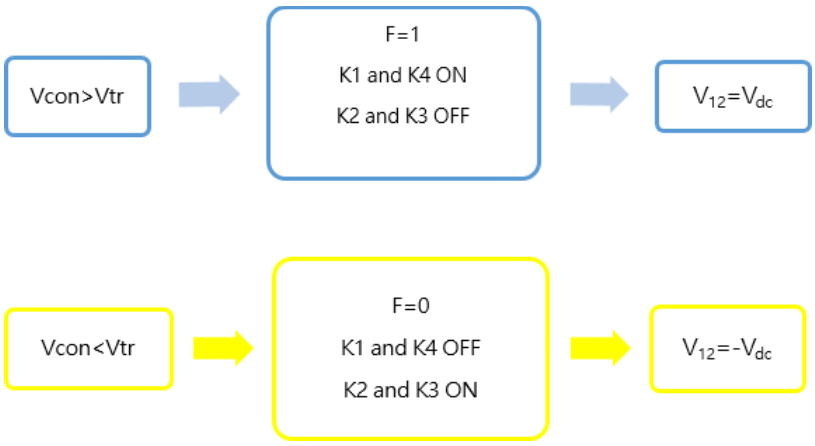


Figure 2.21: Resume of bipolar modulation.

Also, the main waveforms are collected in Figure 2.22: Vcon (sinusoidal control voltage), Vpt (triangular voltage) V10 and V20 (voltage on the low side switchers of each branch), V12 (output voltage without filtering) and iL (current on the inductance).

The output voltage (V12) results from the difference between voltages in both legs. It oscillates between **two levels**, Vdc and –Vdc. Its period is the same as the switching one, as it can be seen in Figure 2.22.

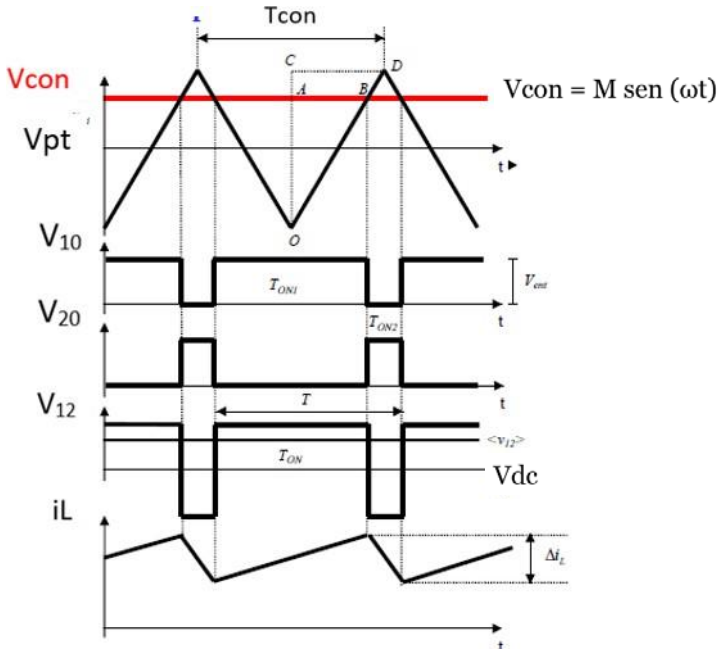


Figure 2.22: Main waveforms of bipolar modulation.

In bipolar modulation, the output voltage **switching harmonics** are the sum of the switching harmonics of

both branches. In order to reduce them, an option is increasing switching frequency, as this eases the filtering. However, as a result the switching losses may become too large.

An important advantage of this modulation is the **constant voltage to ground** (common mode voltage), which make bipolar modulation the one preferred in applications as photovoltaic systems without transformer.

2.7.2 Unipolar Modulation.

Unlike bipolar modulation, in case unipolar modulation is implemented in a circuit, the connection function is **different in both branches**. Given that the switchers must be complementary in performance, both branches of the bridge are related by the triangular voltage. Furthermore, the sinusoidal control voltage is opposite in sign in both legs.

$$V_{con1} = -V_{con2}$$

Figure 2.23 shows a simple schematic of the implementation of unipolar modulation with LTSpice software.

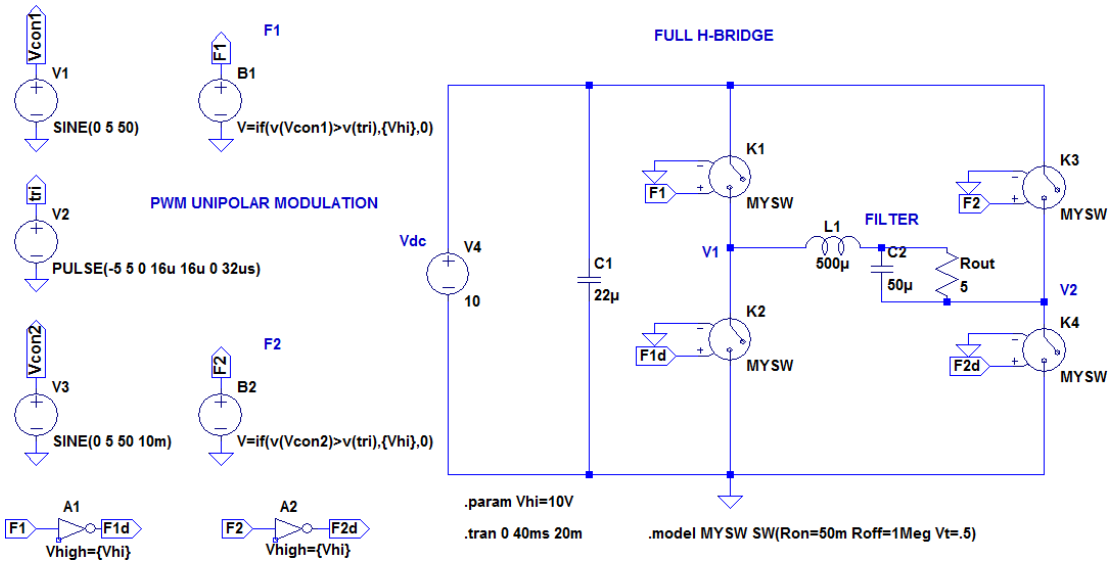


Figure 2.23: Analogic circuitry for unipolar modulation in LTSpice software.

The operation of the connection functions is the same as in bipolar, but instead of having two levels of voltage in the output, there are **three**: Vdc, 0 and –Vdc. This way, the output is **more accurate** than in bipolar modulation. A resume of the performance of unipolar modulation is collected below (Figure 2.24). Also, the main waveforms can be observed in Figure 2.25.

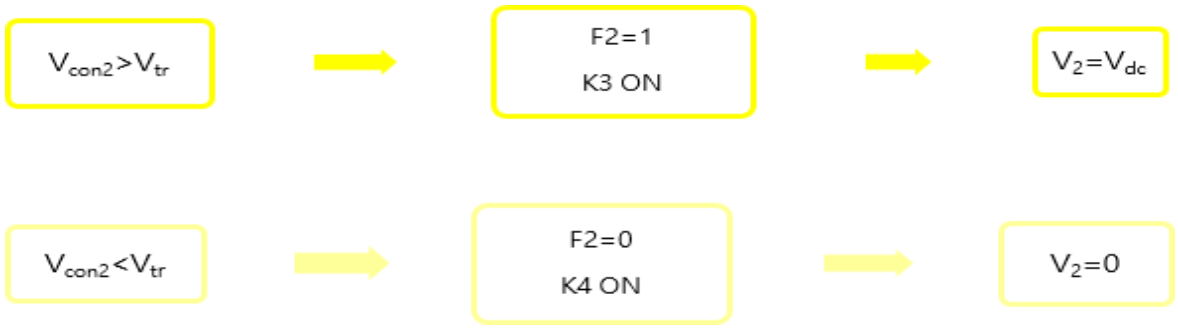


Figure 2.24: Resume of unipolar modulation.

The period of the output voltage is half the switching one and therefore the **output frequency** doubles the switching one. As the **harmonics** are in a higher frequency, for the same switching frequency the output inductance can be smaller than in bipolar modulation.

Also regarding harmonics, as the output voltage results from the difference between branches, the even families of harmonics have double amplitude, given that they are 180º out of phase on each branch. On the other hand, the odd families are in phase and do not appear in the output.

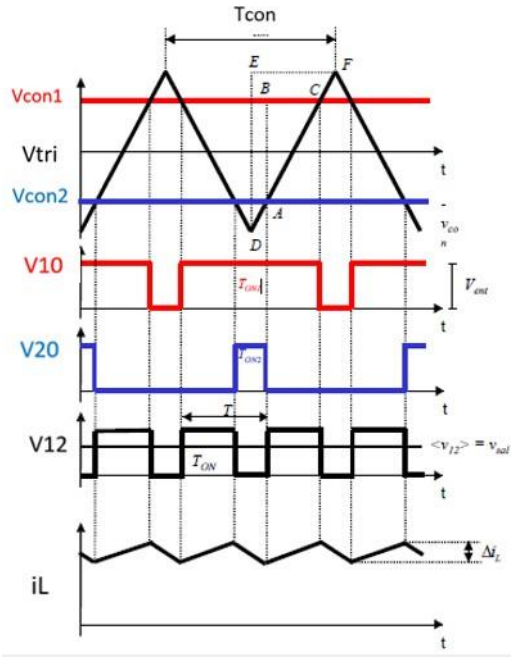


Figure 2.25: Main waveforms of unipolar modulation [1]

Unlike bipolar modulation, unipolar modulation has only one sign on each semiperiod, hence its name. The comparison between both modulations and their outputs is reflected in Figure 2.26. It can be appreciated how the filtered waveform (sinusoidal) is clearer with unipolar modulation. Also the difference between output levels (two in unipolar and three in bipolar) can be seen.

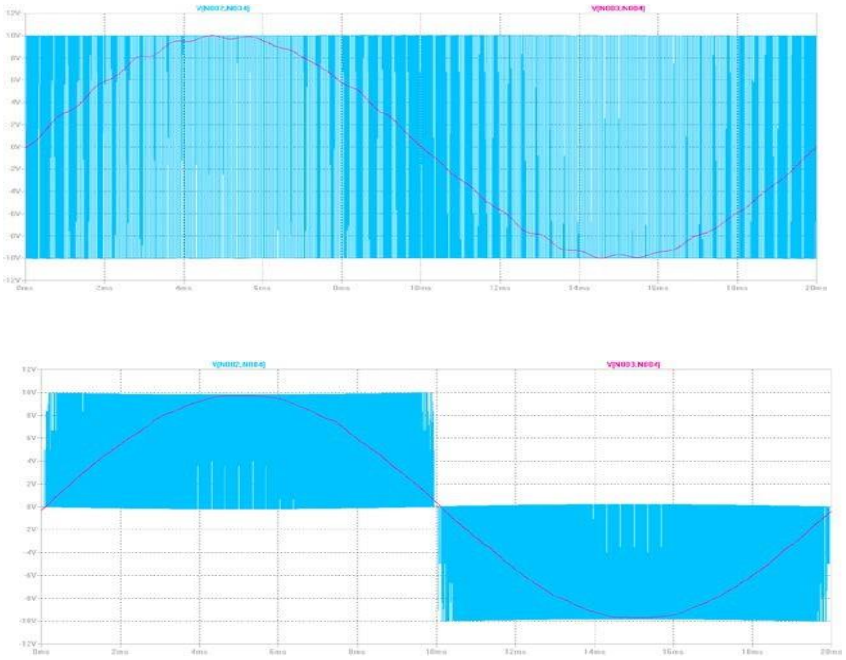


Figure 2.26: Output waveform with bipolar modulation (up) and unipolar modulation.

2.8 Driver

A driver is a device which adapts the connection function to the requirements of the semiconductors. As the connection function only oscillates between two values, sometimes it is necessary to modify the signal in order not to damage the semiconductors.

Main functions:

- Amplification of the control signal in order to adapt it to the desired levels of voltage and current.
- Galvanic isolation: to avoid electrical contact between two parts of the circuit.
- Protection against low feeding voltages or current that could damage the semiconductors.

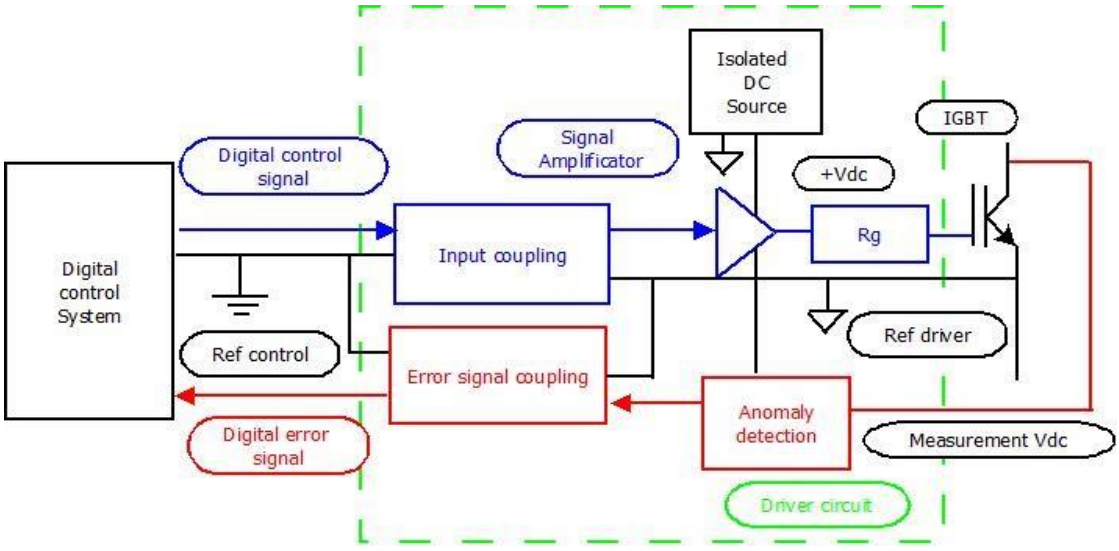


Figure 2.27: Functional schematic of a driver [1]

2.9 Filter

The output voltage is the difference between voltages in the two branches of the bridge. Its waveform is **squared** and therefore a filter is required in order to obtain a sine. Also, it contains a large number of harmonics, which may disturb the correct operation of the output load connected.

A filter is basically a circuit which modifies frequency components between its input and output. It can be analogic or digital and depending on its behaviour, there are mainly four types.

Table 2.2: Types of filters and main features.

Type of filter	Features
Low pass	They let pass low frequencies and attenuate the ones over a cut point
High pass	They attenuate frequencies below a cut point
Band pass	They let pass frequencies between a range
Band rejection	They block frequencies between a range

Once the type of circuit is selected, the cut point and the ranges of frequencies can be chosen by modifying the components.

As in this case the objective is to **attenuate harmonics**, a **low pass filter** will be selected. For a low pass filter, there are two options regarding circuitry: RC (resistor – capacitance) or LC (inductance – capacitance).

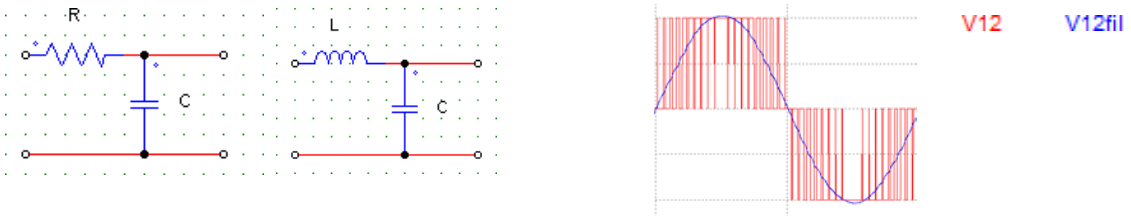


Figure 2.28: RC and LC low pass filters and waveforms.

In Figure 2.28 the output waveform of an inverter before and after an LC filter can be observed. To select the components, it is necessary to determine maximum ripple current, ripple voltage and cut frequency.

Chapter 3

Design

The aim of this chapter is to gather all the design aspects on an inverter. First of all it is necessary to make an approach to the specific features of the problem. Also, a detailed description of the design criteria is developed, that is to say, which aspects are the most important regarding the quality of the inverter.

In these pages, a discussion and explanation about different decisions taken in designing is given. After selecting the topology of the inverter and its components, it comes to compute the different elements of the circuit, as the DC bus capacitor, the output inductance, or the filter. Then, a description of the losses in the different semiconductors is made and employing the software LTSpice they are also estimated.

A key aspect in the design is the value of the switching frequency. The possibilities available, as well as a discussion about PWM modulation are also reflected.

The chapter ends with the circuit protections. Not only a description, but also a selection of the components necessary for the adequate operation of the device is made.

3.1 Context (features of the problem)

Regarding frequency, the desired output sine would be of **50 Hz**, standard value in most part of the world.

Also, it is necessary to define a **switching frequency** for the semiconductors. Given that in this work an Arduino will provide the PWM signal, the frequency can be modified as desired. The best results can be achieved on a range from **5 to 15 kHz**, fact which will be lately explained.

Therefore, a resume of the **main features** for the inverter is:

- Maximum power: 65 – 75 Watts.
- Input voltage: **220 V (AC).**
- Output voltage: **220 V (AC).**
- Sine frequency: **50 Hz.**
- Recommended switching frequency: **5-15 kHz.**

3.2 Performance criteria.

A very important aspect in every design is the determination of the performance criteria, that is to say, which aspects are considered the most important regarding the results obtained.

3.1.1 Efficiency

As it was mentioned in the previous chapter, energy conversion should ensure the optimal utilisation. This requirement can be determined by measuring the efficiency of the system. **Efficiency** (η) is defined as the relation between output and input power, usually measured in percentage. Good efficiency ratios are above 80 or 90%.

$$\eta = \frac{P_o}{P_{in}} \times 100\%$$

Directly related to efficiency are **power losses**. In semiconductors, losses appear not only while switching but also when conducting due to their internal structure. A deeper insight into losses will be given further in these pages.

A 100% successful conversion is not possible in reality. Although the efficiency rates are usually high, there is always a part of power that dissipates in the form of **heat**. Unluckily, this heat cannot be tapped. Also, it has negative effects on the device, especially regarding performance, as temperature increases and components may not work properly for this reason.

3.1.2 Quality of the waveform

Not only the amount of energy obtained after conversion is important, but also its **quality**. On a pure sine inverter, the waveform should be as clear and pure as possible. There are several factors affecting this waveform, being the performance of the circuitry components an example of that, but mainly the distortion of the sine is due to **harmonics**.

Every periodical signal can be decomposed into a sum of sinusoidal functions, by means of Fourier series expansion. Therefore, the mathematical expression for a periodic voltage is:

$$v(t) = V_{DC} + \sum_{n=1}^{\infty} \sqrt{2}\, V_n \sin(n\omega t + \theta\theta_n)$$

As desired component, the **fundamental component** is the one that oscillates at 50 Hz. It is the first term of the series, and the rest of components are regarded as undesired for several reasons.

V_{DC} is the **DC component** of the voltage. It is the medium value of the signal and normally, this project included, is wished to be zero. In order to achieve this, different techniques can be applied. In the current design, this part of the voltage is removed as a result of the modulation used in the H-Bridge.

Harmonics are components whose frequency is a multiple of 50 Hz. They distort the waveform and their value decreases as the series index increases. Other problems related to harmonics are noise, possible damage in electronic circuits or overcharge of capacitances.

Not all the undesired components have frequencies multiple of 50 Hz. **Inter-harmonics** are named sub-harmonics when they appear below 50 Hz, but can also be found as a broadband spectrum.

The most common way of measuring the quality of waveform is the **Total Harmonic Distortion (THD).** It is defined as the ratio between the sum of power of all harmonic components and the power of the fundamental frequency.

Type equation here.

A good voltage THD should be ensured in order to achieve good performance. For low voltage levels, THD should be around 8%, according to UNE-EN 50160 (official standard in Spain that defines features in voltage provided to consumers by electricity distribution grids). However, it is mostly recommended to deal with no more than 5% harmonic voltage distortion factor. The largest single harmonic should not be above **3%** of the fundamental voltage [11]. A high THD can result in malfunction of the equipment.

3.1.3 Reactive Power.

Regarding power, it is necessary to make a first distinction between DC and AC circuits.

On a **DC voltage circuit**, it is only necessary to take into account the power that is transformed into work or heat, called **Active Power** (P). It can be computed as the product of instantaneous voltage (V) and current (I), and its units are Watts. As they are always in phase, power can be calculated as:

$$P = V \cdot I$$

However, dealing with **AC voltage circuits**, there are more circumstances to be considered. In this kind of circuits, apart from Active Power, there is another one which deals with the formation of electric and magnetic fields in the components of the circuit. This power is not really consumed, but fluctuates between those components and the energy source. Its name is **Reactive Power**, and it is represented with letter Q. Its units are volt-ampere reactive (Var).

The way of relating those two powers is **Apparent Power** (S), which is the vector sum of both Active and Reactive Power. It is measured in Volt-Amperes (VA).

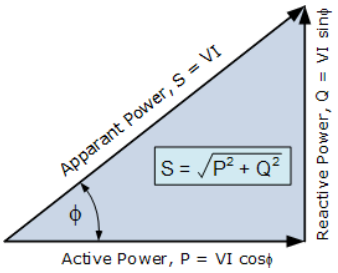


Figure 3.1: Relation between Active, Reactive and Apparent Power [17]

The existence of Reactive Power in an AC circuit depends on the load. If it is purely **resistive**, both current and voltage reverse polarity at the same time, and therefore their product is only positive or zero. They are said to be in phase, and the energy flow goes only in one direction. As a result, only active power is transmitted between the source and the load.

On the other hand, in case the load is **reactive**, voltage and current are out of phase. On each cycle, their product can be positive or negative, and consequently, the energy flow oscillates between the source and the load. This means, an amount of energy is not transmitted to the load (the reactive power). Depending on the gap between current and load, the quantity of energy transmitted varies. This magnitude can be measured by the **power factor (PF)**, which relates active and apparent power.

$$PF = \frac{active\ popper\ (P)}{apparent\ popper\ (S)} \qquad (1)$$

Equation (1) can also be expressed in terms of the **phase angle** ϑ between powers. As it is reflected in Figure 3.1, active and apparent power can be computed taking into account this angle.

$$P = V \,.\, I \,.\, \cos \mathrm{P} \qquad\qquad S = V \,.\, I$$

Therefore, equation 1 results in

$$PF = \frac{active\ power\ (P)}{apparent\ power\ (S)} = \frac{V \,.\, I \,.\, \cos \mathrm{P}}{V \,.\, I} = \cos \mathrm{P}$$

The maximum value for the power factor is 1, that is to say all the energy involved between the source and the load is transmitted. A bad power factor results in wastage of the exchange.

In order to transmit the same active power, in a circuit with low PF, higher currents are needed, resulting in greater losses, wires and equipment required.

The aim of this project is to design a device which could produce as high FP as possible. Sometimes it is not likely to get a good ratio of active power only with normal operation of the device. For this reason, **reactive power is often compensated**. In some cases, an external device or component, such as a capacitance, is added in order to contribute with reactive power to the consumption of the load. This solution is not very precise, and therefore, for optimal compensation, a closed loop control of current is usually employed. Controlling the diphase between current and voltage in the output it is possible to get FP closed to 1.

3.3 Inverter topology

Once the main features of the problem are established, the first issue to consider on the designing is the topology of the inverter. Normally, inverters deal with high voltages and a boost step is required. DC/DC before inversion or AC/AC after it are usual solutions added to the inversion step.

However, the solution adopted in this project will be that of only the **DC/AC conversion,** as the desired voltage levels can be achieved. In case a higher voltage is required, an external boost can be added.

Regarding the bridge topology, a **Full H-Bridge** will be used. This configuration requires two branches and 4 interrupters. As explained in the previous chapter, each elementary switching cell contains a transistor and a diode.

The topology selected (Figure 3.2) implies benefits in regard to Half- Bridge as lower voltages in the semiconductors and lower input voltage for the same output. Switching losses are higher in a Half-Bridge, as semiconductors deal with 2Vdc.

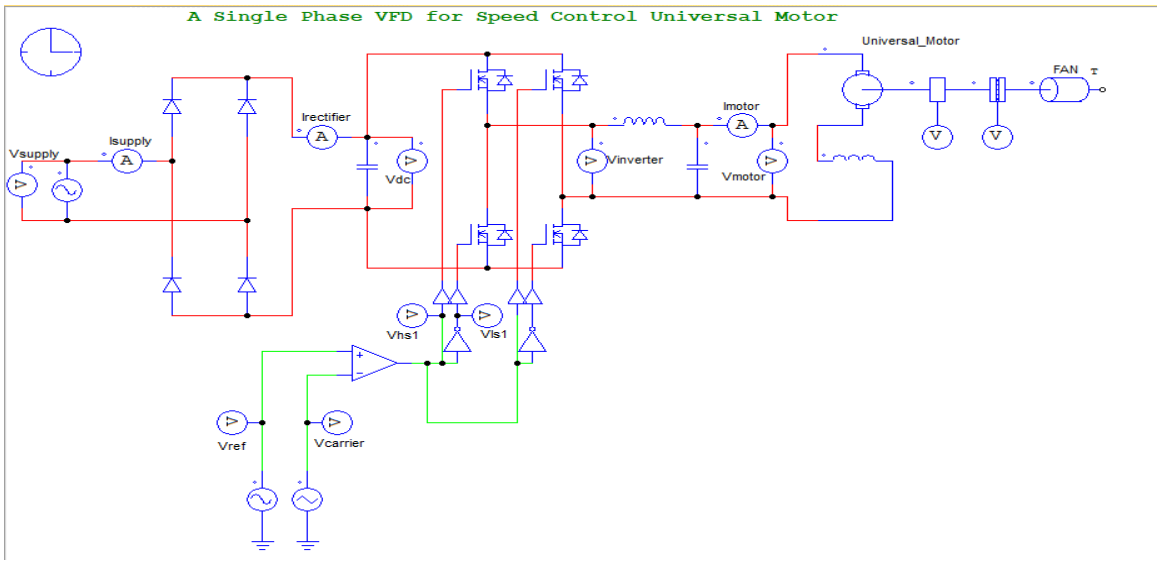


Figure 3.2: Full H-Bridge schematic with PSIM software.

3.4 PWM Modulation. Switching frequency

A key decision in the design of an inverter is the value of the switching frequency. In the following pages, an analysis of the options will be developed. Also it is necessary to select the modulation to apply in the bridge, as the configuration and the calculation of elements vary.

3.4.1 PWM Modulation

In the previous chapter, an insight into different options for PWM modulation was given. The most common ones are **unipolar** and **bipolar** modulation. In this section, a comparison between them will be made and the most suitable option for this project will be selected.

As a starting point for comparison, in both cases **the output voltage** is measured (Figure 3.3), obtaining different values and frequencies. Establishing the same switching frequency for both modulations, in bipolar modulation the **output frequency** remains the same, while in unipolar modulation it **doubles** the initial value. This allows reducing the size of passive components as inductances and capacitors but leads to higher losses. Regarding the **output values**, on bipolar modulation, they oscillate between two values, Vin and –Vin (being Vin the DC input voltage), whereas that on unipolar the output are three levelled (Vin, 0, -Vin). The higher the number of levels for modulation, the better is the waveform.

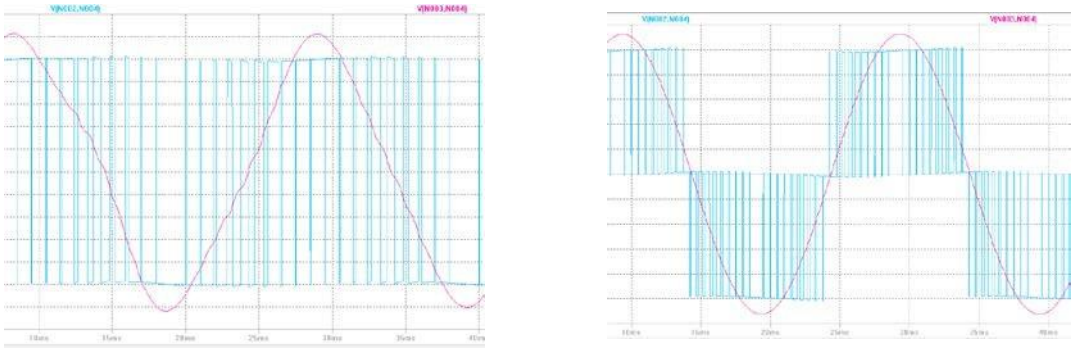


Figure 3.3: Output waveform with bipolar (left) and unipolar (right) modulation.

Regarding **harmonics**, some important points should be stressed. In **bipolar** modulation the output voltage harmonics appear at the frequency of commutation and have twice the amplitude of the branch voltage harmonics. However, in **unipolar** modulation, their frequency is twice the switching frequency and their amplitude is the same as in the branch voltage harmonics. The harmonics of the odd families do not appear in the output, as in every branch they are in phase. As the higher harmonics (first family) are odd and the frequency of the rest is higher than in bipolar, they are easier to filter. This has a direct impact on the **filtering inductance**, resulting it four times lower in unipolar than in bipolar. Another way of reducing harmonics is elevating

the switching frequency, and therefore easing their filtering. However, with this solution the losses can become really high.

Taking into account the criteria described at the beginning of this chapter, the **efficiency** achieved with each modulation should also be analysed. Setting the **same output frequency**, on bipolar modulation the switching frequency is two times higher than in unipolar. For this reason, the switching losses are higher. An insight into Figure 3.4 lets see the different efficiencies between unipolar and bipolar modulation regarding power and with a switching frequency of 20 kHz. The maximum rates are achieved with a unipolar modulated H-Bridge, whereas the Half- Bridge configuration gets the worst results.

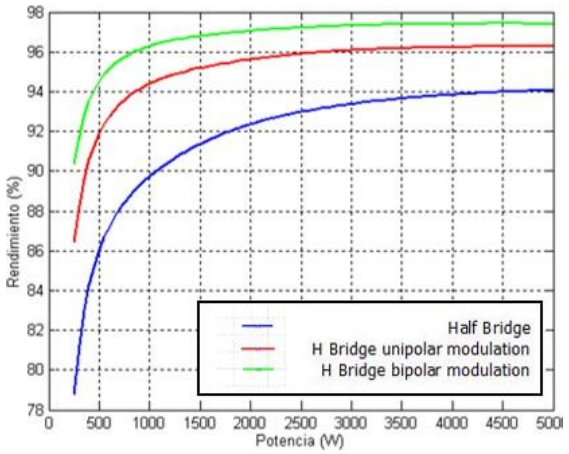


Figure 3.4: Efficiency for f=20 kHz vs. Power [1]

> In applications such as photovoltaic systems, it is necessary to consider the differences regarding **common mode voltages**, but for the current design they will not be a decisive fact for decision.

After the discussion developed it is decided to implement **unipolar modulation**. **Efficiency** is the key feature for this decision. Also the ease to filter harmonics and the possibility to have twice the switching frequency in the output are pros that influence on the selection. As the circuit is made for educational purposes, the **size** of the components is wished to be as small as possible, and the output inductance can be reduced with this modulation.

3.4.2 Switching frequency.

One of the most important aspects in the design of an inverter is the selection of the switching frequency, as **losses** and the **quality of the waveform** are directly related to its value. As in this case the generation of the PWM is digital, the switching frequency will be set by the **microcontroller**. A complete discussion of the possibilities will be developed in Chapter 4. Also different options will be tested on the real circuit, being the results collected in Chapter 5.

3.5 Selection of semiconductors

Taking into account the information given in Chapter 2 about semiconductors, in this section a further comparison between some of them will be given, in order to explain the design decision.

The first semiconductor commonly used in power electronics was **BJT**. Its simple structure and capacity to amplify current are two of its main strong points. However, in order to be turned on, high base current are needed. Also, its turn-off is relatively slow and it is highly susceptible to thermal runaway, due to its negative temperature coefficient.

When **MOSFETs** where developed, they became a good substitute for BJTs. As they are controlled by voltage, the problem with high base current is solved. Also, their temperature coefficient is positive, preventing thermal runaway. They are quick switching devices, and on their turn-off there is almost any current tail. This effect is a consequence of the remaining charges on the PN junction, and affects negatively the turning off of the switcher, delaying it and augmenting losses as a result. Structurally, MOSFETs have a body-drain diode, which can be used as free- wheeling diode for inductive loads. On the other hand, their switching losses are quite noticeable and they cannot deal with very high voltages.

IGBTs combine features from BJTs and MOSFETs. They are controlled by voltage but the output switching and conduction characteristics are those of BJTs. The turn-off is similar to the MOSFET one, but with a larger current tail. This fact makes their shutdown time and losses higher. Other disadvantages are the negative temperature coefficient and the lack of body-drain diodes. However, some solutions can be adopted in order to attenuate those drawbacks, as adding ultrafast recovery diode co-packed to faster the turn off. Furthermore, actual process technology and device structure have been improved, resulting in better switching characteristics [7].

The selection between MOSFET and IGBT depends on the **application**. Solutions are not unique and the features and requirements given in each application determine the choice. However, as a rough view, in Table 3.1, it can be seen a resume of some remarkable features and values.

Feature	MOSFET	IGBT
Voltage	< 250 V	>1000V
Frequency	> 100 kHz	< 20 kHz
Power	< 3 kW	> 3 kW
Efficiency	Light load	Full load
dV/dt	Limited	High

Table 3.1: Resume of features and selection [12]

Design decision

In this current project, **voltage** is the key feature for deciding. As the requirements for the application are very low, the saturation voltage of the IGBTs is a handicap. Glancing over different catalogues and vendors, it is hard to get an IGBT with $V_{CE(SAT)}$ lower than 1.4 volts. As normally two IGBTs conduct at the same time, this results in nearly 3 volts lost between input and output. This is circa a fifth of the DC voltage source so it cannot be taken as adequate. Considering MOSFETs, their behaviour at conducting can be modelled as a resistor with a value in the range of milliohms. Therefore, the difference between input and output is not so remarkable. About **frequency**, although MOSFET are commonly selected in high frequency applications, they can also deal with low values.

At the time of simulating, it is possible to compare the output waveform with ideal switchers, MOSFET and IGBTs in the following circuit:

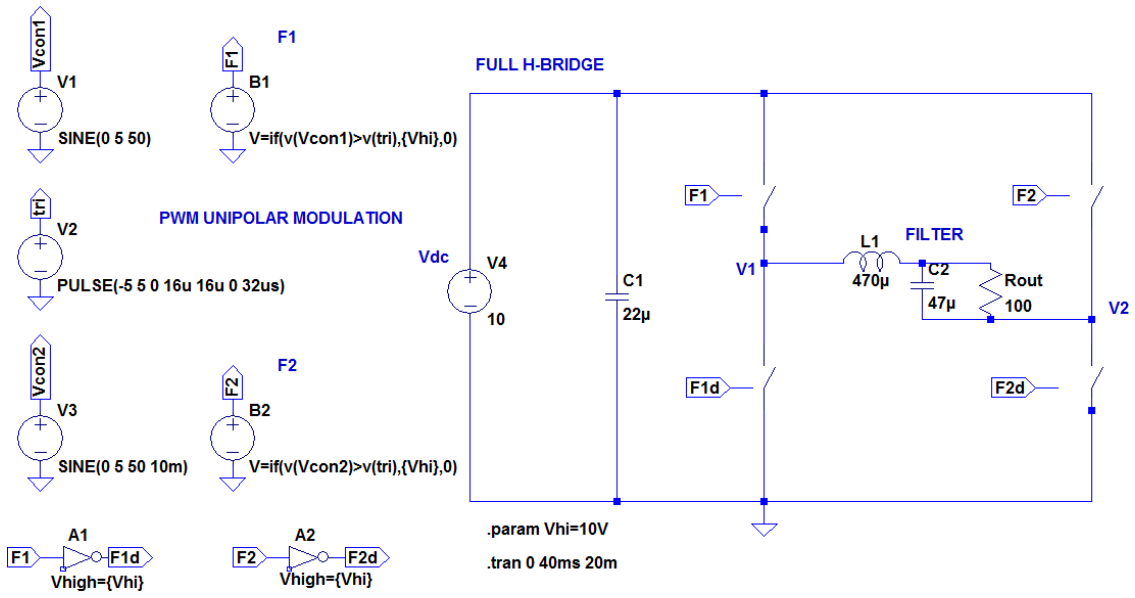


Figure 3.5: Schematic of Full H-Bridge applied for comparison between semiconductors.

For all the cases the input DC voltage is 10V and the switching frequency is set in **10 kHz.** Figure 3.6 shows the different results obtained. The vertical axis division is 2 Volts. The blue waveform corresponds to the output voltage without filtering, whereas the pink one is the voltage in the load.

As it can be seen, while IGBT-bridge remains under 6 volts, MOSFET-bridge is closer to 10 volts. Also, the clarity of the switched waveform is notable in case of MOSFETs, and the unipolar modulation can be well distinguished. On the other hand, with IGBTs the waveform is not so clean and the peaks are more irregular.

1

2

3

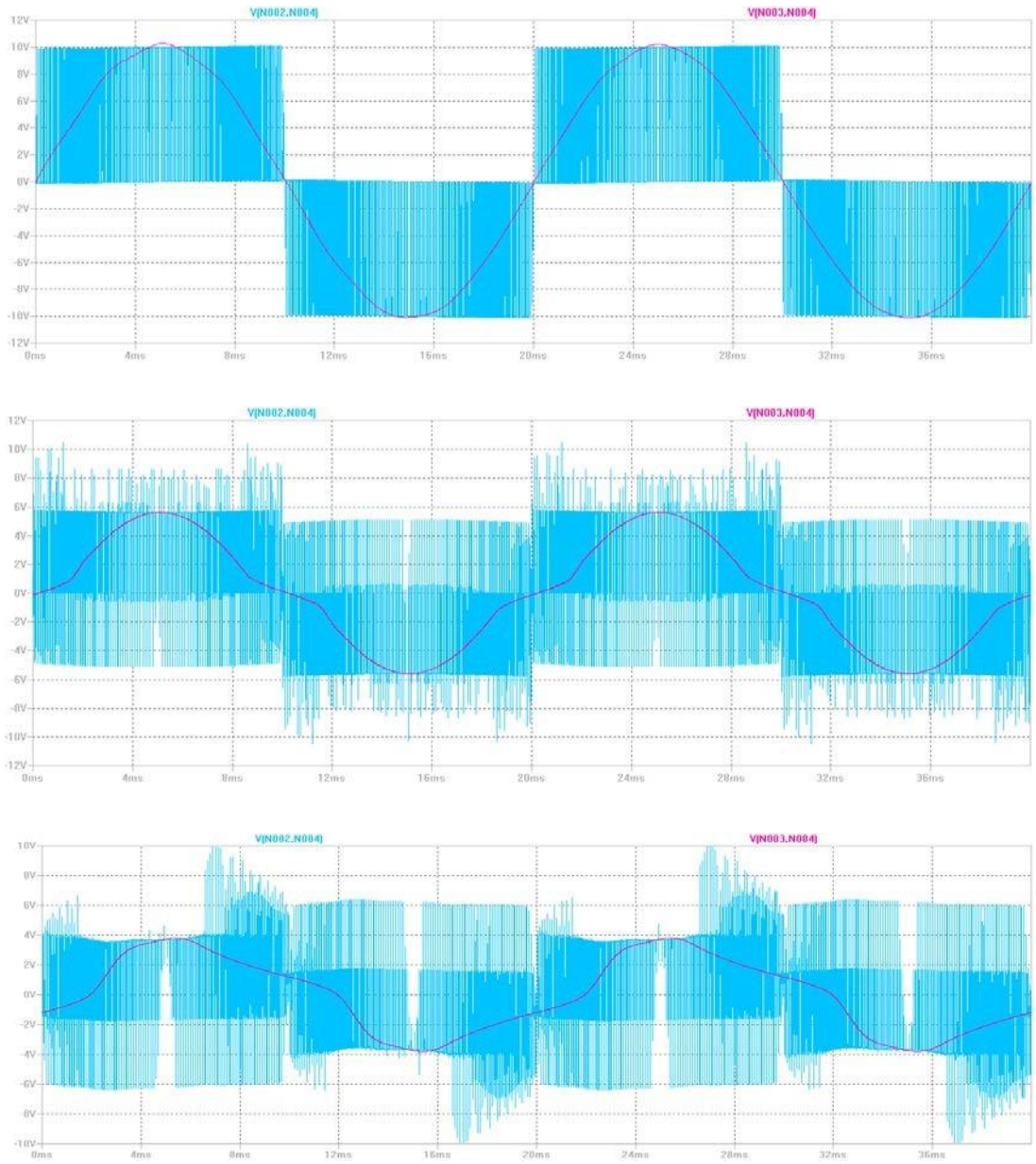


Figure 3.6: Output voltage waveform on ideal switchers (1), MOSFET (2) and IGBT (3).

After the previous discussion, it is finally decided to select **MOSFET** as semiconductors. This way, in order to achieve a three segment switcher, a **MOSFET and a diode in antiparallel** will be chosen.

Regarding MOSFETs configuration, it is possible to find N-Channel and P-Channel semiconductors. As explained before, in power electronics the most widespread type are N- Channel MOSFETs, which have P doped silicon as substrate. When they are turned on, the conducting channel is formed by the movement of electrons. The consequence of employing this type of FETs is that a bootstrap circuit is required to drive the high-side MOSFETs' gates of the bridge.

After consulting different options and vendors available, the MOSFET selected is **IRF840**, from Infineon, specially designed for low voltage applications. Its complete features are collected on its datasheet [17]. The package selected is **TO-220AB**, in order to adapt easily to the breadboard and the PCB.

Figure 3.7: IRF840 with TO-220AB package

3.6 Dead – times on the semiconductors

Ideally, commutations in the semiconductors are instantaneous. That is to say, when the on order is given to the MOSFET, it turns on immediately. This behaviour allows the two semiconductors on each branch to be complementary in performance, avoiding their overlap.

However, when it comes to reality, the MOSFET turns off a bit later than receiving the order. This time is called **turn-off delay time (td_{off})**. The same case occurs at the time of turning on, resulting in a **turn-on delay time on (td_{on}).** This behaviour is shown in Figure 3.9 of this chapter, being the delay times from t_0 to t_1. Considering the branch as a whole, it would not be a problem in case the td_{off} and the td_{on} of the semiconductors would be equal. Unluckily, in nearly all the semiconductors the turn-off delay time is higher as the turn-on delay time.

As a consequence of this, both switchers conduct during a short period of time, which results in a transient **short-circuit**. Voltage drops and there is a peak of current tending to infinite. Depending on the delay, the value of the current could not reach very high values, as normally the overlapping lasts nano or microseconds.

In order to avoid the short circuits, a fixed delay is introduced on the signal of the semiconductor that will be turned-on. This delay is called **dead time**, and during it the voltage of the branch depends on the current sign. As a result, there is an error in the voltage.

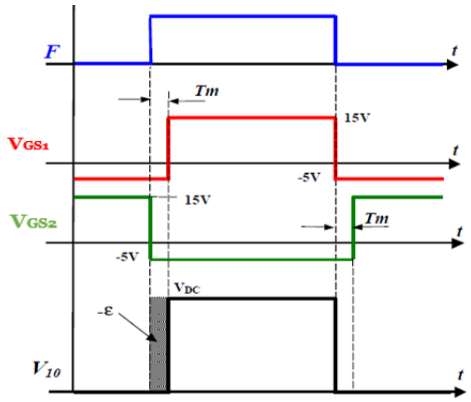


Figure 3.8: Error due to dead time in semiconductors [1]

Also, the **driver** itself helps to handle with this problem. As shown in Figure 3.9, an internal delay is added on the structure of the IR2110 in order to avoid the simultaneous conduction of the switchers.

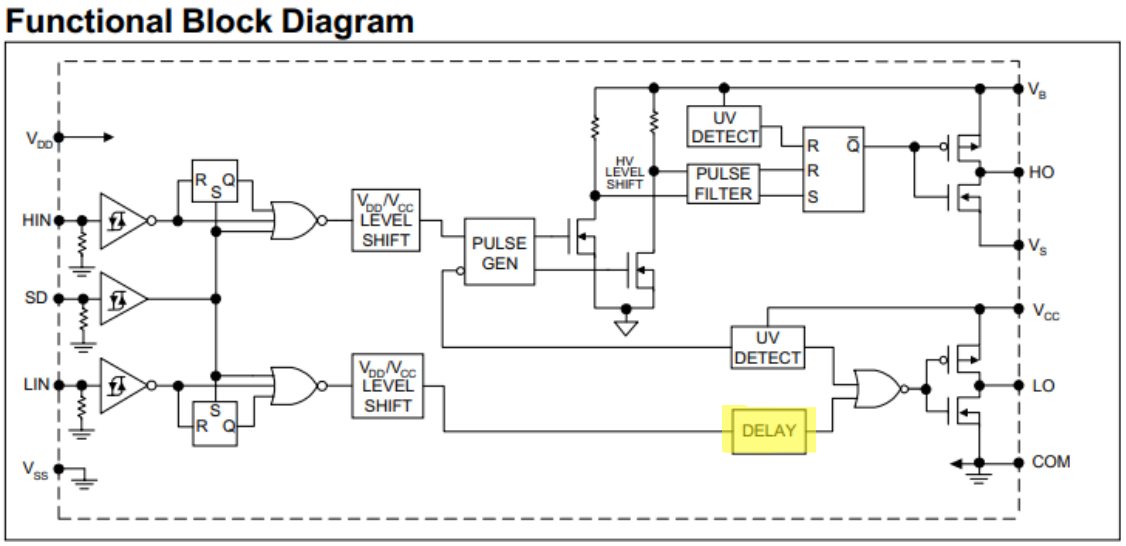


Figure 3.9: Block diagram of the IR2112 [18]

3.7 Losses in semiconductors

An important issue to consider in the design of the inverter are losses in semiconductors. During their performance, semiconductors cause losses not only when switching, but also while conducting. Therefore, an analysis of their internal structure and behaviour should be made in order to compute losses. After this first analysis, in this section an estimation of losses is made. Those computations are required in order to discuss the necessity of a sink.

3.7.1 Analysis

In this current project, the semiconductors selected are MOSFETs and diodes. During their performance, they produce losses that become heat and result in a waste of energy converted. A complete analysis of losses include conducting losses, turn on and turn off losses.

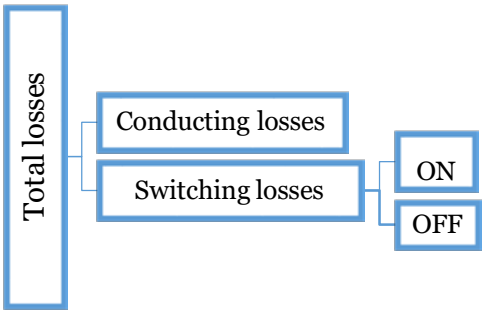


Figure 3.10: Diode conducting model

- **Losses in the MOSFET**

When **conducting**, a MOSFET can be modelled as a resistor with value $R_{DS(ON)}$. This resistor normally is of a very low value, in the range of milliohms.

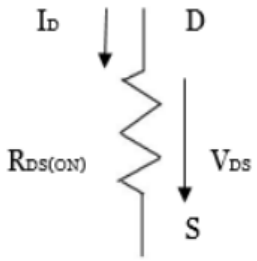


Figure 3.10: Diode conducting model

The **instantaneous power** can be computed as:

$$p\,(t) = R_{DS(ON)}\, {i_D}^2(t)$$

Being i_D the current on the drain. In case i_D is constant, the calculations become easier. This way, the **average power** is:

$$P = \frac{1}{T_{ON}} \int_0^{T_{ON(MOSFET)}} R_{DS(ON)}\, {I_D}^2\, dt = R_{DS(ON)}\, {I_D}^2 \frac{T_{ON(MOSFET)}}{T_{switch}}$$

This expression reflects the computation of the average power only when the MOSFET conducts. For this reason, the duty cycle appears on it. Its value depends mostly on the drain current I_D, as it appears squared.

Regarding **switching losses**, the turning-on and off of the MOSFET should be taken into account, as in both cases voltages and currents appear at the same time, resulting into losses. In figure 3.11, the model of the MOSFET and the variations of current and voltage are shown.

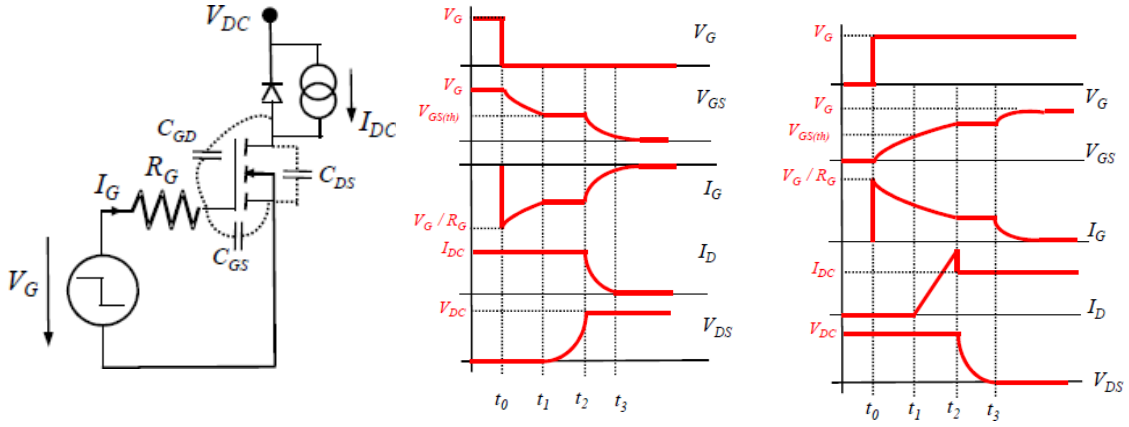
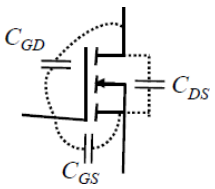


Figure 3.11: Model and waveforms of turning on (left) and off of the MOSFET

Switching losses appear in both cases between t1 and t3. As the switching is not instantaneous, current and voltage deal together during those moments, resulting in losses.

In order to turn-on and off the MOSFET, the electrons of the different layers in which load circulates must be introduced and removed. This behavior can be modelled as **parasitic capacitances.** C_{iss} is the input capacitance, and models the introduction of electrons. C_{oss} is the output capacitance, and takes into account the removal of electrons. Finally, C_{rss} is the Miller capacitance, and reflects the Miller effect (the increase in the equivalent input capacitance of an inverting voltage amplifier as a result of the increase of the effect of capacitance between the input and output terminals). The lower Vds, the higher are these capacitances.



$$C_{iss} = C_{GS} + C_{GD}$$

$$C_{oss} = C_{DS} + C_{GD}$$

$$C_{rss} = C_{GD}$$

Figure 3.12: Capacitances on a MOSFET [1]

Figure 3.12 shows the schematic and composition of the capacitances that can be found on a MOSFET. At the time of computing the losses, the energy involved depends on the drain-source voltage (V_{DS}), the drain current (I_D), the control voltage (V_G), and the gate resistor (R_G).

- **Losses in the diode**

A diode can be modelled as a voltage source and a series resistor when conducting (Figure 3.13). Therefore, a similar procedure as in the MOSFET can be followed to compute the **conducting losses.**

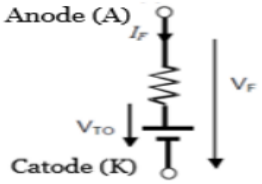


Figure 3.13: Diode conducting model [1]

The instantaneous power is:

$$p = V_{TO} I_F + r_T {I_F}^2$$

Taking Ic as constant, the **average power** is:

$$P = \frac{1}{T_{ON}} \int_0^{T_{ON(diode)}} V_F I_F \, dt = V_F(I_F) I_F \frac{T_{ON(diode)}}{T_{switch}}$$

At the time of computing the **switching losses**, as in the MOSFET, it is necessary to compute the energy lost during the turning-on and off, and multiply it by the switching frequency. However, on a diode, the energy lost during the **turning-on** can be neglected.

In the case of the **turning-off**, it is necessary to relate the value of the graph in the datasheet with the real voltage and current. The energy involved depends on the voltage anode-cathode (V_F), the current (I_F) and the instantaneous change of I_F with time dI_F/dt.

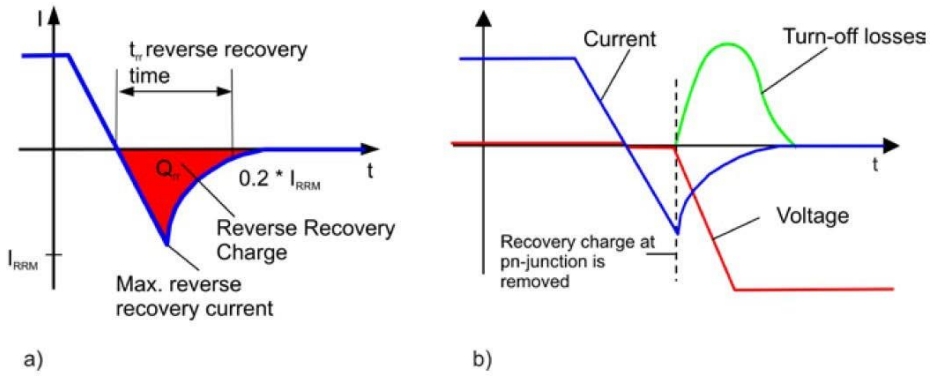


Figure 3.14: Turn-off behaviour (a) and current curve, voltage and switching losses (b) [5]

3.7.2 Calculation

The main difficulty of computing the losses on the inverter is determining the **current** on the semiconductors. As explained in the analysis section, the formulas for conducting losses become simpler taking current as constant. However, on an inverter the current is switched at the switching frequency. For this reason, a method for computing the losses is making the calculations on small periodes of time with different currents. Having those values, it is only necessary to sum them in all the period of time.

As figure 3.15 shows, the current in the branch is **sinusoidal**, with 50 Hz of frequency. The positive semicicle corresponds to the current in the MOSFET, while the diode deals with the negative semicycle. There are several spikes due to transient shortcircuits. The origin of those comes from the dead times on the semiconductors.

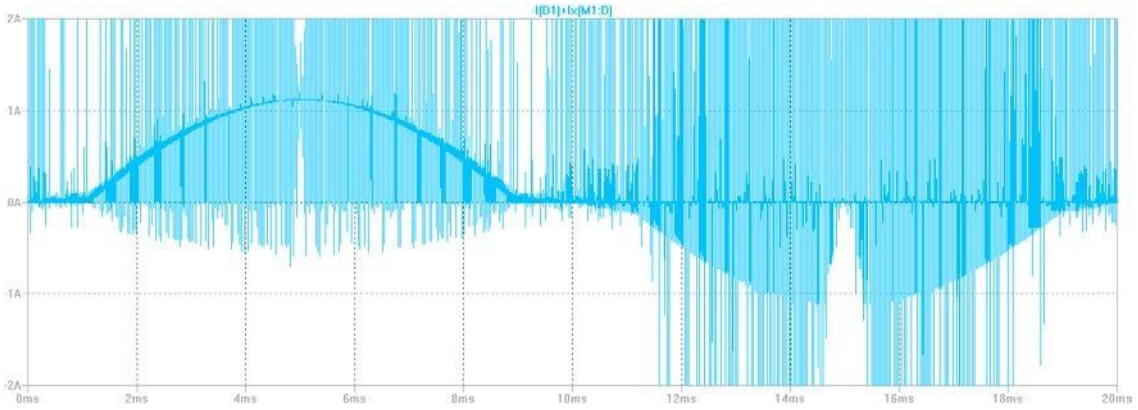


Figure 3.15: Current in a branch in one period (20ms)

The estimation of the losses can be made in several ways. The most accurate is to employ a computation software such as Matlab. An example of code can be found in Appendix 3 of [8].

In this case, it is decided to have a general idea by simulating with the **software LTSpice**. The simulation time is set in 20 ms, in order to have an average value of the losses in one period, and the switching frequency is **31250 Hz**. The main figures are reflected in Table 3.3.

Element		Losses	TOTAL
MOSFET	M1	5.678 W	17.763 W
	M2	3.163 W	
	M3	5.730 W	
	M4	3.191 W	
Diode	D1	167.760 µW	457.918 µW
	D2	62.787 µW	
	D3	167.580 µW	
	D4	62.791 µW	
			17.763 W

Table 3.3: Average losses on the semiconductors in one period

It is highly remarkable the difference between the MOSFETS and the diodes. Also, it can be appreciated that the high-side MOSFETS have nearly twice the losses of the low-side devices.

3.7.3 Power dissipation

As previously commented, it is impossible to obtain a perfect energy transmission between the source and the load. Some of the energy losses its heat capacity and cannot be used, being transformed into **low quality heat**. Not only is the reduction of efficiency a problem, but also the resulting increase of **temperature in the junction**.

The maximum operation temperature on the silicon junction of the MOSFET is **175 ºC** (T_{jjmax}) [17]. In case higher operating temperatures are achieved, the useful life is reduced. This feature, together with losses on the semiconductor (P_{lost}), the maximum ambient temperature (T_{ambmax}) and the total thermal resistor (R_{thjja}), limits the maximum working current on an inverter.

For the discussion in this section, the concept of **thermal resistor** should be clear. On a material, it is defined as its capacity to oppose to heat flow. It is measured in thermal degrees (Celsius or Fahrenheit e.g.) divided by Watts. On an inverter, the total thermal resistor can be divided into several parts, depending on the surfaces in contact.

Regarding thermal analysis, it is possible to model the different junctions and temperatures as an electric circuit. Thus, the power is equivalent to current, thermal resistors to electrical resistors and temperatures to voltages.

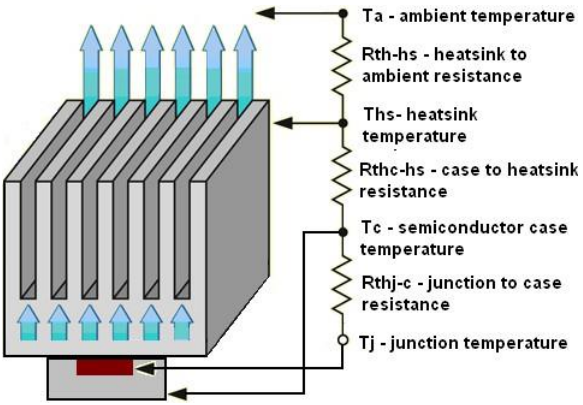


Figure 3.16: Schematic and electric circuit between silicon junction and ambient. [14]

$$T_j = T_a + R_{thja} P_{lost}$$

$$R_{thja} = R_{thjc} + R_{thch} + R_{thha}$$

Power losses can be estimated, and therefore are considered as data on this specific heat analysis. The aim in this section therefore is to discuss the necessity of a sink in order to dissipate heat and the determination of the thermal resistors.

The maximum power losses are

$$P_{lost} = \frac{T_{jjmax} - T_{amax}}{(R_{thjjc} + R_{thch} + R_{thha})}$$

Therefore, thermal **resistors should be minimized** in order to have greater losses.

For this purpose, some options can be considered. Normally, a **heat sink** is added, allowing better dissipation thanks to its specific surface. In case a sink is not allocated, the circuit is simpler, and the total resistor is only the sum of junction-case and case-ambient resistors.

$$R_{thja} = R_{thjc} + R_{thca}$$

For the actual design, and taking into account the estimations of Appendix A, it is decided to **place a sink attached to every MOSFET.**

3.8 Circuit elements selection

Once the features are established, it is necessary to determine the values for the components of the circuit. Not only is the selection of the semiconductors important. Inductances and capacitors help to damp ripples in voltage and current and therefore must be carefully chosen. In this section, a resume of the elements of the circuit is presented. The complete computations of their value are collected in Appendix A.

3.8.1 Capacitors

At the time of selecting the capacitors, it is first necessary to determine the **optimal value** depending on their role on the circuit. Also, the **type** of the capacitor should be carefully chosen according to the application, as it is desired to have the smallest size possible.

Apart from the **decoupling capacitors** and the **bootstrap components**, which will be further explained, it is important to take into account the **DC Bus capacitor**. The input voltage of the inverter comes from a DC source. However, even the most accurate source produces some noise that distorts the original waveform. Also, it should be considered that on the DC side of an inverter, it appears a pulsating current which frequency is twice the output frequency [1]. This results in a rippling voltage.

For those reasons, it is normal to include a capacitor on the DC bus of the inverter, in order to stabilize voltage. In this design, the element chosen is a **47 µF electrolytic** capacitor. The estimation of this value is collected in Appendix A.

3.8.2 Inductances

On an inverter, as the output voltage is switched, the current is not constant, and oscillates depending on the voltage sign. In order to decrease the ripple current and to attenuate harmonics, an inductance should be placed in the output.

As it is described in Appendix A, the value of the output inductance depends on the PWM modulation selected. In this case, for unipolar modulation and setting a 5% of rippling current in the output, the minimum value of inductance is **1mH.**

Once computed theoretically, the next step is to check by simulating the rippling current. On the MOSFET H-Bridge, the output current waveform on the inductance (on steady state and with $L_{OOUT} = 470\ \mu H$) is reflected in Figure 3.17.

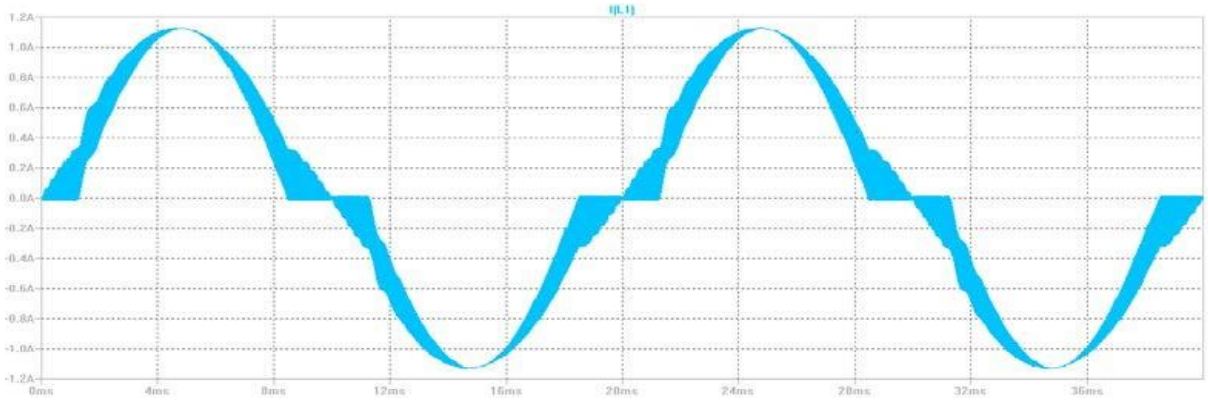


Figure 3.17: Waveform of inductance current with Lout=160 µH.

It can be seen in the figure, that the current ripples mostly on the intermediate values of the sine. It corresponds to the theoretical expectatios, as the maximum rippling value is acquired at a duty cycle of 50% ($m = \frac{1}{2}$), and if it is measured, it corresponds to values around 250 mA.

Depending on the load, the value of the output current can be very low, and therefore it is desired to have as low oscillation as possible. For this purpose, higher inductances can be placed.

For instance, in figure 3.18 an inductance of **470 µH** is employed. As a result, the oscillation of current is only 80 mA. The inductance behaves ideally as a current source, and helps to filter the oscillations. This value will be finally selected.

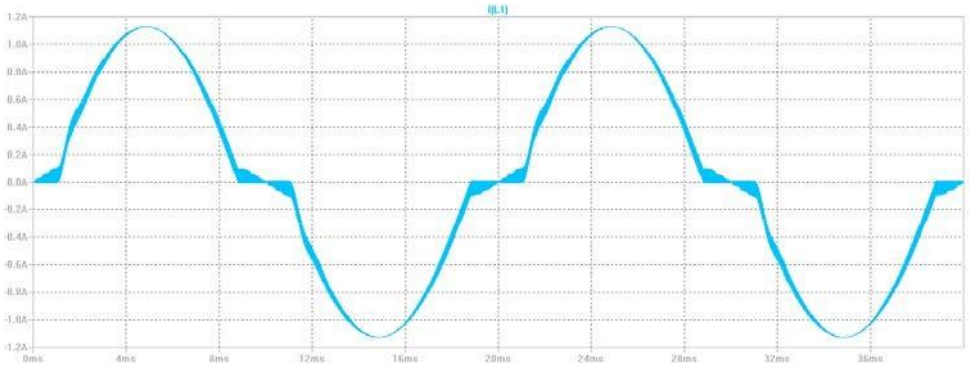


Figure 3.18: Waveform of inductance current with Lout=470 µH.

3.8.3 Filter

The output voltage between two branches (V_{12}) is a **square waveform**. This voltage cannot be applied directly to a load because it could damage it. Therefore, a filter is necessary between the bridge and the load. Not only because of the waveform, but also for **harmonics** is necessary to design and place a low pass filter.

As explained previously in Chapter 2, there are two main types of low pass filters: LC and RC. At the time of selection, it should be taken into account that on an inverter, an inductance is needed in order to filter the ripple current. This inductance can be also used for the filter. Therefore, the best option is an **LC low pass filter**. Moreover, by this choice no extra losses are added, as no resistors are included.

After determining the requisites for cutting frequency, in order not to disturb the normal performance of the device, some computations are made and collected in Appendix A. In conclusion, a low pass LC filter with a series inductance of **1mH** and a parallel capacitance of **220uF** is selected.

3.8.4 Output load

As explained before in this chapter, depending on the type of load (resistive, inductive or capacitive) the power factor varies.

In order to measure the output for simulation, a **resistor of 180 Ω** is placed in parallel with the filter capacitance. The lower this resistor, the quicker becomes the discharge of the capacitor. On the other hand, a higher resistor value would result in a better waveform. Taking into account losses, the value selected for the resistor allows to have good efficiency. In Chapter 5, a further explanation of the changes in the output voltage depending on the load value can be found. A resume of the components of the circuit is collected in Appendix C.

3.9 Driver

As explained in Chapter 2, drivers are usually employed in converters in order to adapt the connection function to the requirements of the semiconductors. Amplification, protection against low feeding voltage or galvanic isolations are some of the main functions of a driver.

Basically, the gate drive requirements of high-side devices can be summarized to three main points [19]:

- The voltage between gate and source must be from 10 to 15 Volts.
- The gate voltage must be controllable from the logic.
- The overall efficiency should not be affected by the power absorbed by the gate drive circuitry.

Feeding the MOSFET with the right value of voltage is crucial. Not only high values are dangerous for the semiconductor, but also **under voltages**. An example of this is the value of the **resistor** between drain and source in the MOSFET ($R_{DS(ON)}$). The semiconductor can be modelled as a resistor when conducting and therefore its value should be known. However, sometimes it is not easy to compute, as it depends on the value of V_{GS} (gate-source voltage). In the saturation region, the higher the value of V_{GS}, the lower is $R_{DS(OON)}$. The explanation for this involves the internal structure of the MOSFET and the electrons channel that appears when the device conducts. Lower values of $R_{DS(OON)}$ are advisable in order to obtain better efficiencies. Nevertheless, it should be constant to avoid instabilities, as it reflects the movement of electrons in the channel.

Figure 3.19 shows this variation of values for the selected MOSFET in the design (IRF60B217). Thus, it is recommendable to obtain a V_{GS} higher than 8 Volts. In this particular case, the range of resistance is milliohms, so the conduction losses are not excessively large.

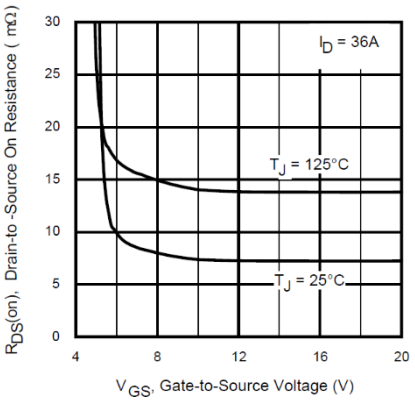


Figure 3.19: On – Resistance vs. Gate Voltage [17]

The connection function applied to the semiconductors, without including a driver, comes from the microcontroller. The PWM output of the **Arduino UNO** oscillates between **0 and 5 Volts**. From Figure 3.19, it can be seen that the resistor's value is not constant in that range. This means, in case of a small oscillation in the PWM output value, the resistance changes considerably.

To avoid this, a driver which provides at least 8 Volts is needed. The drain-to-source resistor is around 7 mΩ for those values. Furthermore, the input gate values in the MOSFET should be over the threshold value, otherwise its **saturation** is not achieved, and conducting losses are excessively high.

For these reasons, a driver is placed between the control and the semiconductors. The model selected is **IR2110**, by International Rectifier-Infineon Technologies. As explained on its datasheet [18], it is a high voltage, high speed MOSFET and IGBT driver with independent high and low side output channels. It is adapted to switch the high-side MOSFETs with a simple external bootstrap circuit. Also, propagation delays are matched and its internal structure assures a minimum delay between internal signals in order to reduce the dead times on semiconductors.

Figure 3.20 shows the typical connection for the device, set from its datasheet.

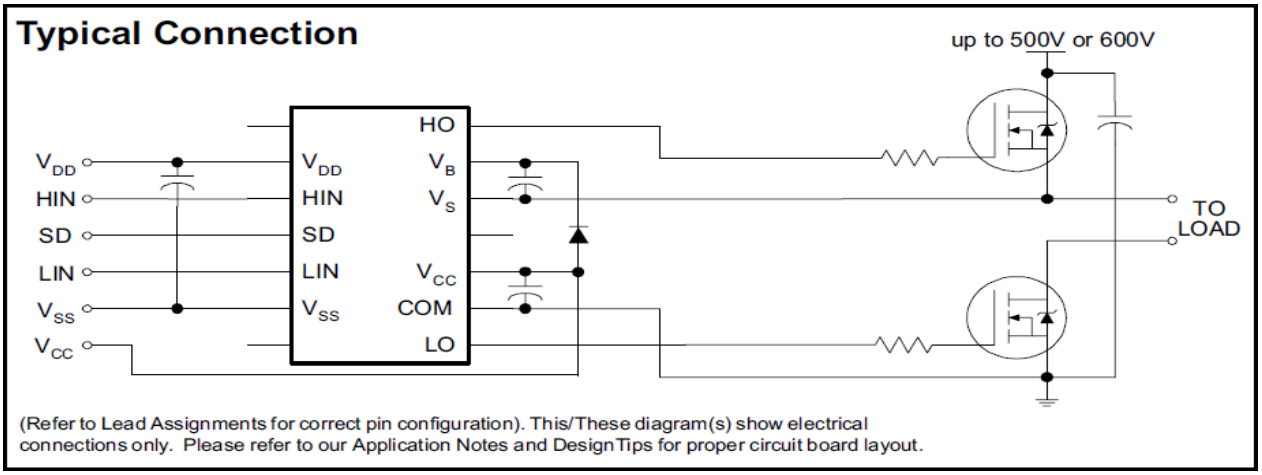


Figure 3.20: Typical connection of IR2110 [18]

In order to assure a safe operation, it is necessary to define the **input voltages**, as well as the **external elements** required. Strictly, only a **bootstrap** diode and a capacitor between V_B and Vs must be placed with the aim of feeding the high-side gate drive circuitry of the driver. However, it is recommended to place **decoupling capacitors** on the Vcc and V_{DD} supplies to compensate inductances in the supply lines [19].

3.9.1 Input voltages

The IR2110 driver requires two different levels of feeding voltage. On the one hand, V_{DD} is related to the input logic part, and must be adapted to its level. On the other hand, V_{CC} deals with the output voltage, and therefore should be chosen according to the desired levels.

SD is a shutdown input that allows disabling the driver. In this case it will be set into zero, but another example of connection is connecting it by a capacitor to V_{DD} (Figure 30 from the Application Note AN 978 [19]). For its part, V_B is a floating input referred to Vs and corresponds to the triggering of the high-side MOSFETs.

Following the recommendations of the vendor, the values set for the input voltages are collected in Table 3.3. The only value that cannot be defined is Vs, as it is referred to the middle point of the branch of the bridge.

Table 3.3: Description and values selected for the input voltages.

Symbol	Value (V)	Description
V_{DD}	5	Logic supply
HIN	[0-5]	Logic input for high-side gate driver output HO
SD	0	Logic input for shutdown
LIN	[0-5]	Logic input for low-side gate driver output LO
Vss	0	Logic circuit ground
VB	15	High side floating supply voltage
Vs	-	High side floating supply offset voltage. Undefined value.
Vcc	15	Low side fixed supply voltage
COM	0	Low side ground

By powering the driver with **15 Volts,** the output levels are assured to be high enough to feed the MOSFET

appropriately. The input return voltages will be set to **zero**, as it is necessary to assure that their values are below the threshold voltage of the MOSFETs in order to turn them off. Regarding the logic input, it is recommended to adapt it to the top value of HIN and LIN. Therefore, it will be fed with **5 Volts**.

In order to achieve this, it is decided to place a **voltage regulator**. Thus, it is only necessary to feed externally the logic circuit with 15V, as the regulator adapts this value to the 5V also required by the driver. The model selected is an **LM7805C** [22], widespread linear voltage regulator available in **TO220 package**, and with a low power consumption. Simply adding two external capacitors, it is possible to obtain 5V of output voltage.

According to its datasheet, the current rating of the logic power supply of the driver is around 350μA for the Vcc input and 20 μA for the V_{DD} input, values low enough to avoid excessive heating. The complete scheme is collected in Figure 3.21.

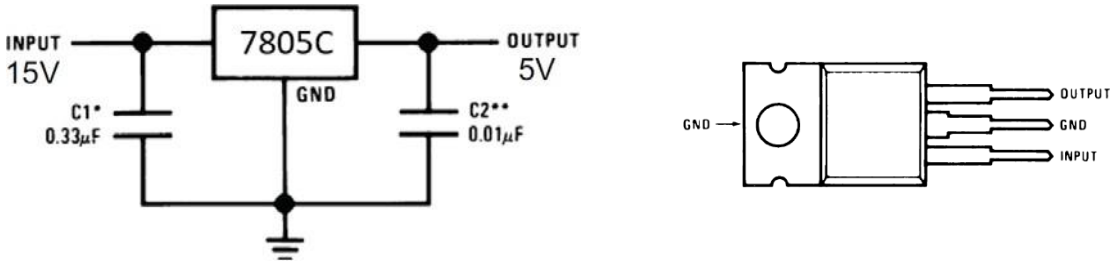


Figure 3.21: Resume schematic of LM7805C.

3.9.2 External elements.

From the **Application Note AN-978** [19], only a bootstrap diode and a capacitor between V_B and V_s are required for a standard PWM application with the IR2110. Also some decoupling capacitors can be placed to compensate the inductance of the supply lines. The complete scheme is shown in Figure 3.22.

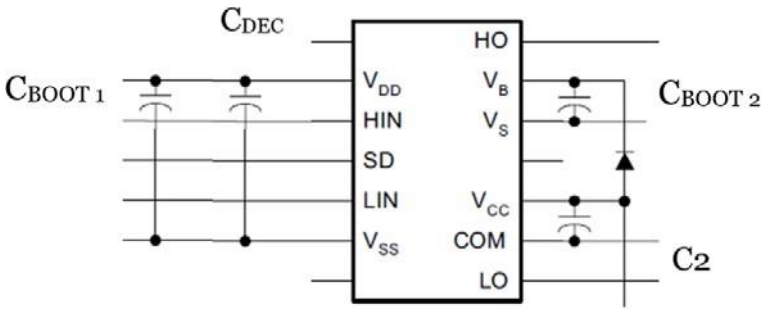


Figure 3.22: Complete scheme of the driver and external elements

- **Bootstrap capacitor 1 ($C_{BOOT\,1}$)**

In the scheme above, two bootstrap capacitors can be found. In the case of $C_{BOOT\,1}$, the aim of this component is to give the current peak necessary to turn on the MOSFET. The energy required is stored when the semiconductor is turned-off. Its value should be appropriately computed, as an excessive capacitance involves high charging times. This fact could lead to the limitation of the switching frequency. On the other hand, an insufficient value can lead to voltage drops on the driver's power. As a general idea for its value, the same procedure as in [9] will be followed.

The input supply for the driver should be as constant as possible. Therefore, it can be established a maximum ripple on the capacitor's voltage, being 5% a normal value. In order to have this rippling, the charge of the capacitor (Q_{BOOT}) should be at least 20 times higher than the charge required to turn on the MOSFET (Qg) [9]. As explained before, in case the capacitance is too low, the voltage in the driver's power can drop.

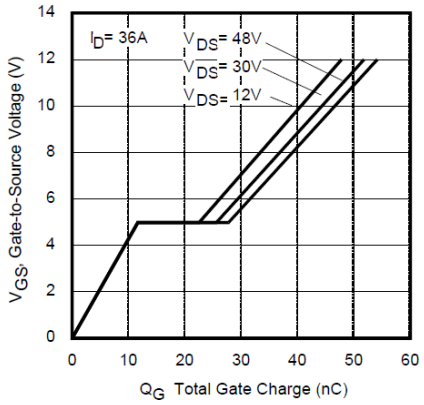


Figure 3.23: Typical Gate Charge vs. Gate-to-Source Voltage on IRF60b217 [17]

The graph that relates the typical charge gate vs. Gate-to- Source voltage can be found in the MOSFET's datasheet (Figure 3.23). As the drain-to-source voltage is closer to 12

V and V_{GS} will be 10V as maximum, the total charge required to turn-on the MOSFET is **40 nC**.

Once this value is defined, the minimum capacity of the bootstrap capacitor can be computed as:

$$QQ_{BOOOOT} = C_{BOOOOT} * V_{BOOOOT} = QQ_{gg} * 20$$

$$C_{BOOOOT} = \frac{QQg * 20}{V_{BOOOOT}} = \frac{40 * 10^{-9} * 20}{10 - 0} = 8888\, nF$$

Nevertheless, some additional recommendation given in [19] are also followed. An example given is to increase the bootstrap capacitor value to **470 nF** in order to improve local decoupling and reduce overcharging in case the value of Vs is not high enough. Thus, this value will be selected.

- **Decoupling capacitor (C_{DEC})**

As an extra protection, the placement of a decoupling capacitor is also considered. In case the driver is fed by a switching power supply, some current spikes might be present, and the driver can be negatively affected. In order to avoid this it is possible to place another capacitor. However, the bootstrap capacitor is enough to deal also with the decoupling.

- **Bootstrap diode and capacitor (C_{BOOST_2})**

The internal structure of the driver allows the adjustment of the voltage levels for the high-side and the low-side MOSFETs. In the case of the low-side MOSFETS, as they are connected to ground it is only necessary to adapt their gate voltage level to values that assure their saturation. However, in order to achieve the saturation of the high-side MOSFETs, the voltage supplied in V_B must be floating with respect to V_S.

As recommended in the AN-978, a bootstrap capacitor can be placed between **V_B and V_S**, as well as a diode between **Vcc and V_B**. Thus, when the low-side MOSFET is conducting, the capacitor is charged through the diode with Vcc. On the other hand, the diode avoids the discharge of the capacitor when the MOSFET stops conducting [28].

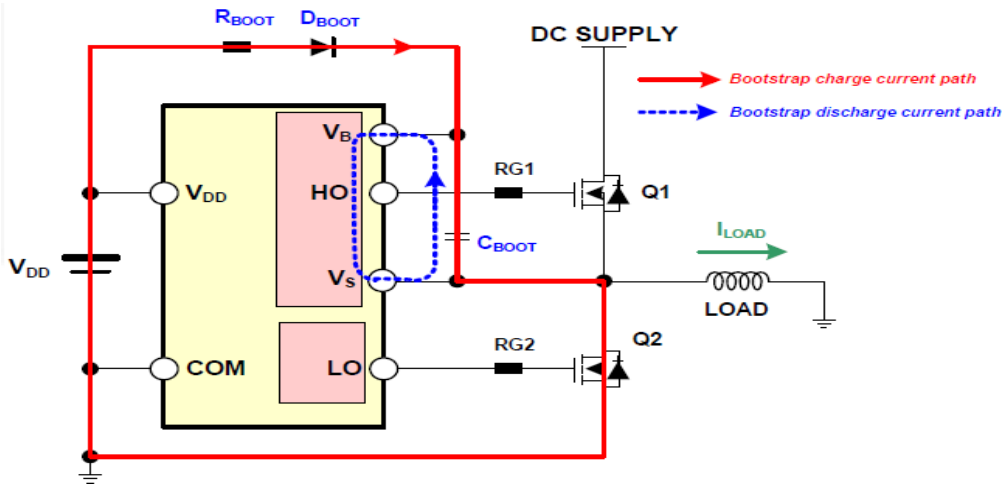


Figure 3.24: Current path on a bootstrap circuit

Figure 3.24 shows the current path for bootstrap charge (red) and discharge (blue) on a similar driver. For the IR2110, V_{DD} in the Figure corresponds to V_{CC}.

The value of the capacity should be enough to assure a stable voltage for the turning-on of the high-side MOSFET. The exact formula for the computation of the minimum value can be found in the Application Note 978 [19]. Following the vendor's advice [19], a value of **470 nF** will be selected. The diode chosen is a **1N4001**, common model used in low voltage circuits.

- **Other elements**

A detailed example of the typical implementation of the driver with an H-Bridge is shown in Figure 3.24. Also, it is recommended to select a value for C2 around ten times higher than C_{BOOST}, as this capacitor supports both the low-side output buffer and the bootstrap recharge. Thus, the value selected is **2.2 µF.**

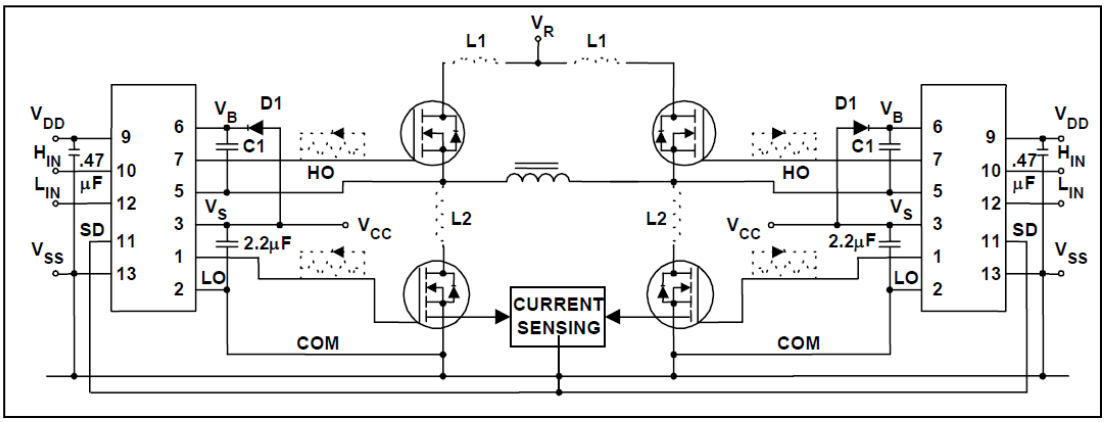


Figure 3.24: Typical implementation of an H-Bridge [19]

3.10 Circuit protections

A very important issue to consider in the design of a circuit are possible problems in operation. The elements of the circuit can be exposed to dangerous operational currents or voltages that may result in their deterioration or even their breakdown. Therefore, some precautions must be taken in order to assure a safe operation of the H-Bridge. In this section, the most important risks will be analyzed. As a solution to them, some proposals will be made.

3.10.1 Overvoltage protection

The PN junction is the base of the semiconductors. If an excessive voltage is applied to it, it can result in its breakdown and therefore, the whole device can be destroyed. On an inverter, one of the most common reasons for overvoltage are the commutations of the semiconductors. When the current is interrupted in an inductive load, the voltage boots. In real circuits, there are parasitic inductances due to the conductors or the connections between elements. When the semiconductors switch, the current changes instantaneously and as a result there are overvoltages. To avoid them a simple solution is to place the elements as close as possible [1].

The **breakdown voltage** varies depending on the specific MOSFET. According to the datasheet of the IRF60B217, the maximum drain-to-source voltage is 60V. As the input source is 10 volts, an overvoltage seems unlikely during normal operation. In the case of **gate-to-source voltage,** its value should not exceed **±20V**. In order to assure those values, a solution commonly taken in this case is to place a **Zener diode** between the gate and the source. This type of diode conducts when a positive voltage is applied between the anode and the cathode. However, unlike other types of diodes, when they are reversely polarized and the 'Zener Voltage' is reached, they act as voltage regulators, as they maintain this value as constant. Thus, they don't allow the MOSFET get into avalanche because of overvoltages. For the purpose of assuring both positive and negative limits, normally two Zener diodes are put joined by their cathodes. In the current design it is decided to place only one **15V Zener diode.** The resulting scheme is shown in Figure 3.25.

3.10.2 Overcurrent protection

One of the most significant sources of danger are excessive currents on the elements. For instance, in case a short-circuit happens, the current will shoot up, only limited by the parasitic resistances in the circuit. However, the values of current achieved could even destruct the device. For this reason, it is common to measure the current in several points of the circuit, in order to disconnect it if the values become dangerous.

- **MOSFET overcurrent protection**

In the case of the actual design, the continuous drain current can be up to **60 amperes**, whereas the device can bear pulses of 225 A. It must be taken into account that the current limits vary with the temperature of the junction. The higher the junction temperature, the lower are the maximum currents allowed in order not to destroy the internal junctions.

As explained previously, in the gate of the MOSFET there is a parasitic capacitance due to its internal structure. Therefore, the switching of the device can be modelled as the charge and discharge of this capacitance. It is desirable to minimise this switching times, as the device deals

with significant voltages and currents, resulting in high losses. However, it is necessary to limit the changes of current with time (di/dt), as they may induce voltage spiking that could damage the MOSFET, especially their gate insulations.

For this reason, it is usual to place a resistor between the driver and the gate, in order to limit the current. The value of this resistor can be determined from the maximum values for output voltage and current in the driver. This device has an output current limit, setting a top value of 2.5 amperes. The maximum voltage that it can provide depends on the maximum input voltage, and it must be below 25 volts. Thus, the gate resistor can be computed as

$$R_G = \frac{V_{out\ driver\ (\max)}}{I_{out\ driver\ (\max)}} = \frac{25}{2{,}5} = 188\ \Omega$$

The **gate resistor** modifies the gate current, affecting the switching of the device. The higher the resistor, the longer the switching takes, and therefore the higher are the losses. However, a minimum value for the resistor is needed in order to limit the current. The MOSFET includes an internal resistor of 2 Ω, but adding an external **resistor** of **10 Ω** poses an extra margin.

In the case of **ideal switchers**, no current flows while they are opened. However, the semiconductor has a very low leakage current in the magnitude of nA. Even though the value is really low, it could charge the gate capacitance of the MOSFET, making it turn on and off and even resulting in its destruction. To avoid this, a **resistor between the gate and the source** can be placed. Its value should be high enough not to affect the normal switching but below a limit determined by the leakage current. A detailed explanation of its computation is given in Appendix
A. The standard value chosen for it is **47 kΩ**.

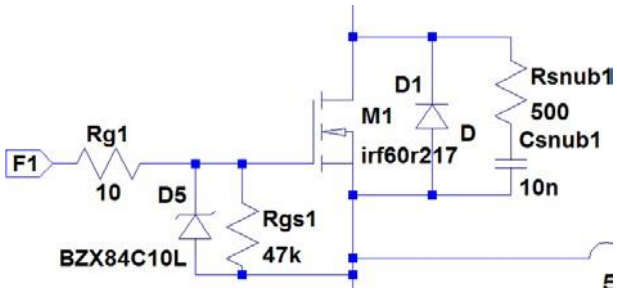
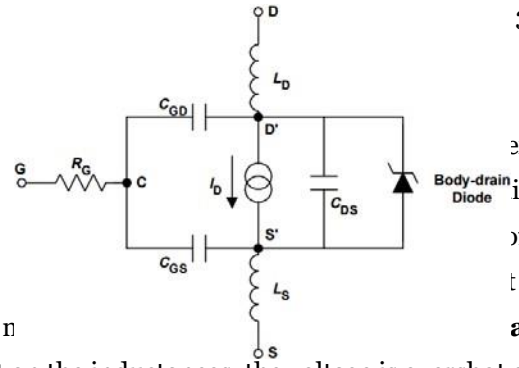


Figure 3.25: Complete scheme of MOSFETs protection

- **Switching protection: snubber circuit.**

As its name indicates, a snubber element is placed to suppress a transient on electrical circuits. In the case of a MOSFET, there are several elements that affect its switching performance, as it can be seen in Figure 3.26.



3.26: Equivalent circuit of a MOSFET showing components with greatest effect on switching [29]

but has n example, when the high-side MOSFET turns on, the body-iode of the low-side transistor (which was conducting before) off. During this process it draws a peak reverse recovery t and snaps off [20]. This phenomenon lasts a short time **asitic inductances.** As a consequence of these **reverse current** on the inductances, the voltage is overshot and may result in the turn on of the low side MOSFET again or in avalanche breakdown.

Also the **noise** resulting from commutations can get coupled to the sensitive electronic components in the load, even resulting in malfunctions. For those reasons, it is necessary to follow some recommendations at the time of designing [1], as placing the elements as **close** as possible or locating bypass capacitors next to leads of switching components. Also, the best way to reduce switching noise is to minimise the parasitic inductances [20].

The placement of a **snubber circuit** is a solution that helps to deal with parasitic inductances reduction. An RC snubber is a common combination for protection and it will also be designed and applied in this project. The **capacitor** is placed in order to absorb the inductive energy stored in the load at the moment of switching, whereas the **resistor** helps the damping and makes sure that the capacitance does not discharge instantly on the next commutation.

Following the instructions given in the Application Note AN100-1 form Alpha-Omega [20], some simple computations can be made in order to have an estimation of the optimal values for the circuit. The complete procedure is described in Appendix A. As a resume of it, a **capacitor of 10 nF and a resistor of 500 Ω** will be selected.

The parasitic inductance is distributed in all the PCB and includes the package inductances [20]. They should be minimised to reduce overshoots and ringing. A good layout with the elements as closed as possible is the best way to reduce parasitic inductances. Also, selecting transistors with low inductance packages or which contain integrated Schottky body diodes help to deal with this problem.

- **Load overcurrent protection**

At the time of designing, it is important to define the maximum values for the output. For security reasons, the output current is not desired to be over 5 amperes, as this value can be harmful for humans. From the design features, the output voltage is set to 15 peak volts. Thus, the minimum resistor that can be placed in the output is

$$R \geq \frac{V_{OOUT(\max)}}{I_{LOOAD(\max)}} = \frac{15}{5} = 33\ \Omega$$

For extra protection, a **fuse** can be placed in the output.

Chapter 5

Simulation and results

Chapter 6 Conclusion

In this report, a complete description of the procedure followed for designing a single-phase inverter has been developed. As a resume, the following points have been described:

- **Theoretical approach** to the single-phase inverter. Definition, applications and topologies, as well as an explanation of its elements.

- Definition of the **design criteria** and **selection of the specific components**. Discussion of the best options regarding modulation, switching frequency and topology.

- Justification of the **elements placed** in the design and their value.

- Analysis of the **microcontroller**. Possibilities regarding PWM generation.

- **Testing** of the circuit on a protoboard. Discussion of the results obtained and comparison with simulating expectations.

6.1 Objectives achieved

The main purpose of obtaining a pure sinusoidal waveform with digital implementation is met. The PWM generation is achieved with a simple C code, as a convenient substitute of analog circuitry. Thus, in case some changes are desired to be made regarding signal or PWM frequency, it is only necessary to change the corresponding values of the registers.

Also, as the circuit is built using discrete components instead of an integrated circuit, it is easier to check the performance of the elements that constitute the bridge.

However, the levels of voltage achieved in the output are a little lower than the ones expected from simulation. One possible reason for this is the performance of the real elements. Voltage drops and power consumption are some effects that cannot be easily predicted and that have high influence on the results obtained.

Regarding the C code, to have the optimal output in the Arduino, the PWM frequency is limited on a range from 35 to 62.25 kHz. This fact is due to the memory available in the microcontroller selected.

6.2 Further developments

Some recommendations and guidelines are also collected with regard to future improvements of the circuit. The lack of time is the main reason of their absence in the current work.

To determine the quality of the inverter, the best option would be applying the spectrum analyser or the Picoscope to have an idea of the distortion in the waveform. Also, to analyse the variation of power factor, different inductive or capacitive loads could be placed as output. 7

6.2.1 Efficiency

The efficiency tested on the circuit is around **11%**. However, it would be necessary to check the values of the current more carefully to have a better idea of the exact figure. Taking this estimation, the first idea that comes into mind to increase this value. As explained in previous pages, switching frequency on the semiconductors is directly related to this fact, and therefore it should be kept on values around 30-40 kHz on the current design. Also there are some considerations that can be taken into account to increase efficiency, as selecting another power supply or trying with other PWM modulations.

- **PWM modulation**

Although unipolar has been the most widespread solution regarding PWM modulation, the current techniques in power electronics are mostly focused on **modified unipolar modulation** as an option to increase efficiency (e.g. [13]). In this case, the high-side transistors switch at high frequency (in the order of kilohertz) and the low-side at grid frequency, depending on the sign of the control signal. Whereas the switching losses dominate the high-side transistors, they are almost insignificant in the low-side devices. As a whole, the efficiency achieved is similar or even better than in unipolar modulation.

Thus, as an idea of further guideline, the digital implementation of this modulation can be also considered. Due to the lack of analog circuitry related to the PWM generation, fortunately only the code needs to be adapted.

Also, it is possible to select different models of transistors for the high-side and low-side switchers. Thereby, the MOSFETs are optimized for their correspondent switching frequency and have lower losses.

6.2.2 Microcontroller

For the current project the microcontroller selected is Arduino UNO. As explained before, the optimal output signal of the board with the current C code is obtained in a range of PWM frequencies from 35 kHz to 62.5 kHz. As the top values of the dutycycle and the length of the sine array are related to the PWM frequency, the compiler warned of memory limitations for the lowest values of frequency in this range.

In case the resolution is desired to be improved, the output obtained in the Arduino is not the optimal. Thus, it would be necessary to consider other options of microcontrollers to achieve lower PWM frequency values.

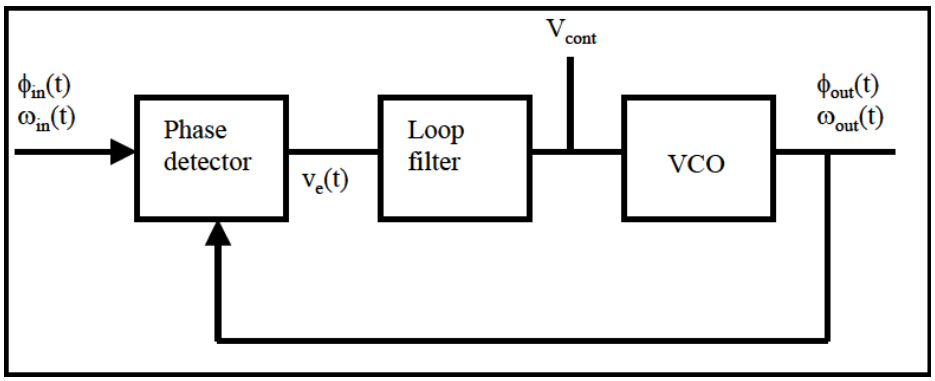
Also, with regard to a future control implemented, it is possible to select a more powerful option, as Arduino Due or Nano.

6.2.3 Control

Despite the implementation of a control system was considered at first, it is left to further work due to limitation in time.

Depending on the application of the circuit, the control applied varies. In this case, the option is to make it a grid connected inverter. Thus, a **phase loop** is considered as the option to implement.

PLL (Phase – Locked Loops) are control systems that generate an output signal whose phase is related to the phase of an input signal. Their main blocks are the phase detector, a low pass filter and a Voltage Controlled Oscillator (VCO).



Normally this system is developed with analog circuitry. However, as the PWM has already been generated digitally, it is only necessary to modify the code in order to add the control.

Some issues should be taken into account, as how to implement the **phase detection** and specially the **voltage oscillator**. The phase difference measured between the reference and the input has to be related to the value of the **dutycycle**, and therefore included on the Interrupt Service Routine of the current code.

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Appendix A: Calculations

On the following pages, a further explanation of some of the computations made to determine the elements of the circuit is developed. In some cases the origin of the formula is referenced to the source applied, but in the case of the output inductance, the formula is deduced.

A.1 Bus DC capacitor

Placed after the voltage source, its aim is to damp the voltage ripple resulting from a pulsating current that appears on the DC side of the inverter. The frequency of this current is twice the output frequency. In [1] the value of the peak to peak ripple voltage is determined to be:

$$\Delta V_{DCpp} = \frac{V_{AC}\, I_{AC}}{C\ \omega\ V_{DC}}$$

From this expression, the value of the DC capacitor can be computed as:

$$C \geq \frac{P_{nom}}{\Delta V_{DC} \,.\, \omega \,.\, V_{DC}}$$

Where

- Pnom is the nominal power, measured in Watts.
- ΔV_{DC} is the maximum ripple voltage desired in the capacitor.
- ω is the output frequency of the inverter.
- V_{DC} is the voltage in the DC side.

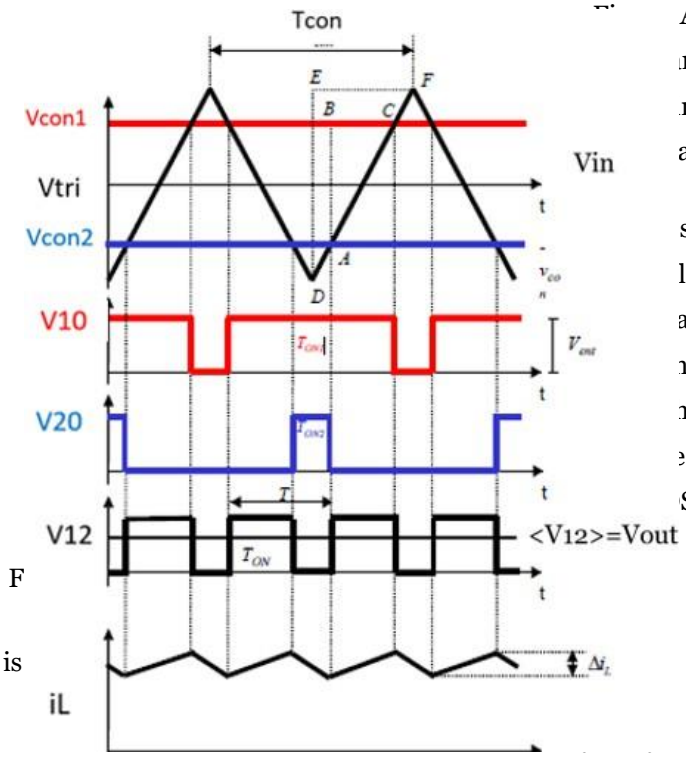
The maximum ripple voltage is desired to be 10%. The input DC voltage is 15 volts and the desired frequency is 50 Hz. Regarding power, the inverter would be desired to deal with around 25-30W. For security reasons, the nominal power of the inverter will be taken as 30 W. Taking all of this into account, the minimum capacitance that can be used in the circuit is:

$$C \geq \frac{P_{nom}}{\Delta V_{DC} \,.\, \omega \,.\, V_{DC}} = \frac{30}{0{,}1 \,.\, 15 \,.\, 2\pi 50 \,.\, 15} = 44.2222\ mF$$

It may be shocking the relatively high value of the capacitance. However, it is necessary to take into account that the values for input voltage and output frequency and very low. Also, this value is indicative and will be the highest achieved, as the power figure is set as limit. For this reason, a capacitance of **22µF** is enough for the design.

A.2 Output inductance

The determination of the value for the output inductance depends on the PWM modulation selected. As unipolar modulation is chosen in the current project, the formulas will be deducted for this specific case. Although PWM is generated digitally, the procedure followed to determine the inductance will be the same as in analogical implementation.



F A.1 shows the main waveforms of analogical voltage is r PWM modulation. The output voltage (V12) ned by the difference between the voltages in anches (V10 and V20).

sume of the explanation in section 2.8.2, the lar voltage (Vtri) defines the switching period and for each branch the correspondent voltages id V20) are obtained with comparators that ne control voltage (Vcon) with Vtri. The outputs e comparators are the connection functions of SFETs.

As it can be seen graphically in Figure A.1, the period of V12 (T) is half the switching period (Tcon). This output period must not be misled with the 50Hz output sine, as it corresponds to the waveform before the filter. To clarify the procedure followed, a basic schematic of an H-Bridge is shown in Figure A.2.

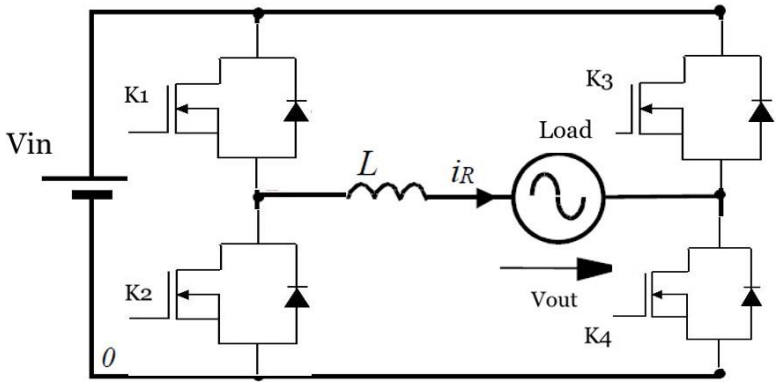


Figure A.2: H-Bridge schematic The voltage on

an inductance can be computed as:

$$V_L = L\,\frac{di_L}{dt}$$

During Ton (semiconductors K1 and K4 conducting on figure A.2), this voltage is

$$V_L = V_{in} - V_{out} \rightarrow (V_{in} - V_{out})\,dt = L\,di_L$$

As the sine output frequency is much lower than the switching frequency, the output voltage can be considered as constant for computations:

$$\int_0^{T_{OON}} di_L = \frac{1}{L}\int_0^{T_{OON}} (V_{in} - V_{out})\,dt = \frac{(V_{in}-V_{out})\,T_{OON}}{L} \qquad (1)$$

From the graph in A.1, it can also be deduced the relationship between PWM generation voltages and the duty cycle.

$$\frac{B-C}{T} = \frac{T_{OON}}{D-E} = \frac{A-B}{2V_{pt}} = \frac{2V_{con}}{E-F} = m$$

m is defined as the modulation index, and relates the control voltage and the triangular wave on the PWM.

Considering this, the average output voltage can be expressed employing the modulating as follows:

$$< V_{12} >= V_{12f} = \frac{T_{on}}{T} V_{in} = m\,.\,V_{in}$$

Also, the output voltage (Vout) can be approximated to the fundamental component of V12 (< V_{12} >, the one at 50 Hz). Applying this to expression (1), it can be seen that ripple depends on the modulation index.

$$V_{out} =< V_{12} >= V_{12f}$$

$$\Delta i_L = \frac{(V_{in} - V_{out})\, T_{OON}}{L} = \frac{(V_{in} - m\, V_{in})\, m\, T}{L} = \frac{V_{in}\,(1-m)\, m}{2\, L\, F_{sppitch}}$$

In order to include the switching frequency (F_{switch}) in the formula, it is necessary to multiply by 2, as the output frequency is twice the switching frequency.

To establish the maximum rippling current (Δi_{Lmax}) the function must be maximized.

$$\frac{\partial \Delta i_L}{\partial m} = 0 \rightarrow m = \frac{1}{2} \rightarrow \Delta_{Lmax} = \frac{V_{in}}{8\, L\, F_{sppitch}}$$

The value of the maximum rippling current desired should be defined in each case. After that, the minimum inductance that assures this value can be determined as:

$$L \geq \frac{V_{in}}{8\, \Delta i_{Lmax}\, F_{sssitch}} \qquad (2)$$

In the actual design, the value of the current in the inductance can be computed taking as data power and voltage, and assuming current and voltage are in phase ($\cos \varphi = 1$).

$$P = V.I\,.\cos\varphi \rightarrow I = \frac{P}{V} \qquad (3)$$

To have an estimation, the power will be set into 35 W and the output voltage is 10.6 effective volts. From (3) an output alternating current of 3 A effective as top value can be computed. A maximum rippling of 5% is desired.

Substituting variables in expression (2):

- Input voltage, Vin= 15 V.
- Switching frequency, F_{switch}= 31250 Hz
- $\Delta i_{Lmax} = 5\%\ i_L = 0.167\ A$

$$L \geq \frac{V_{in}}{8\, \Delta i_{Lmax}\, F_{sppitch}} = \frac{15}{8\,.\,0{,}167\,.\,31250} = 336688\ uH$$

As the frequency can vary on the design and the current value is not very high, in order to have lower oscillations in the current an inductance of **470µF** will be selected.

A.3 Filter

In order to design the LC filter, it is necessary to determine the **cut-off frequency** (fc) above which frequencies are attenuated.

$$wc = \frac{1}{\sqrt{LC}}\left(\frac{rad}{s}\right) \rightarrow fc = \frac{1}{2\pi\sqrt{LC}}\,(Hz)$$

Having chosen unipolar modulation, the output frequency is twice the switching frequency, which is 31.25 kHz. Thus, the **output frequency** will be 62.50 kHz. As the inductance is the same employed to smooth the output current, its value is already fixed on **470 µH.**

The cut-off frequency also depends on the value of the capacitor of the filter. This way, one of the variables (cut frequency or capacitor) must be fixed in order to obtain the other. As the values of the capacitors are standard, the procedure chosen will be that of selecting a capacitor which assures a satisfactory output waveform. This way, on a rough range between 50 and 500µF, it will be chosen a capacitance of **47µF**. Thereby, the cut-off frequency will be

$$fc = \frac{1}{2\pi\sqrt{470\,.\,10^{-6}.\,47.\,10^{-6}}} = 1881188,8833\ Hz$$

This value is high enough not to filter the output voltage at 50 Hz but much lower than the switching frequency. Therefore only the frequencies desired are obtained.

In conclusion, a low pass **LC filter** with a series inductance of **470 µH** and a parallel capacitance of **47 µF** is selected.

A.4 Gate to source resistor

The aim of the gate to source resistor is to discharge the gate capacitance C_{GS} in case there are parasitic charges due to leakage currents. A simple procedure can be followed in order to determine its maximum value.

The voltage in a capacitance can be computed as

$$V_c = \frac{1}{C}\int i_c(t)dt$$

When the IRF60B217 is turned off, the gate-to-source leakage current is 100 nA (from its datasheet).

The minimum gate voltage is set in 2.1 volts. As the gate capacitance (C_{GS}) is not given as data, the reverse transfer capacitance (C_{rss}) is substracted from the input capacitance (C_{oss}).

$C_{rss} = C_{GD} = 140\ pF$ ⟶ $C_{GS} = C_{iss} - C_{rss} = 2090\ pF$

$C_{iss} = C_{GD} + C_{GS} = 2230\ pF$

Therefore, the time necessary for charging the gate capacitance by the leakage current is:

$$t_{min} = \frac{V_c . C_{GS}}{I_{GS}} = \frac{2{,}1 \,.\, 2090 \,.\, 10^{-12}}{100 \,.\, 10^{-9}} = 4.3890\ ms$$

$\tau_{chargge}$ can be defined as the time needed in order the gate capacitance to achieve the 63,2 % of the total charge.

$$\tau_{chargge} = 0{,}632 * \ 4{,}389.10^{-3} = 2.7738\ ms$$

In an RC circuit, the time constant τ can be computed as $\tau = RC$. The time constant of discharge must be lower than the parasitic charge, in order to avoid it and to protect the MOSFETs. Thus, the maximum value that R_{GS} can have is

$$R_{GS} < \frac{\tau_{charge}}{C_{GS}} = \frac{2{,}7738 \,.\, 10^{-3}}{2090 \,.\, 10^{-12}} = 1, \mathbf{332211}\ M\Omega$$

The value selected for the resistor will be a standard of **47 kΩ.**

A.5 Snubber circuit

As explained in the Application Note AN100-1 form Alpha-Omega [20], in order to determine the values of the snubber resistor and capacitor, it is necessary to have a previous estimation of the parasitic inductances. These are undesirable effects in the circuit, and their sources are the traces between input capacitor and the switching devices. In practical circuits, they cannot be eliminated.

The optimum value of the snubber resistor must equal the characteristic impedance of the LC circuit [20].

The output capacitor of the low-side MOSFET (Coss) is the main source of parasitic capacitances that may ring with these inductances. For the IRF60B217 this value corresponds to 215 pF with a drain-to-source voltage of 25 volts. This value can vary with lower supply voltages, but having a glimpse into Fig. 7 of the datasheet, for $V_{DS} = 10\ V$ can also be taken as valid.

To estimate the value of the parasitic inductances, as a practical method it is possible to measure the frequency in the ringing waveform. Figure A.3 reflects the results obtained for the gate-to- source voltage. As it can be seen, the voltage oscillates during two periods in a range of 4 volts. Measuring the time with the cursors, it is possible to determine the period of one pulse (T_{ringg}).

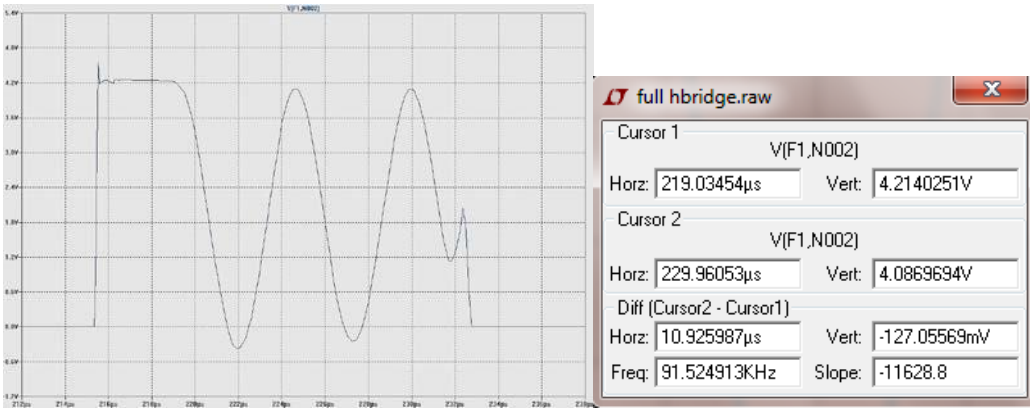


Figure A.3: Ringing drain-to-source voltage.

$$T_{ringg} = \frac{time\ measured}{number\ of\ periods} = \frac{10{,}9259\ .\ 10^{-6}}{2} = 5{,}4629\ \mu s$$

Following the calculation procedure of [20], the total estimated parasitic inductance (L_{ckt}) can be computed as

$$T_{ringg} = 2\,\pi\,\sqrt{L_{ckt} C_{oss}}$$

$$L_{ckt} = \frac{{T_{ringg}}^2}{4\,\pi^2\,C_{oss}} = 3.5160\ mH$$

The snubber resistor needed for damping and also for avoiding the instantaneous discharge of C_{snub} is

$$R_{snub} = \sqrt{\frac{L_{ckt}}{C_{oss}}} = \sqrt{\frac{3{,}516.10^{-3}}{215.10^{-12}}} = 4043.97\,\Omega \approx \mathbf{44}\ k\Omega$$

In order to determine the value for the snubber capacitor, it is necessary to take into account that large values provide over damping and reduce the number of oscillations. This capacitor also stores and dissipates energy every cycle. As the energy dissipated is not very high, it would not be very harmful. It is usual to multiply the ringing period by a constant to compute the time constant of the RC circuit.

The $R_{snub}C_{snub}$ time constant can be expressed as a multiple of the ringing period [20]. Usually 3 is the minimum value selected.

$$C_{snub} = \frac{3.}{R_{snub}} T_{ringg} \approx 44\,nF$$

To provide extra damping, a value of **10 nF** will be selected. The energy stored in the capacitor can be computed as

$$E_{snub} = -C_{snub} \frac{1}{2} .V_{in}^{2} = \frac{1}{2} 4.10^{-9}.15^{2} = 450\,nJ$$

Taking into account the switching frequency (F_{spp}) he power in the capacitance is

$$P_{snub} = E_{snub} . F_{spp} = 450 .10^{-9} . 31250 = 14.06\,mWW$$

The snubber resistor should dissipate this power. The value selected for it is **500Ω.**

A.6 Heatsink

In order to determine the necessity of placing a sink or not in the circuit, some simple calculations can be made. As briefly explained in Chapter 3, the losses that the elements can dissipate depend on their thermal resistors and the maximum temperatures.

$$P_{lost} = \frac{T_{jjmax} - T_{amax}}{(R_{thjjc} + R_{thch} + R_{thha})}$$

From the datasheet of the MOSFET IRF60B217, it is possible to establish the maximum temperature for the junction, which is said to be 175°C. Also, the maximum ambient temperature will be fixed in 40°C.

Regarding the thermal resistors, from the datasheet there are some values available (Figure A.4).

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	1.8	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Figure A.4: Thermal resistances of IRF60B217 [Appendix B]

Thus, in case a sink is not placed, R_{thjja} is 62 °C/W . The maximum dissipated losses are

$$P_{lost} = \frac{175 - 40}{62} = 22,1111144\,WW$$

This value is pretty low for the current application, according to the estimation made with LTSpice. Therefore, a **sink will be attached to every MOSFET.**

Appendix B: Code

In this section, the complete code for the Arduino board is developed, as a complement for the explanation given in previous pages. Also, a table with some PWM frequencies and the values for the registers according computations can be found. It is recommended to write the values by hand instead of relating them to a formula. Otherwise the program does not recognize them and the compiler does not work.

f_pwm	ICR=TOP	n	TOP/2		OCR	
				fs (Hz)	prescaler 8	prescaler 1
62500	255	510	127.5	25500	77	626
60000	266	532	133	26567	74	601
55000	290	581	145	28991	68	551
50000	319	638	159.5	31900	62	501
45000	355	710	177.5	35456	55	450
40000	399	798	199.5	39900	49	400
35000	456	912	228	45614	43	350

Table B1: Values computed for different PWM frequencies.

```
1   //.....VARIABLES  DEFINITION.....
2    // int f_signal=50;                  // Hz. Frequency desired for the output sine.
3   int f_pwm=62500;                     // Hz. PWM frequency.
4   // int TOP (int) (16000000/f_pwm)-1;          // Top value for the resolution selected.
5   int TOP= 255;
6   int n= (TOP * 2);                    // Length of the array.
7   int n= 510;
8   //int fs = n / 0.02;                  // Hz. Sampling frequency.
```

```
int i=0;                          // Cursor 1
int j= n/2. +1;                   // Cursor 2. The voltages must be 180 degrees shifted.
int dutycycle [510];              // Array that contains the values for the dutycycle.
// int dutycycle [n];             // It only works if the value is defined manually.

//.....SETUP.....
void setup () { 16
// PIN DEFINITION.
pinMode (9, OUTPUT);
pinMode (10, OUTPUT);

//.....DUTYCYCLE  COMPUTATION.....
for (i=0; i<=n; i++)
 {
   dutycycle[i] = (int) ( (1 + sin (2.* PI *i/n ))* (TOP/2) + 0.5);
 }

//..... TIMER 1: PWM.....
cli ( );                          // Deactivating global interruptions
TCNT1= 0;                         // Initialize counter value to zero.
TCCR1A = (1<<COM1A1) | (1<<COM1B1) | (1<<WGM11);
// Non-inverting, fast PWM MODE. Clear OC1A/OC1B on Compare match. Mode 14.
TCCR1B= (1<<WGM13) | (1<<WGM12) | (1<<CS10);
// Counts from the bottom to the top and then decreases. No prescaling. 34
// ICR1= (int) (16000000 / f_pwm)-1;
// Overflow value. It sets the resolution of the PWM.
ICR1=TOP;
// In case another PWM frequency is desired, this value must be changed.
OCR1A= dutycycle[i];              // Dutycycle for pin 9
OCR1B= dutycycle[j];              // Dutycycle for pin 10
```

```
41  //.................................. TIMER 2: INTERRUPTION.....................................
42  TCCR2A=0;                          // Setting the entire registers to zero.
43  TCCR2B=0;
44  TCCR2A | = (1<<WGM21);             // Turn on Comparing Output Mode, non PWM.
45  TCCR2B | = (1<<CS21);              // Prescaler at 8.
46  // In case it is changed, the formula below must be changed to the new prescaler.
47  //OCR2A = (byte) ((16000000 / (fs * 8) ) - 1);
48  // Number of pulses it counts until the interruption is activated.
49  OCR2A= 78;
50  TIMSK2 |= (1 << OCIE2A); // Timer 2 Output Compare Match A Interrupt Enable
51  sei ( );                           // Global interruption activation
52  }  //setup
53
54  void loop ( )      {
55  }
56
57  //.....................TIMER 2 INTERRUPT SERVICE ROUTINE.....................
58  ISR (TIMER2_COMPA_vect) {
59  if (i<= n-1)
60  {
61  OCR1A= dutycycle [i];
62   i++;
63  }
64  else { i=0; } ;
65  if ( j<= n-1)
66  {
67   OCR1B= dutycycle[j];
68   j++;
69  }
70  else { j=0; }
71  }  //ISR
```

Appendix C: Modes of Operation in Arduino.

This Appendix collects the Bit Description for the Waveform Generation in Arduino UNO. As explained before, there are 7 Modes of Operation available in Timer 0 and 2 and 15 on Timer 1. Reference: [21].

- **Timer 0:**

Table 15-8. Waveform Generation Mode Bit Description

Mode	WGM02	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on(1)(2)
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	BOTTOM	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

Notes: 1. MAX = 0xFF
2. BOTTOM = 0x00

Figure C.1: Waveform Generation Mode Bit Description for Timer 0 [21]

- **Timer 1:**

Table 16-4. Waveform Generation Mode Bit Description[1]

Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	Timer/Counter Mode of Operation	TOP	Update of OCR1X at	TOV1 Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX

Table 16-4. Waveform Generation Mode Bit Description[1] (Continued)

Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	Timer/Counter Mode of Operation	TOP	Update of OCR1X at	TOV1 Flag Set on
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICR1	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCR1A	BOTTOM	TOP

Note: 1. The CTC1 and PWM11:0 bit definition names are obsolete. Use the WGM12:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

Figure C.2: Waveform Generation Mode Bit Description for Timer 1 [21]

- **Timer 2:**

Table 18-8. Waveform Generation Mode Bit Description

Mode	WGM22	WGM21	WGM20	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on[1][2]
0	0	0	0	Normal	0xFF	Immediate	MAX
1	0	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRA	Immediate	MAX
3	0	1	1	Fast PWM	0xFF	BOTTOM	MAX
4	1	0	0	Reserved	–	–	–
5	1	0	1	PWM, Phase Correct	OCRA	TOP	BOTTOM
6	1	1	0	Reserved	–	–	–
7	1	1	1	Fast PWM	OCRA	BOTTOM	TOP

Notes: 1. MAX= 0xFF
2. BOTTOM= 0x00

Figure C.3: Waveform Generation Mode Bit Description for Timer 2 [21]

Appendix D: Design Documents

Element	Value	Units	Number of units	Reference Name
Capacitors	10	nF	5	
	100	nF	1	
	0.33	µF	1	
	0.47	µF	4	
	2.2	µF	2	
	22	µF	2	
	47	µF	1	
Inductances	470	µH	1	
Resistors	10	Ω	4	
	180	Ω	1	
	500	Ω	4	
	47	kΩ	4	
Diode			6	1N4004
Zener diode 15V			4	1N4728
MOSFET			4	IRF60B217
Driver			2	IR2110
Inverter gate			1	74LS04
Voltage regulator			1	LM7805C

Table D.1: Resume of the components of the circuit.

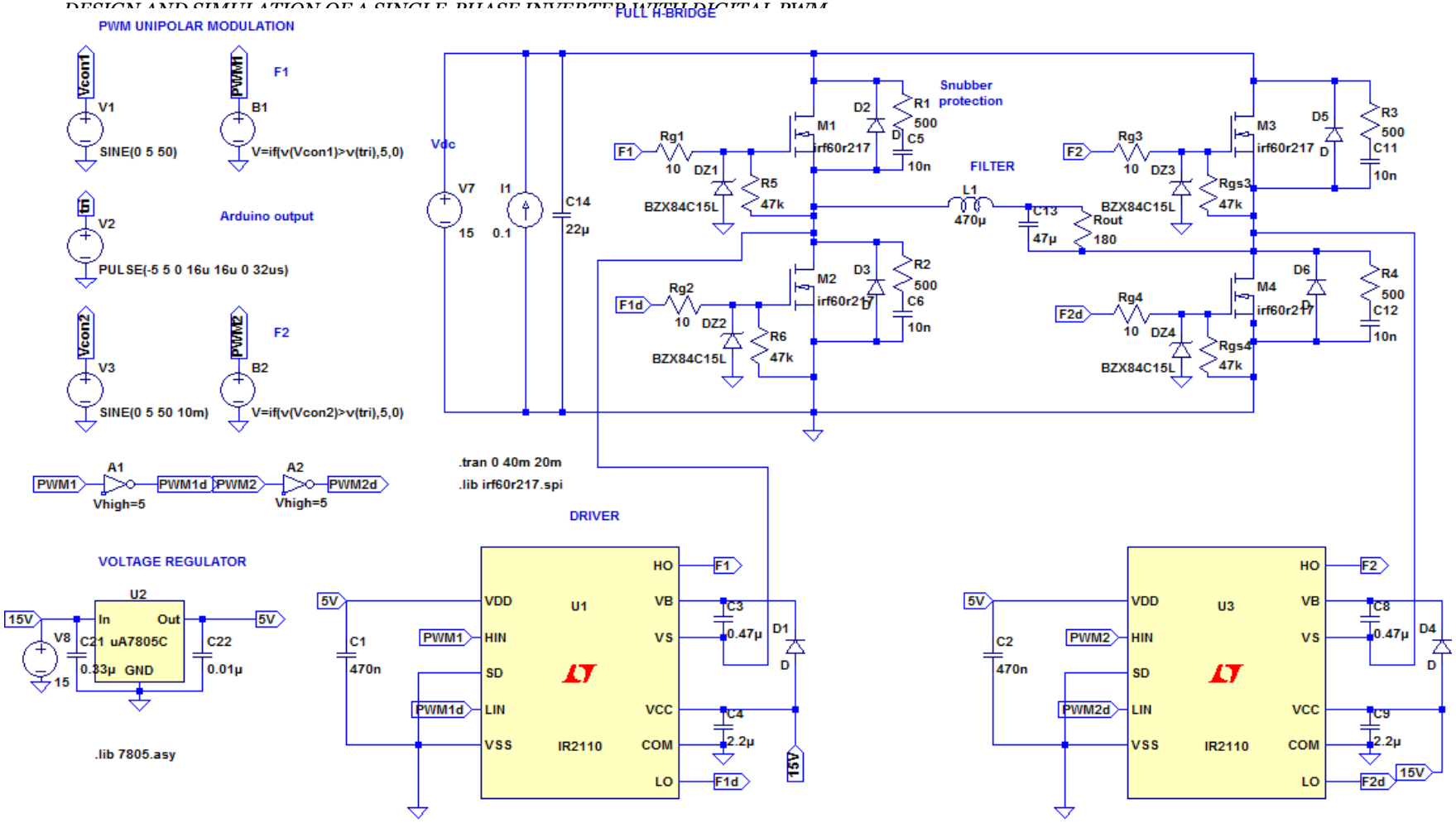


Figure D.1: Schematic with LTSpice software

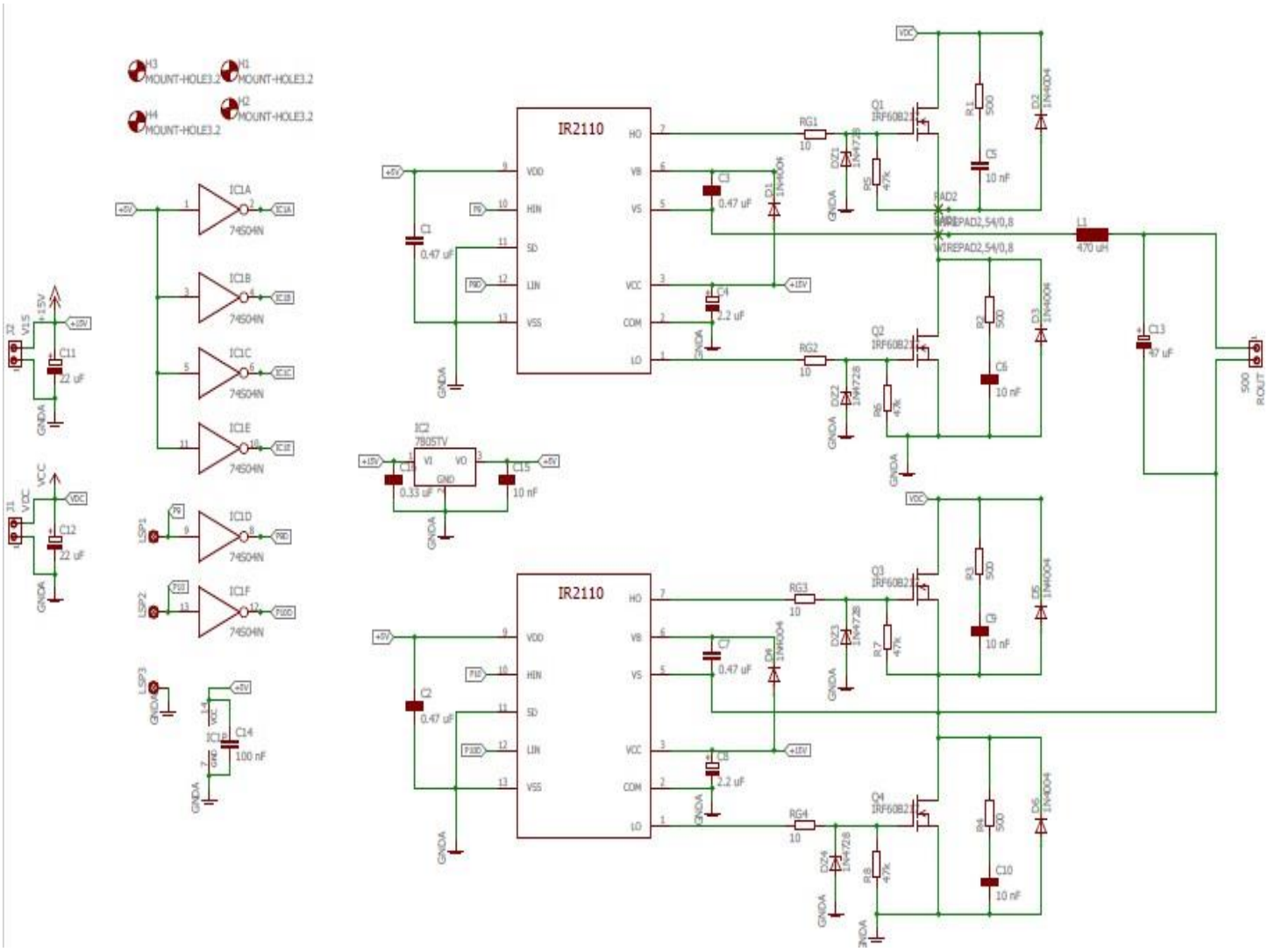


Figure D.2: Schematic with EAGLE software