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1- Introduction :

Writing a bare-metal application from scratch is not hard that you think, in this report I will build a simple bare-metal application in cortex-m3 micro-controller chip which is based on stm32f103c6 chip to toggle led using gpio ports, I will build everything from scratch including startup, linker script, make file and source code, and compile them using arm-non-eabi cross tool chain for arm processors.

I will execute this simple application on a virtual board using protus tool .

2- Specifications to toggle led based on arm-cortex-m3 :

- led is connected to gpio port A13
- to make a gpio toggling in stm32, you need to work with two peripherals:
 - RCC (reset and clock control)
 - GPIO A (general purpose i/o)
- the RCC is must due to the gpio has disabled clock by default.
- base address RCC (0x40021000)

- GPIO port A (0x40010800)
- APB2ENR (0x18) which is responsible for enable port A on its pin 2.
- CRH Register (0x04) to start signal to write on portA
- ODR Register (0x0c) to write 1 or 0 on bit 13.

3- Source code

3.1 – main application code

```

1
2 typedef volatile unsigned int vuint32_t;
3
4 #include<stdint.h>
5
6 #define RCC_BASE      0x40021000
7 #define GPIOA_BASE    0x40010800
8
9 #define RCC_APB2ENR    *(volatile uint32_t *) (RCC_BASE + 0x18)
10 #define GPIOA_CRH      *(volatile uint32_t *) (GPIOA_BASE + 0x04)
11 #define GPIOA_ODR      *(volatile uint32_t *) (GPIOA_BASE + 0x0c)
12 //////////////////////////////////////////////////
13 #define RCC_IOPAEN     (1<<2)
14
15 typedef union {
16     vuint32_t      all_field;
17     struct{
18         vuint32_t   reserved:13;
19         vuint32_t   p_13:1;
20     }Spin;
21 } U_R_ODR_t ;
22
23 volatile U_R_ODR_t*  R_ODR=  (volatile U_R_ODR_t*)(GPIOA_BASE+0x0c);
24
25 int main(void)
26 {
27     int i;
28     RCC_APB2ENR |= RCC_IOPAEN;
29     GPIOA_CRH   &= 0xFF0FFFFF;
30     GPIOA_CRH   |= 0x00200000;
31     while(1){
32         R_ODR->Spin.p_13=1;
33         for(i=0;i<5000;i++);
34         R_ODR->Spin.p_13=0;
35         for(i=0;i<5000;i++);
36     }
37     return 0;
38 }

```

In the main application code , which I called “app.c” I defined RCC_base and GPIOA addresses , and defined some registers to reference to base addresses and offset to drive to its destination , and make an union variable to control bits of port A , in the main I set RCC_register with bit 2 to 1,make CRH Register from bit 20-24 set to 2 in binary, and make pin13 to be on set it by 1 and make a delay then make pin 13 to be on clear by 0 and then delay again this is in continuous switching.

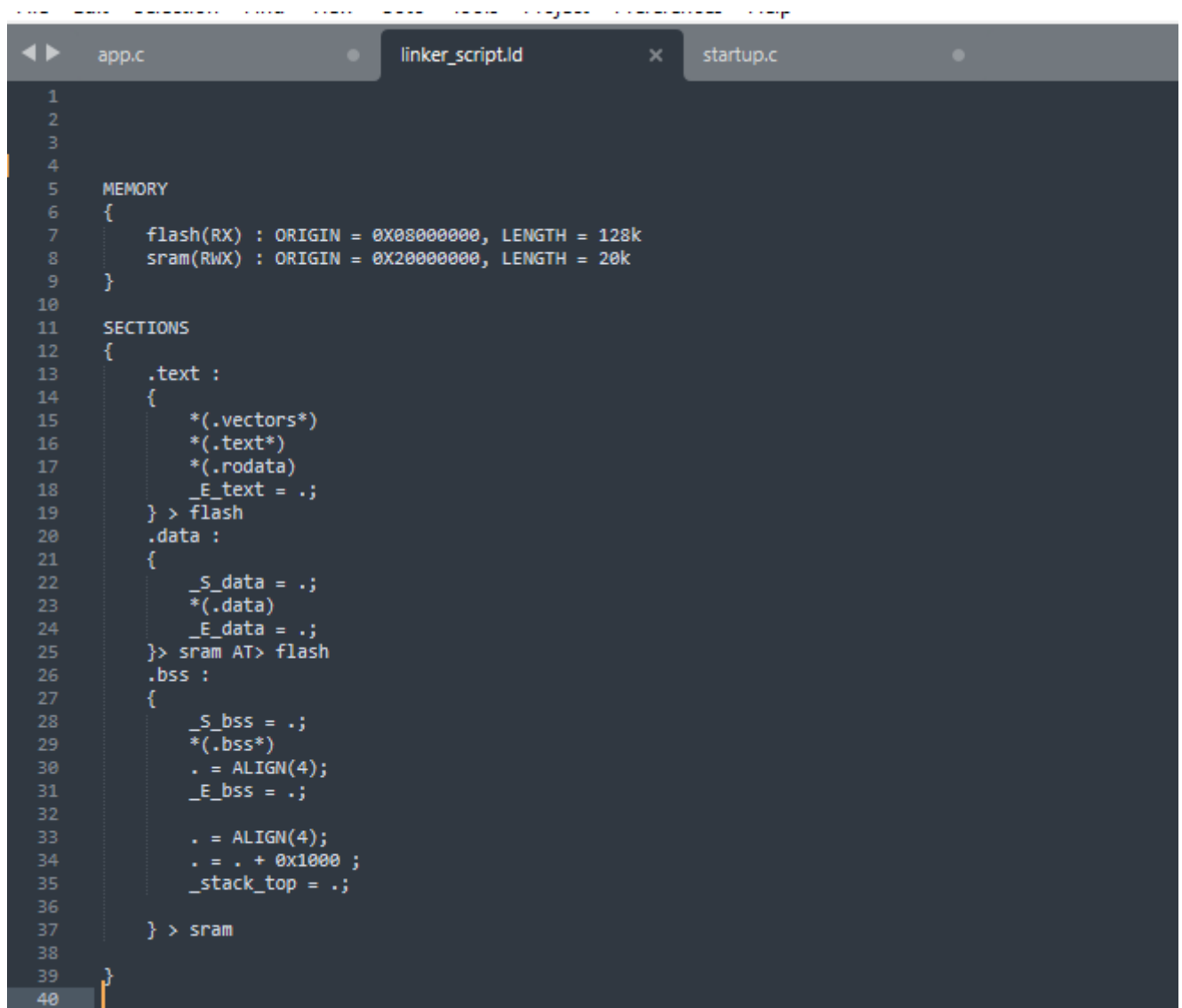
3.2- startup with c :

```
app.c | linker_script.ld | startup.c
4  #include <stdint.h>
5  extern int main();
6  extern int _stack_top;
7  void Reset_Handler();
8
9  void Default_Handler(){
10     Reset_Handler();
11 }
12 void NMI_Handler() __attribute__((weak,alias("Default_Handler")));
13 void H_Fault_Handler() __attribute__((weak,alias("Default_Handler")));
14 void MM_Fault_Handler() __attribute__((weak,alias("Default_Handler")));
15 void Bus_Fault() __attribute__((weak,alias("Default_Handler")));
16 void Usage_Fault_Handler() __attribute__((weak,alias("Default_Handler")));
17
18 uint32_t vectors[] __attribute__((section(".vectors"))) = {
19     (uint32_t)&_stack_top,
20     (uint32_t)&NMI_Handler,
21     (uint32_t)&H_Fault_Handler,
22     (uint32_t)&MM_Fault_Handler,
23     (uint32_t)&Bus_Fault,
24     (uint32_t)&Usage_Fault_Handler
25 };
26
27 extern unsigned int _S_data;
28 extern unsigned int _E_data;
29 extern unsigned int _S_bss;
30 extern unsigned int _E_bss;
31 extern unsigned int _E_text;
32
33 void Reset_Handler(){
34     //copy data from rom to ram
35     unsigned int data_size=(unsigned char*)&_E_data - (unsigned char*)&_S_data;
36     unsigned char* p_src =(unsigned char*)&_E_text;
37     unsigned char* p_dst =(unsigned char*)&_S_data;
38     int i;
39     for(i=0;i<data_size;i++){
40         *((unsigned char*)p_dst++)=*((unsigned char*)p_src++);
41     }
42     //init bss with zero
43     unsigned int bss_size=(unsigned char*)&_E_bss - (unsigned char*)&_S_bss;
44
45     p_dst =(unsigned char*)&_S_bss;
46
47     for(i=0;i<bss_size;i++){
48         *((unsigned char*)p_dst++)=(unsigned char) 0;
49     }
50     // jump to main
51     main();
```

I know startup should be written in assembly to set stack pointer and branch label to it then branch label to main but in cortex m3 stack is labeled when power is applied to MCU the (pc) value will be 0 which mapped to (0x08000000) and will start at the same address which point to stack .

In this startup.c , I defined an array which holds every handlers and entry (SP) according to (IVT),and put it in vectors section, and I defined handlers to be weak and alias to override in user code and cause declaration to be emitted for another symbol, and I copy data from rom to ram and initialize bss in ram then jump to main.

3.3- linker script

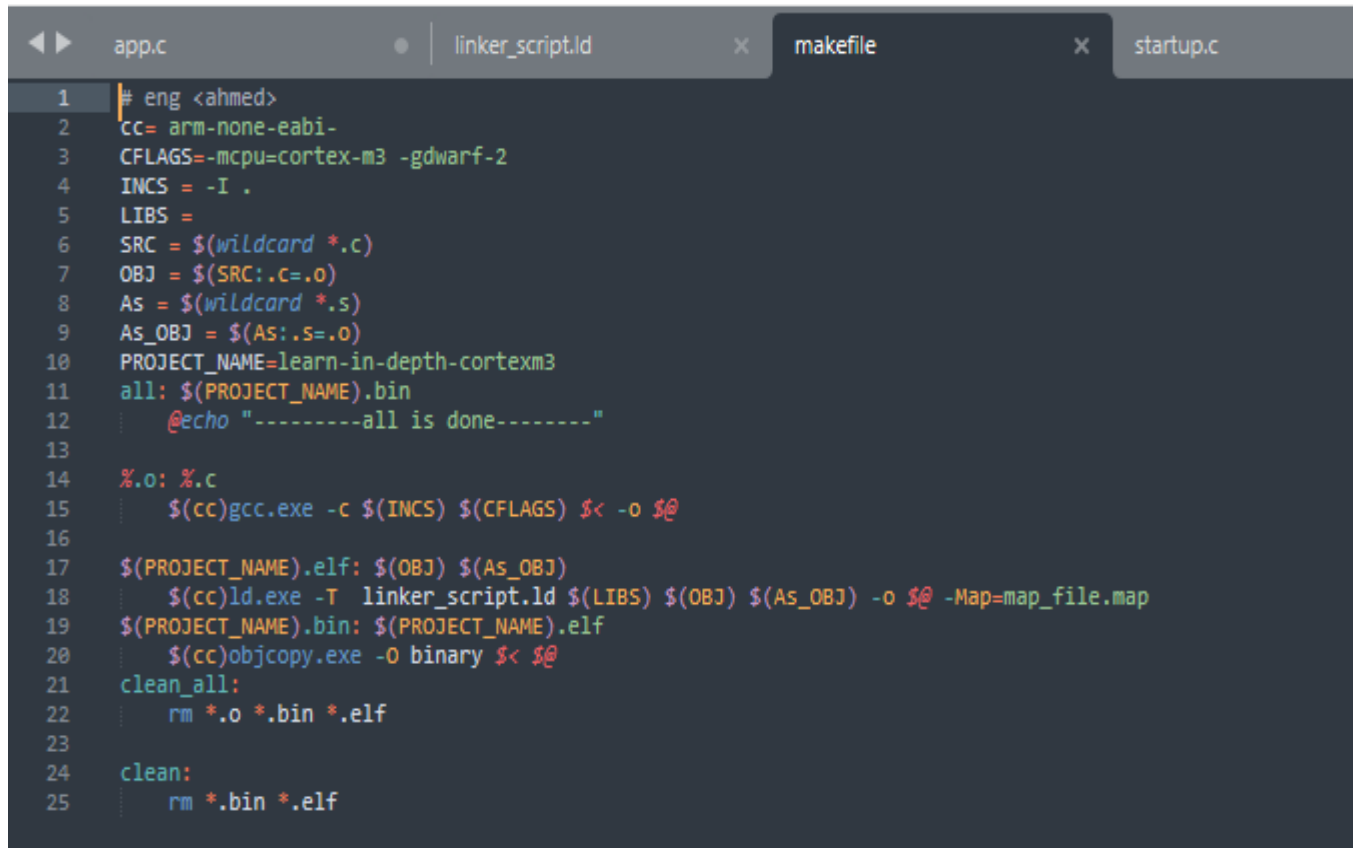


```
1
2
3
4
5 MEMORY
6 {
7     flash(RX) : ORIGIN = 0X08000000, LENGTH = 128k
8     sram(RWX) : ORIGIN = 0X20000000, LENGTH = 20k
9 }
10
11 SECTIONS
12 {
13     .text :
14     {
15         *(.vectors*)
16         *(.text*)
17         *(.rodata)
18         _E_text = .;
19     } > flash
20     .data :
21     {
22         _S_data = .;
23         *(.data)
24         _E_data = .;
25     } > sram AT> flash
26     .bss :
27     {
28         _S_bss = .;
29         *(.bss*)
30         . = ALIGN(4);
31         _E_bss = .;
32
33         . = ALIGN(4);
34         . = . + 0x1000 ;
35         _stack_top = .;
36     } > sram
37
38
39 }
40
```

In this linker script file I defined two memory flash and sram with its addresses and lengths ,then I made sections like (.text)

Which contain (.vectors,.text,rodata) and mapped it flash ,and then made (.data) section of all initialized data and (.bss) for all uninitialized data , and I made a locator counter to count addresses to jump stack and take some memory .

3.4 – make file :



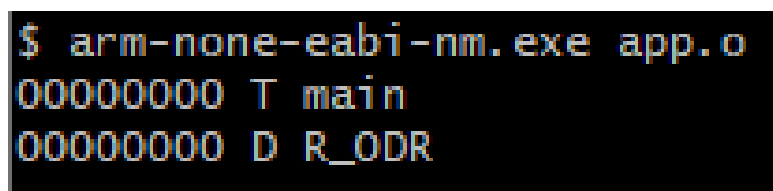
```
1 # eng <ahmed>
2 cc= arm-none-eabi-
3 CFLAGS=-mcpu=cortex-m3 -gdwarf-2
4 INCS = -I .
5 LIBS =
6 SRC = $(wildcard *.c)
7 OBJ = $(SRC:.c=.o)
8 AS = $(wildcard *.s)
9 AS_OBJ = $(AS:.s=.o)
10 PROJECT_NAME=learn-in-depth-cortexm3
11 all: $(PROJECT_NAME).bin
12     @echo "-----all is done-----"
13
14 %.o: %.c
15     $(cc)gcc.exe -c $(INCS) $(CFLAGS) $< -o $@
16
17 $(PROJECT_NAME).elf: $(OBJ) $(AS_OBJ)
18     $(cc)ld.exe -T linker_script.ld $(LIBS) $(OBJ) $(AS_OBJ) -o $@ -Map=map_file.map
19 $(PROJECT_NAME).bin: $(PROJECT_NAME).elf
20     $(cc)objcopy.exe -O binary $< $@
21 clean_all:
22     rm *.o *.bin *.elf
23
24 clean:
25     rm *.bin *.elf
```

This make file is optimize compiling the program , so I used some make feature to do it like simplifaction dry and wildcards.

4- symbols:

Using nm binary utility, I can hack every binary file and see its symbols and which section every symbol belongs to and address of every symbol. In object files there is only virtual addresses, and every symbol will take a real load address after linking process in the elf image.

4.1 app.o symbols



```
$ arm-none-eabi-nm.exe app.o
00000000 T main
00000000 D R_ODR
```

- this object file contains two symbols,
1. Main: which is in text section.
 2. R_ODR: which is in data section.

4.2 elf image symbols

```
des/PCES/Tab2_WFen_2
$ arm-none-eabi-nm.exe learn-indepth-cortex-m3.elf
20000004 B _E_bss
20000004 D _E_data
0800017c T _E_text
20000004 B _S_bss
20000000 D _S_data
20001004 B _stack_top
080000c0 W Bus_Fault
080000c0 T Default_Handler
080000c0 W H_Fault_Handler
08000018 T main
080000c0 W MM_Fault_Handler
080000c0 W NMI_Handler
20000000 D R_ODR
080000cc T Reset_Handler
080000c0 W Usage_Fault_Handler
08000000 T vectors

soft@DESKTOP-VJG2KBC MINGW64 /d/mastering_embedded_di
```

4.3 startup.o symbols

```
$ arm-none-eabi-nm.exe startup.o
                 U _E_bss
                 U _E_data
                 U _E_text
                 U _S_bss
                 U _S_data
                 U _stack_top
00000000 W Bus_Fault
00000000 T Default_Handler
00000000 W H_Fault_Handler
                 U main
00000000 W MM_Fault_Handler
00000000 W NMI_Handler
0000000c T Reset_Handler
00000000 W Usage_Fault_Handler
00000000 D vectors
```

5- Sections Headers:

In this section we just care about .text, .data, .bss and .rodata sections, linker may add some other sections like .ARM.attributes and .comment but we don't care about these sections as it will be excluded in the final executable file and wont be loaded the micro-controller.

5.1 app.o sections header

```
ges/lec3/lec3_Writing_C
$ arm-none-eabi-objdump.exe -h app.o

app.o:      file format elf32-littlearm

Sections:
Idx Name          Size      VMA           LMA           File off  Algn
 0 .text          000000a8  00000000  00000000  00000034  2**2
    CONTENTS, ALLOC, LOAD, RELOC, READONLY, CODE
 1 .data          00000004  00000000  00000000  000000dc  2**2
    CONTENTS, ALLOC, LOAD, DATA
 2 .bss           00000000  00000000  00000000  000000e0  2**0
    ALLOC
 3 .debug_info     00000124  00000000  00000000  000000e0  2**0
    CONTENTS, RELOC, READONLY, DEBUGGING
 4 .debug_abbrev   000000bf  00000000  00000000  00000204  2**0
    CONTENTS, READONLY, DEBUGGING
 5 .debug_loc      00000038  00000000  00000000  000002c3  2**0
    CONTENTS, READONLY, DEBUGGING
 6 .debug_aranges  00000020  00000000  00000000  000002fb  2**0
    CONTENTS, RELOC, READONLY, DEBUGGING
 7 .debug_line     0000009d  00000000  00000000  0000031b  2**0
    CONTENTS, RELOC, READONLY, DEBUGGING
 8 .debug_str      00000123  00000000  00000000  000003b8  2**0
    CONTENTS, READONLY, DEBUGGING
 9 .comment        00000012  00000000  00000000  000004db  2**0
    CONTENTS, READONLY
10 .ARM.attributes 00000033  00000000  00000000  000004ed  2**0
    CONTENTS, READONLY
11 .debug_frame    0000002c  00000000  00000000  00000520  2**2
    CONTENTS, RELOC, READONLY, DEBUGGING
```

5.3 startup.o sections

```
$ arm-none-eabi-objdump.exe -h startup.o

startup.o:   file format elf32-littlearm

Sections:
Idx Name          Size      VMA           LMA           File off  Algn
 0 .text          000000bc  00000000  00000000  00000034  2**2
    CONTENTS, ALLOC, LOAD, RELOC, READONLY, CODE
 1 .data          00000000  00000000  00000000  000000f0  2**0
    CONTENTS, ALLOC, LOAD, DATA
 2 .bss           00000000  00000000  00000000  000000f0  2**0
    ALLOC
 3 .vectors        00000018  00000000  00000000  000000f0  2**2
    CONTENTS, ALLOC, LOAD, RELOC, DATA
 4 .debug_info     00000167  00000000  00000000  00000108  2**0
    CONTENTS, RELOC, READONLY, DEBUGGING
 5 .debug_abbrev   000000c0  00000000  00000000  0000026f  2**0
    CONTENTS, READONLY, DEBUGGING
 6 .debug_loc      00000064  00000000  00000000  0000032f  2**0
    CONTENTS, READONLY, DEBUGGING
 7 .debug_aranges  00000020  00000000  00000000  00000393  2**0
    CONTENTS, RELOC, READONLY, DEBUGGING
 8 .debug_line     000000af  00000000  00000000  000003b3  2**0
    CONTENTS, RELOC, READONLY, DEBUGGING
 9 .debug_str      0000016c  00000000  00000000  00000462  2**0
    CONTENTS, READONLY, DEBUGGING
10 .comment        00000012  00000000  00000000  000005ce  2**0
    CONTENTS, READONLY
11 .ARM.attributes 00000033  00000000  00000000  000005e0  2**0
    CONTENTS, READONLY
12 .debug_frame    0000004c  00000000  00000000  00000614  2**2
    CONTENTS, RELOC, READONLY, DEBUGGING
```

5.4 final elf image sections

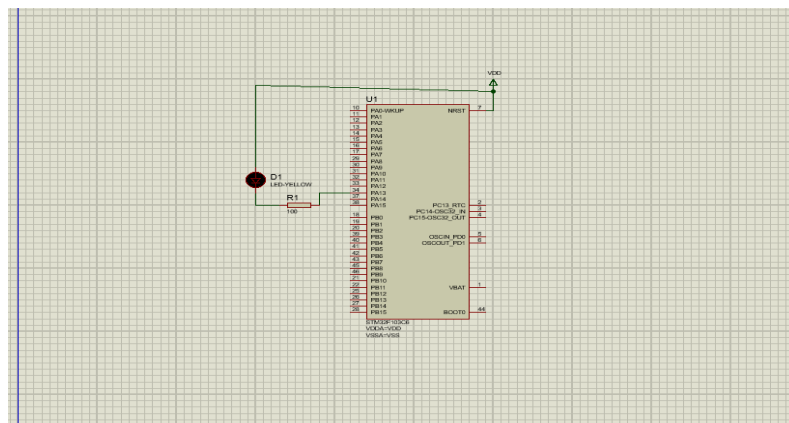
```
$ arm-none-eabi-objdump.exe -h learn-indepth-cortex-m3.elf

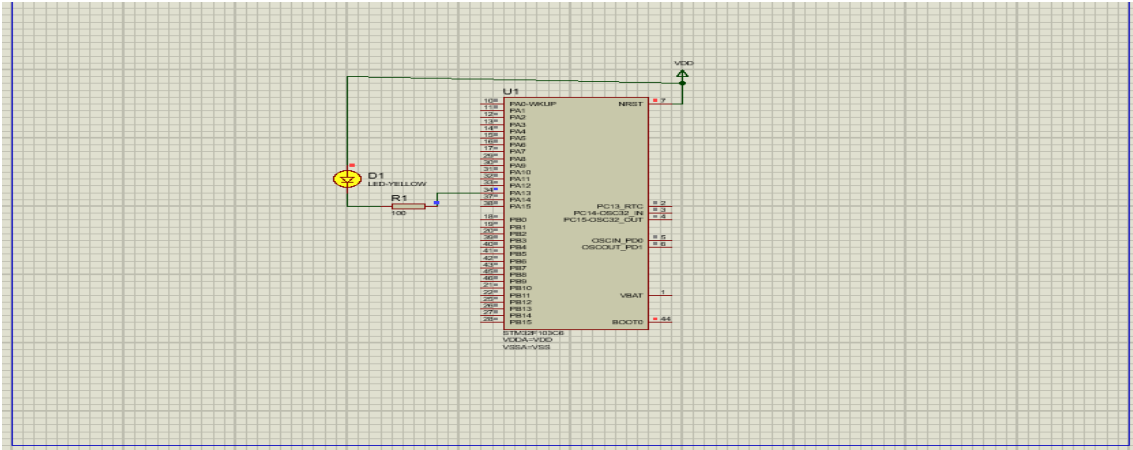
learn-indepth-cortex-m3.elf:      file format elf32-littlearm

Sections:
Idx Name          Size      VMA       LMA       File off  Algn
  0 .text          0000017c 08000000 08000000 00008000 2**2
    CONTENTS, ALLOC, LOAD, READONLY, CODE
  1 .data          00000004 20000000 0800017c 00010000 2**2
    CONTENTS, ALLOC, LOAD, DATA
  2 .bss           00001000 20000004 08000180 00010004 2**0
    ALLOC
  3 .debug_info     0000028b 00000000 00000000 00010004 2**0
    CONTENTS, READONLY, DEBUGGING
  4 .debug_abbrev   0000017f 00000000 00000000 0001028f 2**0
    CONTENTS, READONLY, DEBUGGING
  5 .debug_loc      0000009c 00000000 00000000 0001040e 2**0
    CONTENTS, READONLY, DEBUGGING
  6 .debug_aranges  00000040 00000000 00000000 000104aa 2**0
    CONTENTS, READONLY, DEBUGGING
  7 .debug_line     0000014c 00000000 00000000 000104ea 2**0
    CONTENTS, READONLY, DEBUGGING
  8 .debug_str      00000171 00000000 00000000 00010636 2**0
    CONTENTS, READONLY, DEBUGGING
  9 .comment        00000011 00000000 00000000 000107a7 2**0
    CONTENTS, READONLY
10 .ARM.attributes 00000033 00000000 00000000 000107b8 2**0
    CONTENTS, READONLY
11 .debug_frame     00000078 00000000 00000000 000107ec 2**2
    CONTENTS, READONLY, DEBUGGING
```

All sections now have the real load memory addresses which is given to every section in linker script.

6- run application on protus





7 – Debug with protus

lab2 - Proteus 8 Professional - Source Code

File Project Build Edit Debug System Help

Schematic Capture Source Code

CM3 Source Code - U1

startup.c

```

-----
#include<stdint.h>
extern int main();
extern int _stack_top;
void Reset_Handler();

80000000 void Default_Handler() {
80000004   Reset_Handler();
80000008 }
-----
void NMI_Handler() __attribute__((weak, alias("Default_Handler")));
void H_Fault_Handler() __attribute__((weak, alias("Default_Handler")));
void MM_Fault_Handler() __attribute__((weak, alias("Default_Handler")));
void Bus_Fault() __attribute__((weak, alias("Default_Handler")));
void Usage_Fault_Handler() __attribute__((weak, alias("Default_Handler")));

-----
uint32_t vectors[] __attribute__((section(".vectors"))) = {
-----
  (uint32_t)&_stack_top,
  (uint32_t)&NMI_Handler,
  (uint32_t)&H_Fault_Handler,

```

CM3 Variables - U1

Name	Address	Value
vectors	08000000	dw0rd[6]
vectors[0]	08000000	536875012
vectors[1]	08000004	134217921
vectors[2]	08000008	134217921
vectors[3]	0800000C	134217921
vectors[4]	08000010	134217921
vectors[5]	08000014	134217921
R_ODR	20000000	0x00000000
R_ODR	00000000	0x04 0x10 0x00 0x20
all_field	00000000	536875012
spin	00000000	0x04 0x10 0x00 0x20
reserved	00000000	4100
p_13	00000000	0

3 Message(s)

PAUSED: 0.002500750s



Schematic Capture Source Code

CM3 Source Code - U1

app.c

```
----- #define RCC_IOPAEN (1<<2)
-----
----- typedef union {
-----     vuInt32_t    all_field;
-----     struct {
-----         vuInt32_t    reserved:13;
-----         vuInt32_t    p_13:1;
-----     } spin;
----- } U_R_ODR_t;
-----
----- volatile U_R_ODR_t* R_ODR= (volatile U_R_ODR_t*)(GPIOA_BASE+0x0C);
-----
----- int main(void)
8000018 {
-----     int i;
-----     RCC_APB2ENR |= RCC_IOPAEN;
8000036 GPIOA_CRH |= 0xFFFFFFF;
800004E GPIOA_CRH |= 0x00200000;
-----     while(1){
```

CM3 Variables - U1

Name	Address	Value
vectors	08000000	dword[6]
vectors[0]	08000000	536875012
vectors[1]	08000004	134217921
vectors[2]	08000008	134217921
vectors[3]	0800000C	134217921
vectors[4]	08000010	134217921
vectors[5]	08000014	134217921
R_ODR	20000000	0x00000000
R_ODR	00000000	0x04 0x10 0x00 0x20
all_field	00000000	536875012
spin	00000000	0x04 0x10 0x00 0x20
reserved	00000000	4100
p_13	00000000	0

3 Message(s) PAUSED: 0.002500750s