Layout Design and Simulation (IC Design Flow)

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Outlines

- Living in a 3D World
- Design Rules Check
- MOSFET Layout
- CMOS Inverter
  - Layout Editor
  - DRC
  - LVS
- Cadence Hot Keys
- Discussion

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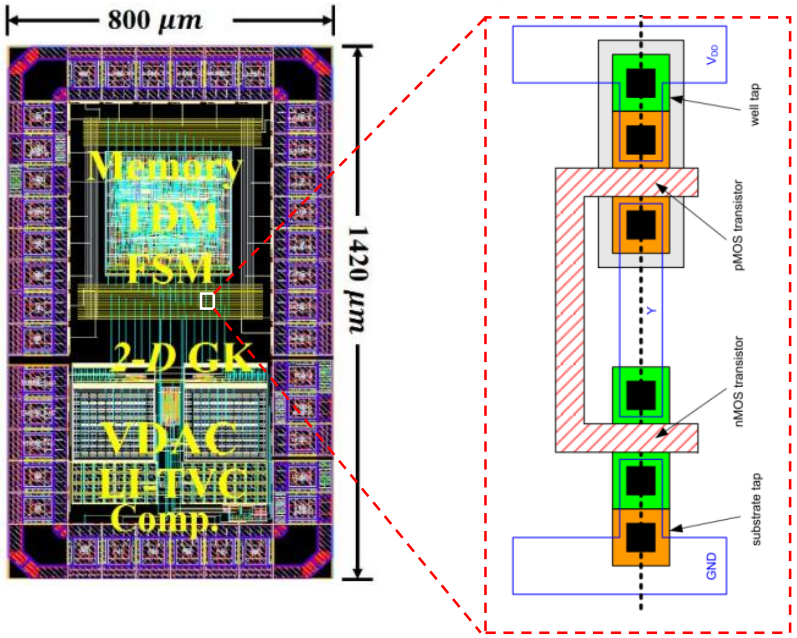
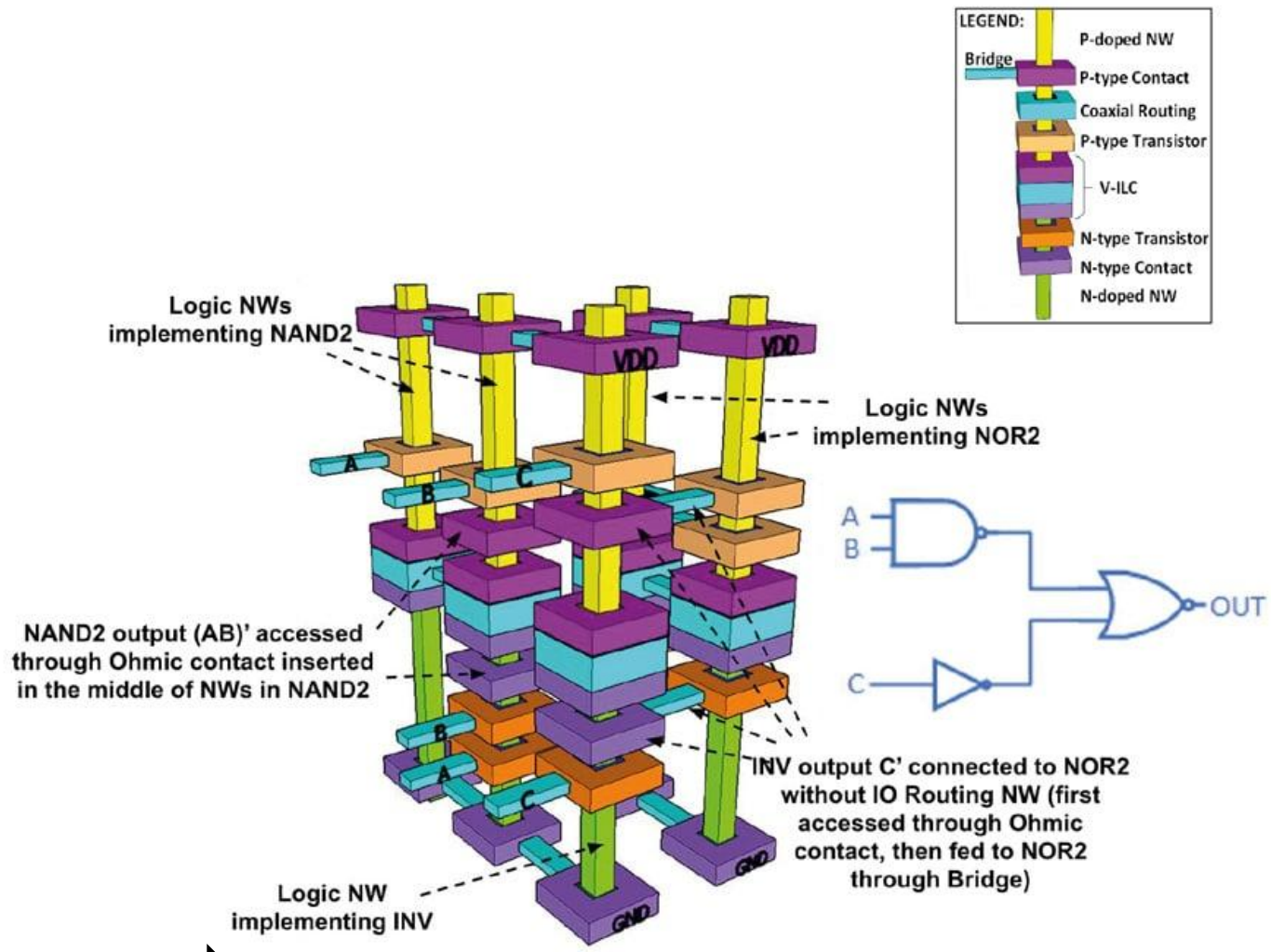
Living in a 3D World (1/2)

- **Your Job**
  - **Create Layout**



- **Manufacture's task**
  - **Fabricate the Layout**

Fabrication process controls vertical dimensions



Circuit for a combinational logic function with NAND, NOR and INV logic gates.

Living in a 3D World (2/2)

- Layout is a group of planer geometries drawn on different colored layers corresponding to different masks used in fabrication (Each layer has unique color)
- Planer dimensions are mainly set by design through mask dimensions.
- Designer is typically concerned with both schematic and layout "views" of the design .
- Once layout is completely done, the tool generate a special GDSII format (tapeout) to send to IC fabrication facility.

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Depending on fab & process

Fabrication process also sets some constraints on planer dimensions (Design Rules Check)

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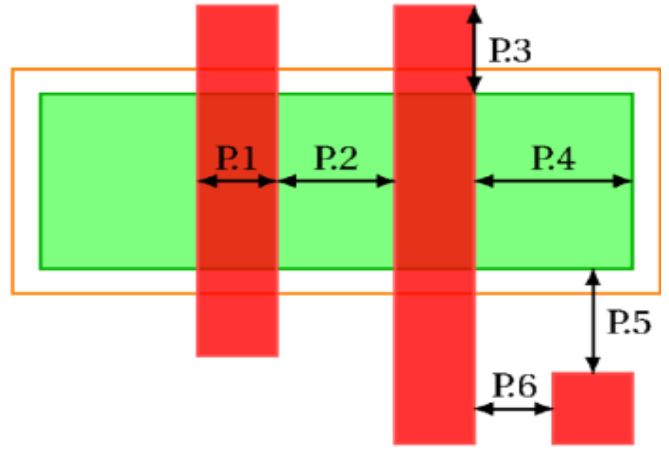
Design Rules Check (1/5)

- Design Rules Check (DRCs) are the interface between the designer and process engineer.
- They provide guidelines for constructing process masks .
- These are generally categorized as:
  - **Intra-layer rules**: minimum widths, spacing, area, etc., only relating to a single layer.
  - **Inter-layer rules**: minimum enclosures, extensions, overlaps,… etc., between two layers.
  - **Special rules**: non geometric rules, such as antenna rules, density, distance to well tap, …etc.



Poly	Rule name (minimum)	Length
P.1	Poly width	65nm
P.2	Space poly and active	80nm
P.3	Poly extension beyond active	30nm
P.4	Enclosure active around gate	85nm
P.5	Space field poly to active	70nm
P.6	Space field poly	25nm

We can create wider or longer transistors, ploy, metal …. But you waste silicon area and generate parasitic elements

Design Rules Check (2/5)

XH018 BASIC DESIGN RULES

Mask	width [µm]	Spacing [µm]
N-well	0.86	1.4
Active Area	0.22	0.28
Poly-silicon Gate	0.18	0.25
Poly-silicon Resistor	0.44	0.44
Contact	0.22	0.25
Metal 1	0.23	0.23
Via 1, 2, 3, 4	0.26	0.26
Metal 2, 3, 4, 5	0.28	0.28
Top Via	0.36	0.35
Top Metal	0.44	0.46
Thick Metal	3.0	2.5

XH035 BASIC DESIGN RULES

Mask	width [µm]	Spacing [µm]
N-well	1.6	1.0
Active Area	0.5	0.6
Poly-silicon Gate/Resistor	0.35	0.45
Contact	0.4	0.4
Metal 1, Via 1, 2, 3	0.5	0.45
Metal 2, 3	0.6	0.5 (0.6 if Top Layer Metal)
Metal 4	0.6	0.6
Thick Metal	3.0	2.5

XFAB
MIXED-SIGNAL FOUNDRY EXPERTS

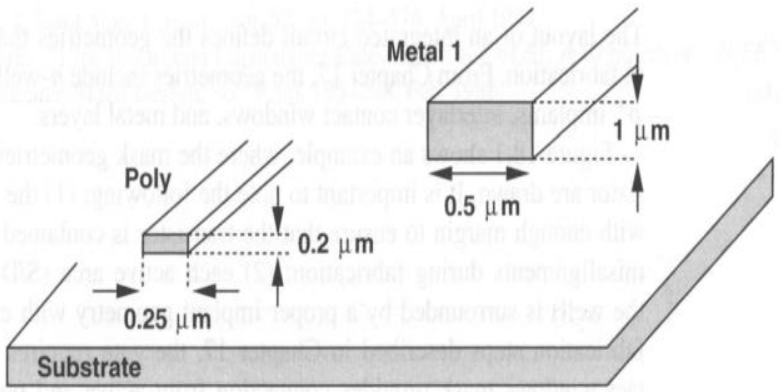
0.18 µm Process Family:

› XH018

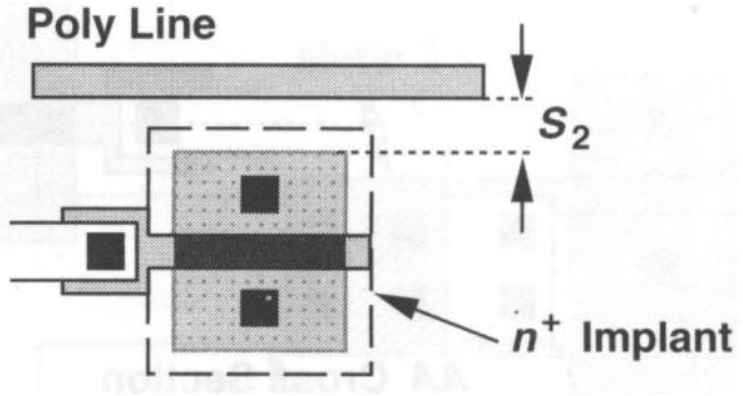
0.35 µm Process Family:

› XH035

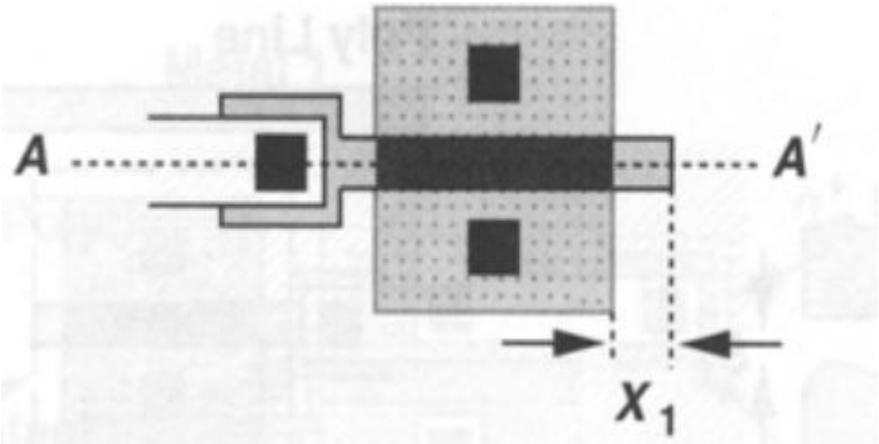
Design Rules Check (3/5)



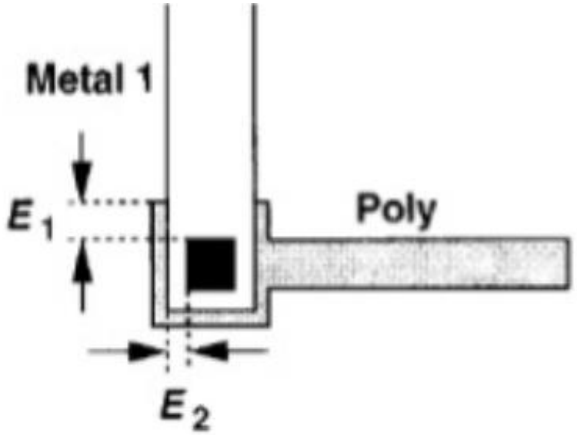
Minimum Width Rules



Minimum Spacing Rules



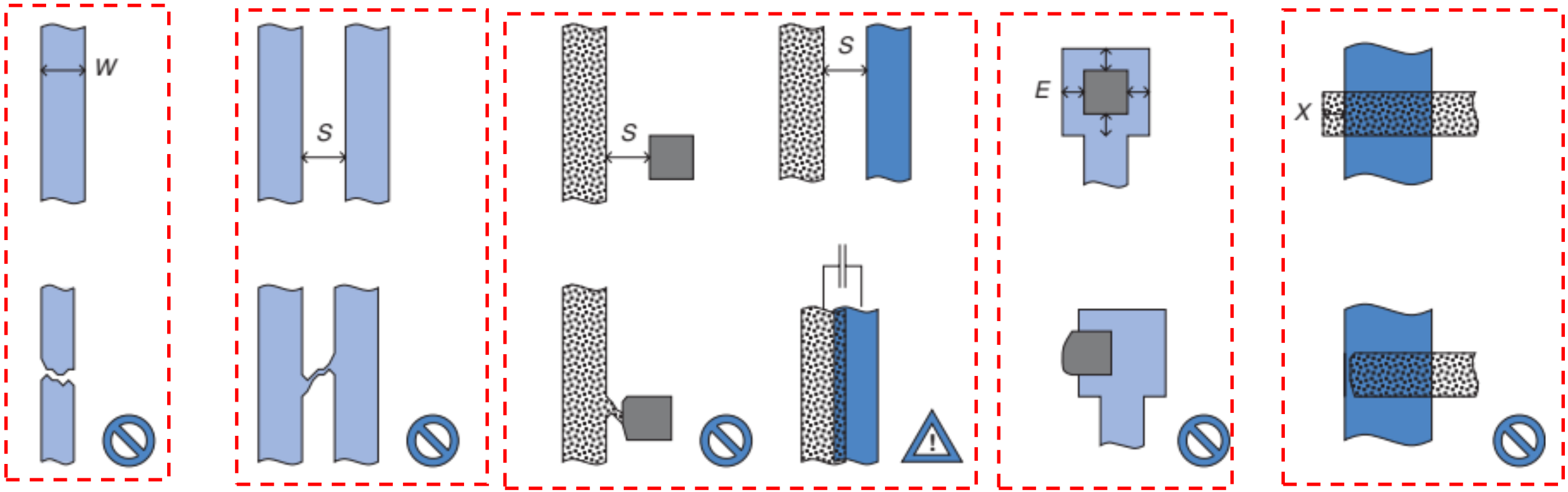
Minimum Extension Rules



Minimum Enclosure Rules

Design Rules Check (4/5)

- What happens to transistor if min extension of poly is not observed.



Min. Width

Min. Interalayer spacing

Min. Interlayer spacing

Min. enclosure

Min. extension

Design Rules Check (5/5)

- In practical, DRCs of the layout are very complicated.
- Checked by a software CAD tool (industry standard DRC tool)
  - Assura (Cadenc)
  - Calibre (Mentor Graphics)
  - Hercules (Synopsys)
- Generally, the foundry will not accept any design with DRC errors
  - All errors must be fixed
  - In special cases, minor DRC errors can be accepted by the foundry (but you must request an official DRC error waiver)

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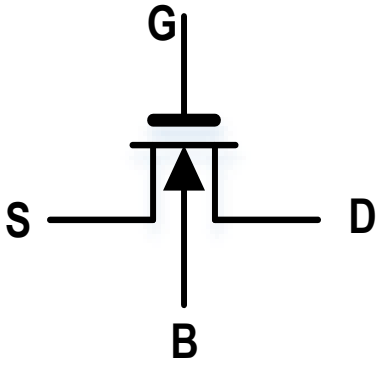
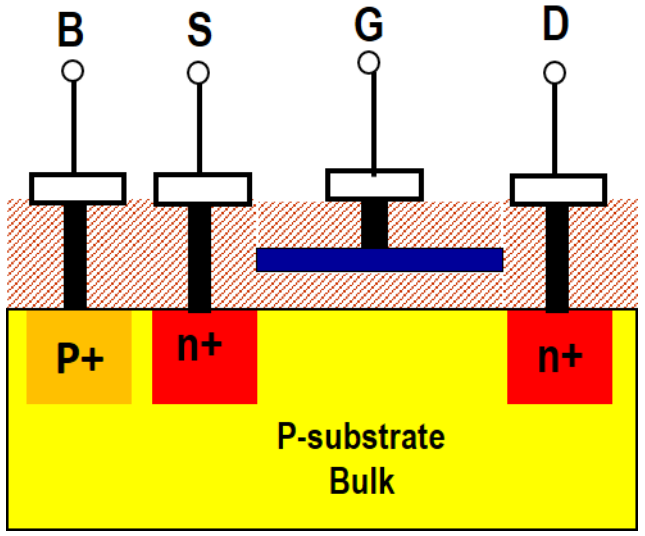
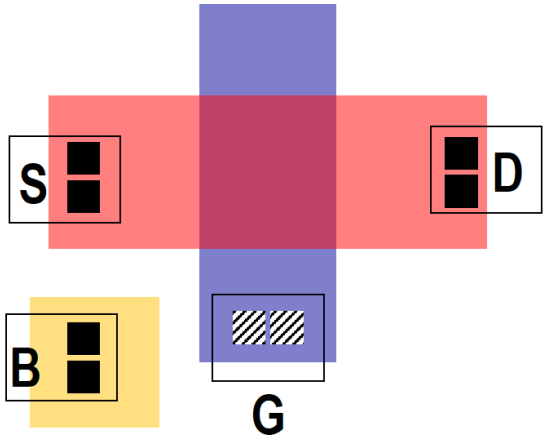
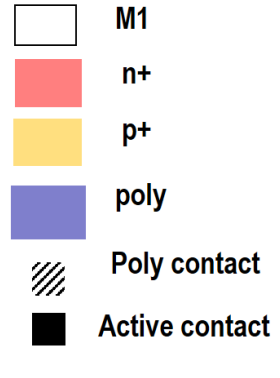
MOSFET Layout (1/2)

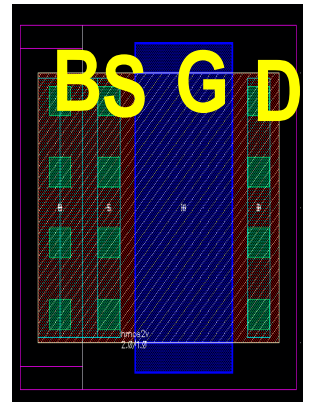
n-MOSFET



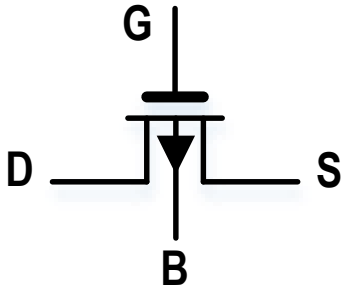


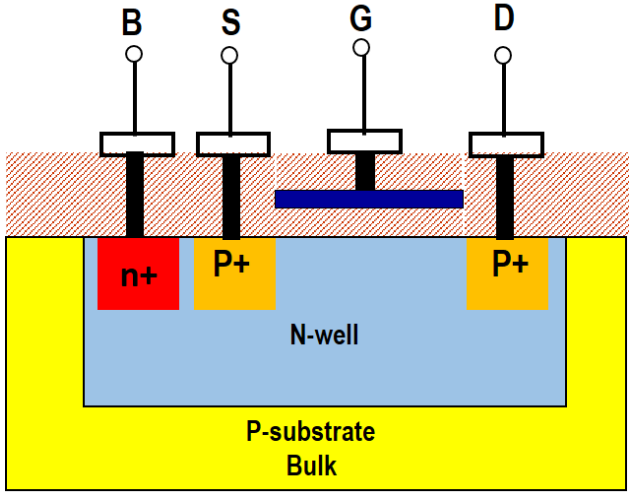


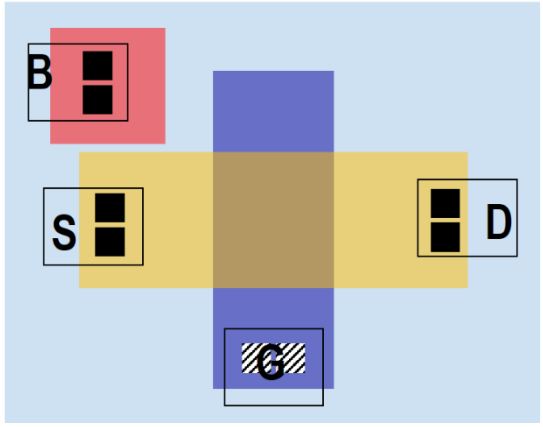


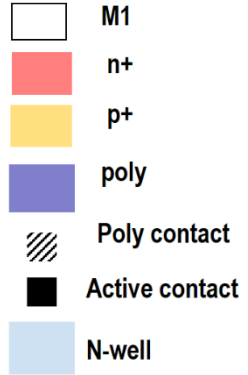


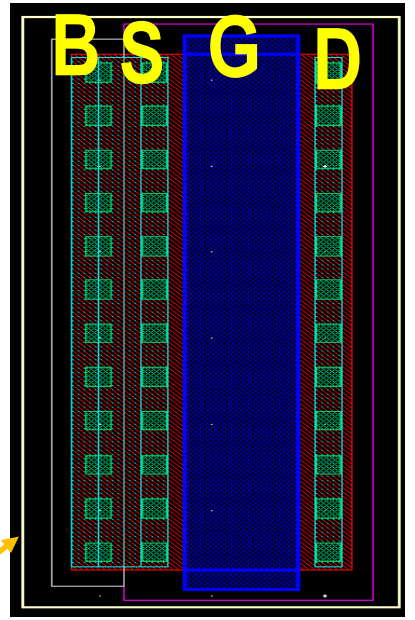
P-MOSFET











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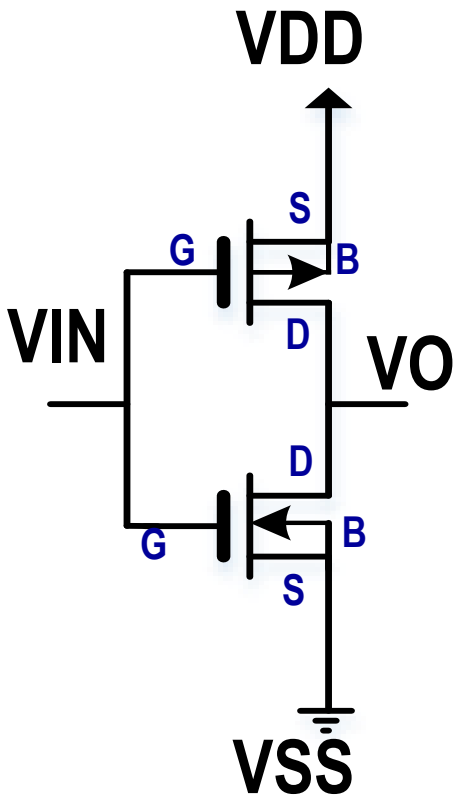
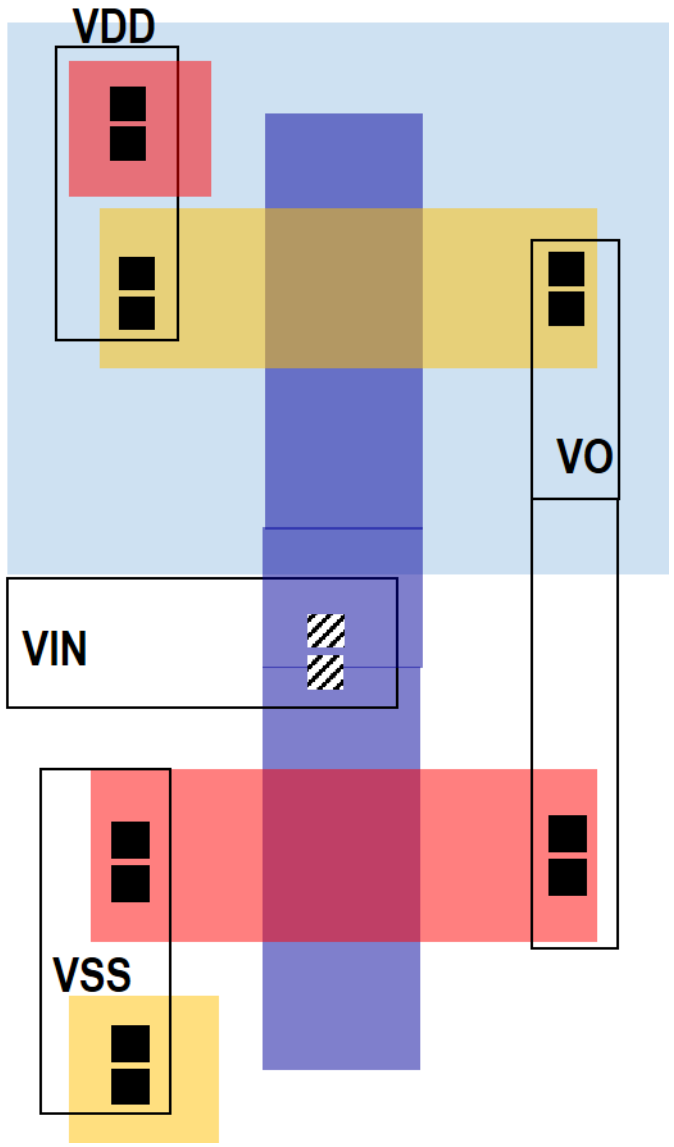
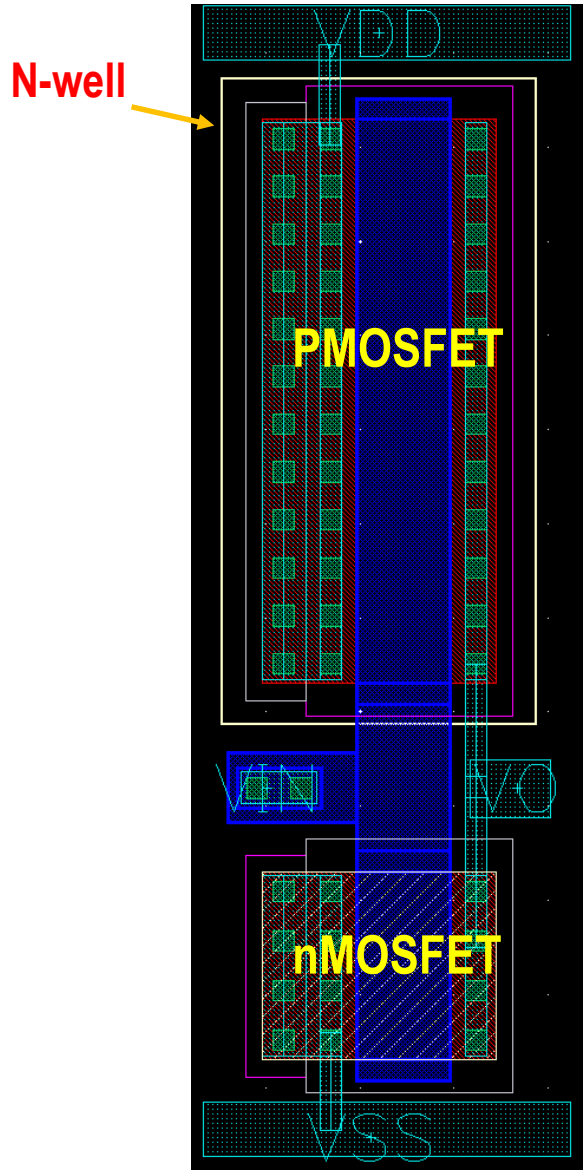
CMOS Inverter







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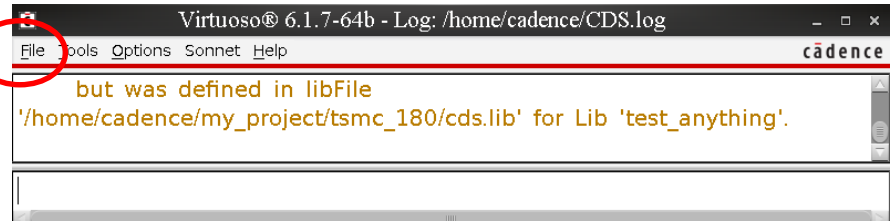
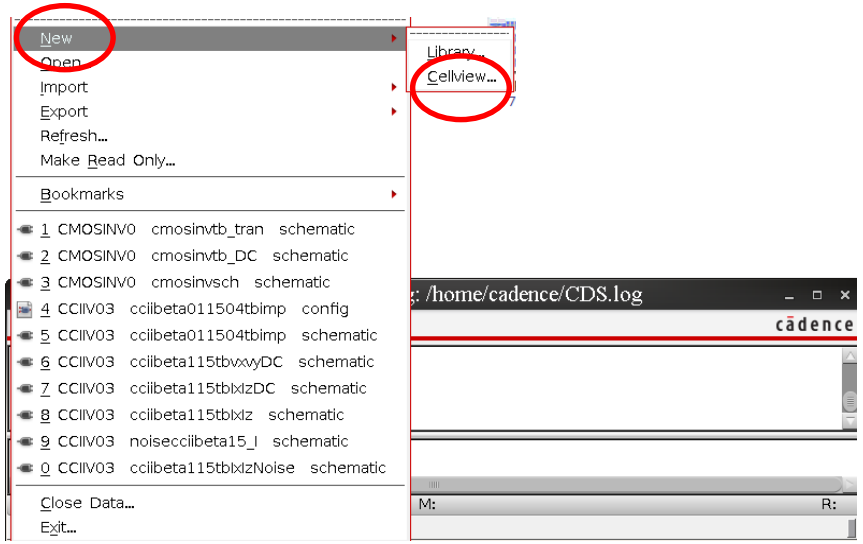
Layout Editor (1/6)

- Open a terminal and write “virtuoso &”

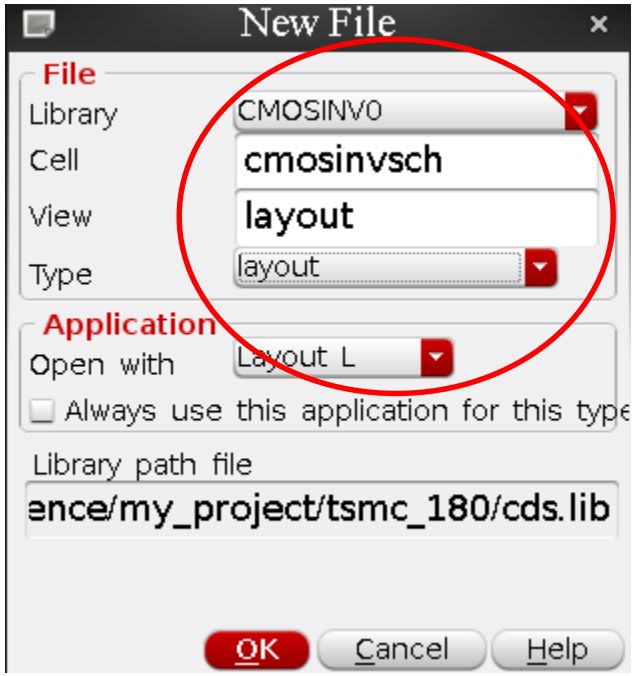
- Select “File”



- From new →cell view

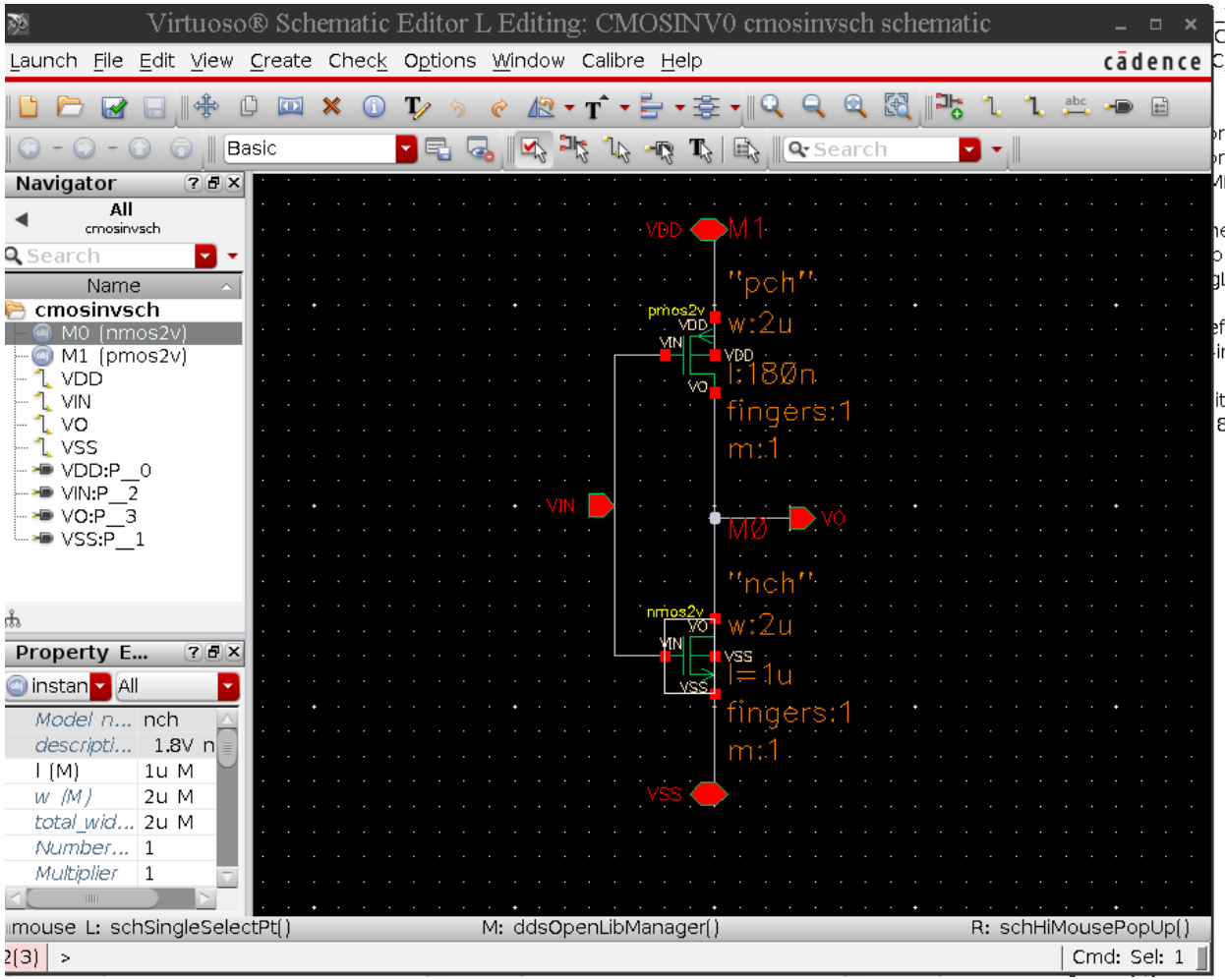


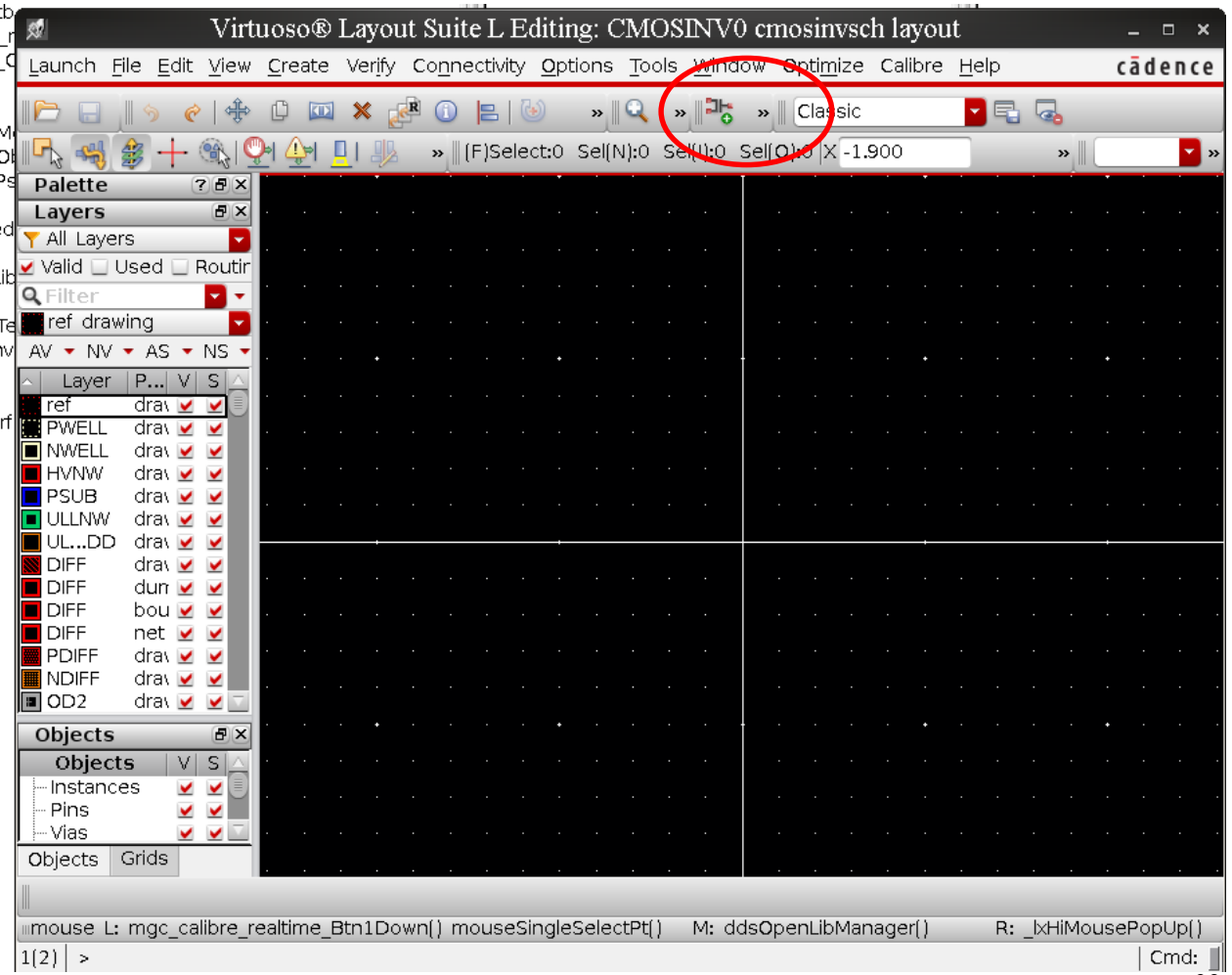
- Cellname is similar to the schematic name but the view and type will be layout



Layout Editor (2/6)

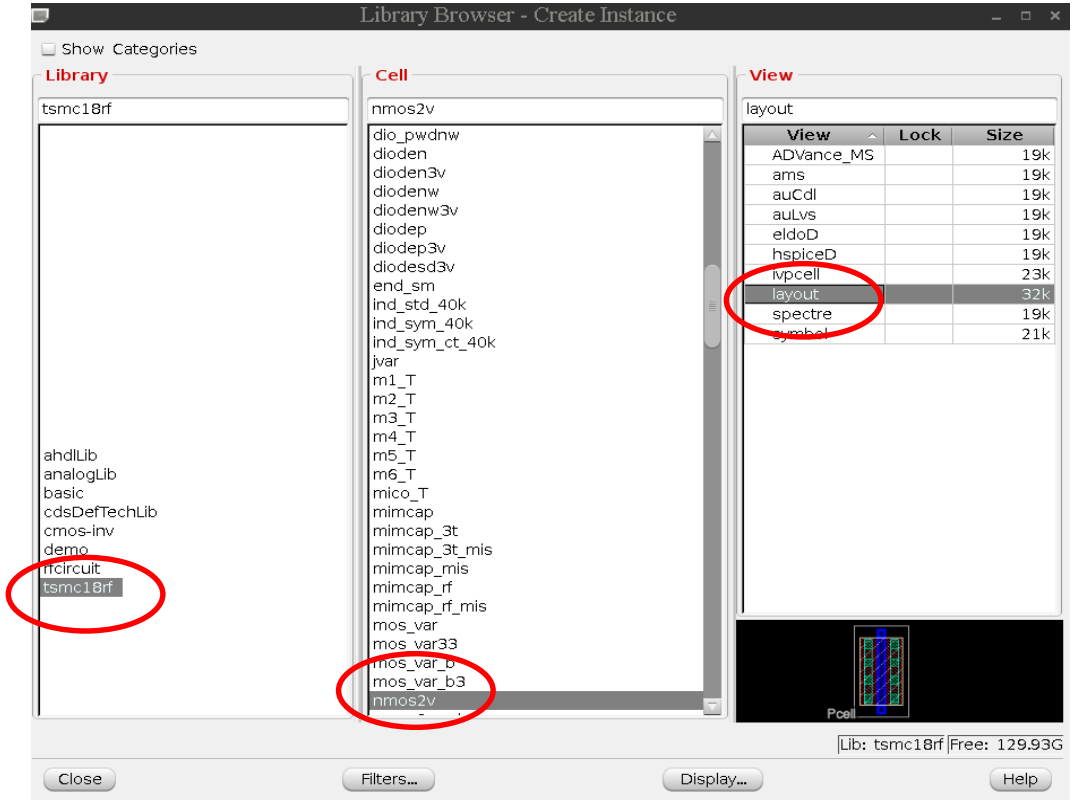
- Open both schematic and layout cellviews
- Add layout of both NMOS and PMOS



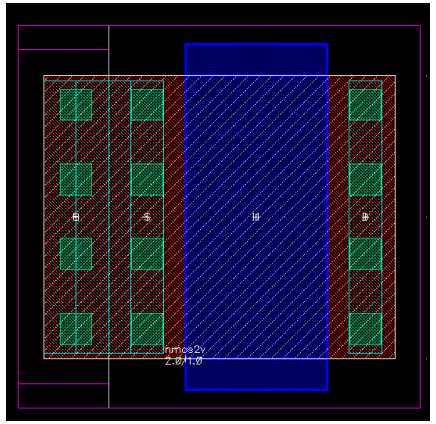


Layout Editor (3/6)

❑ Add NMOS

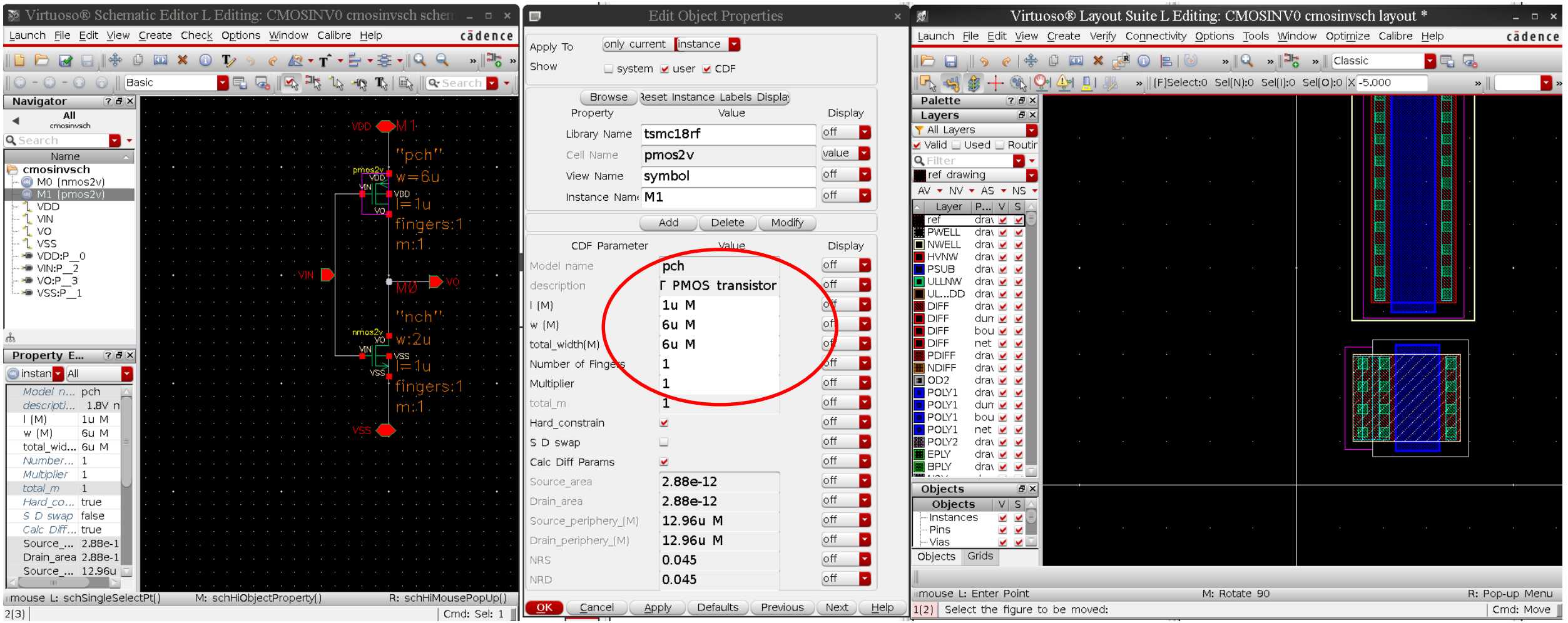


❑ Adjust dimensions of NMOS



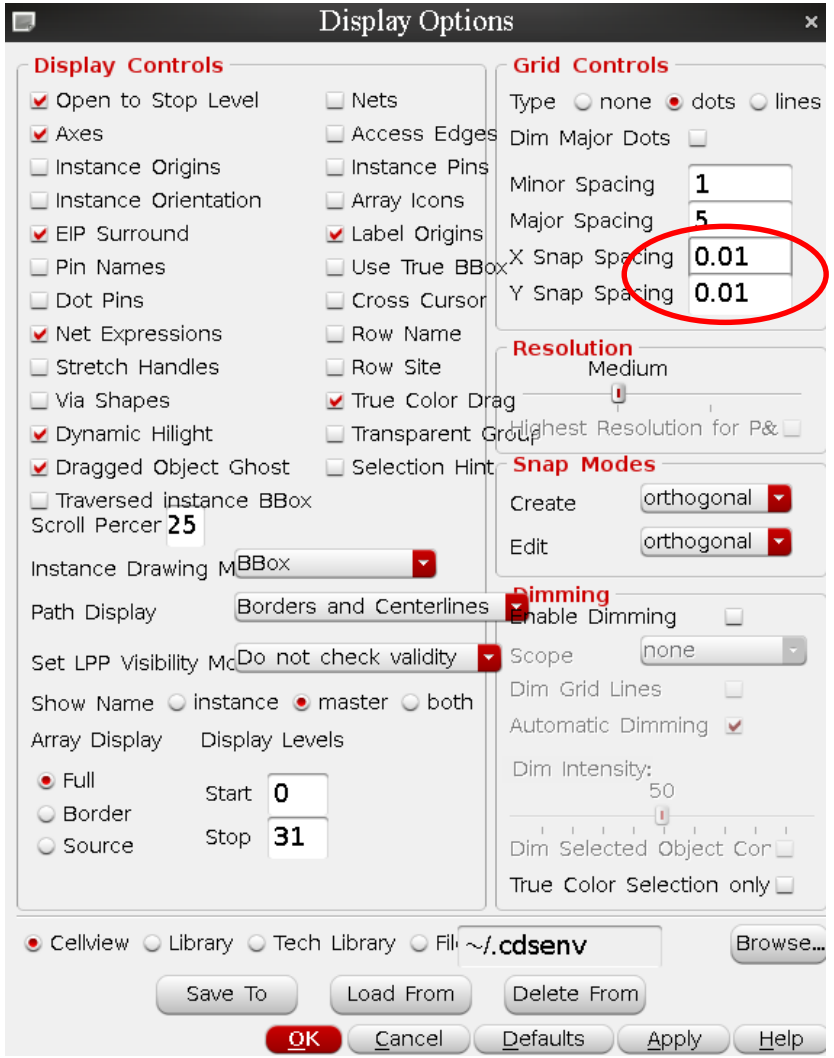
Layout Editor (4/6)

- Repeat the previous steps for PMOS

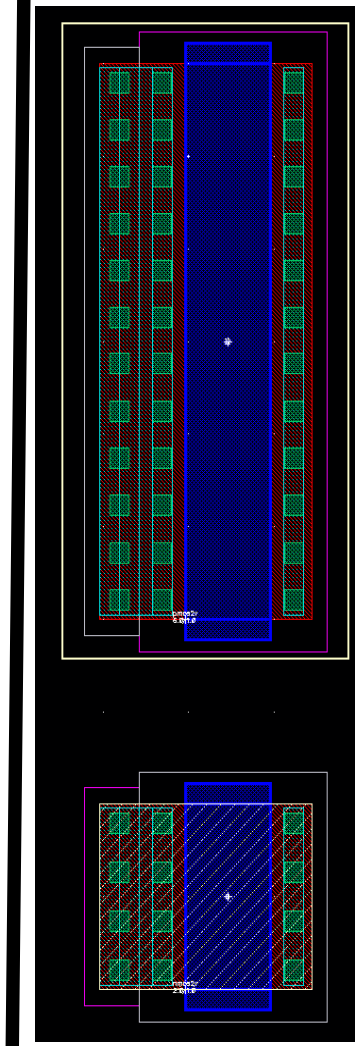


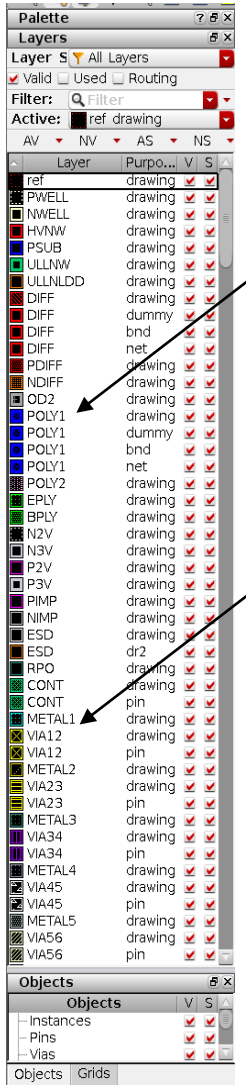
Layout Editor (5/6)

- Before drawing the wiring, please adjust the X and Y snap spacing



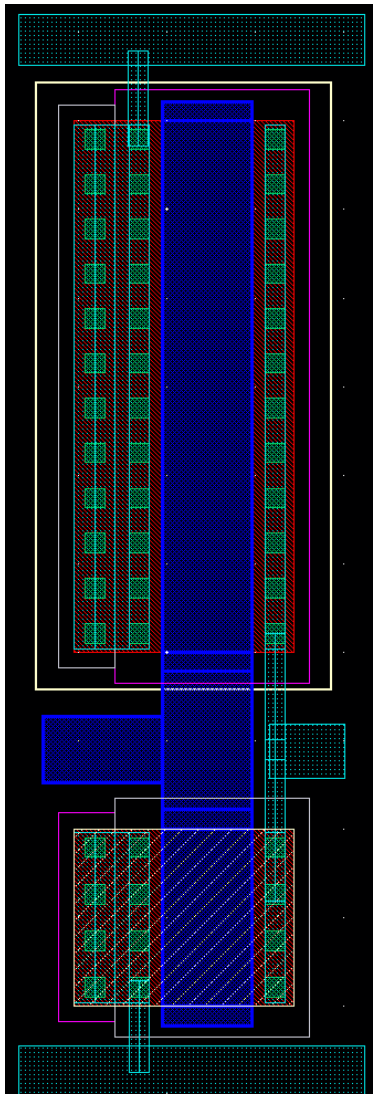
- Start to draw layout of the wiring, build rect. For both VDD (UPPER) and VSS (Botton)





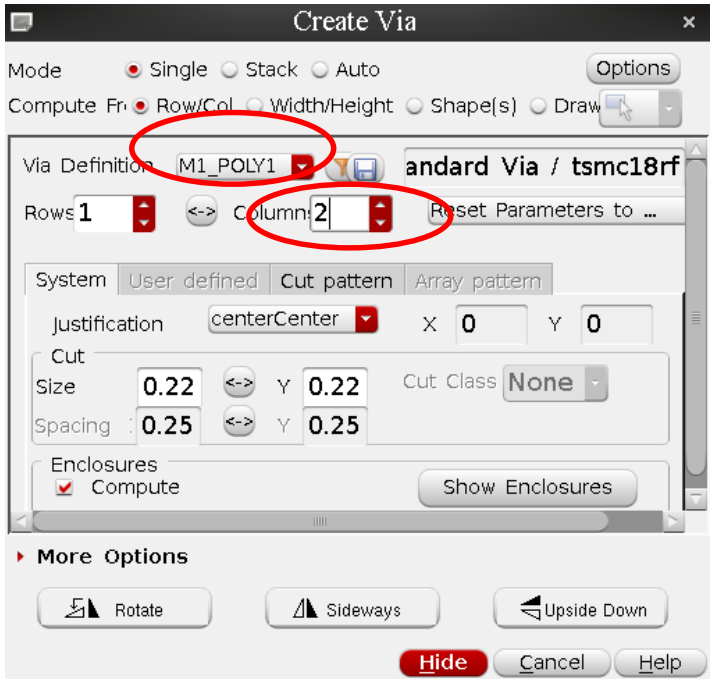
POLY1 (drawing)

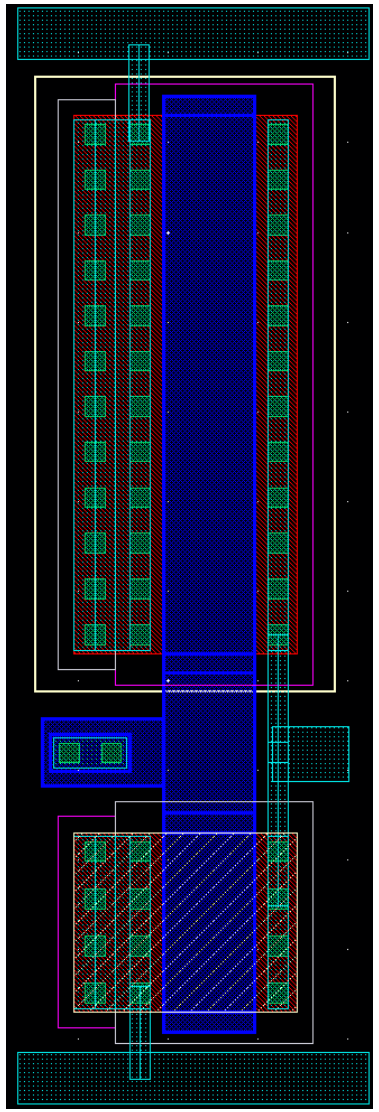
METAL1 (drawing)



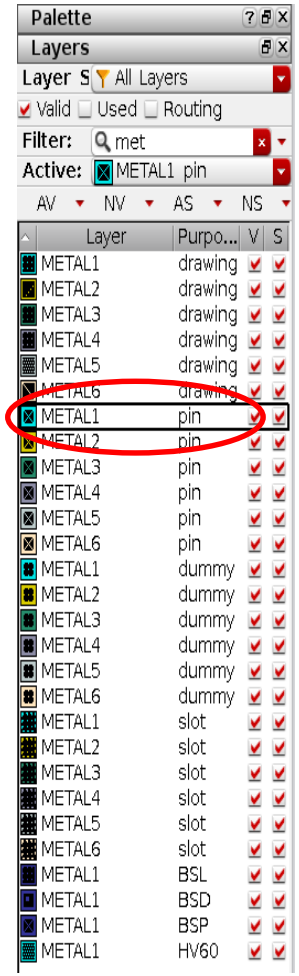
Layout Editor (6/6)

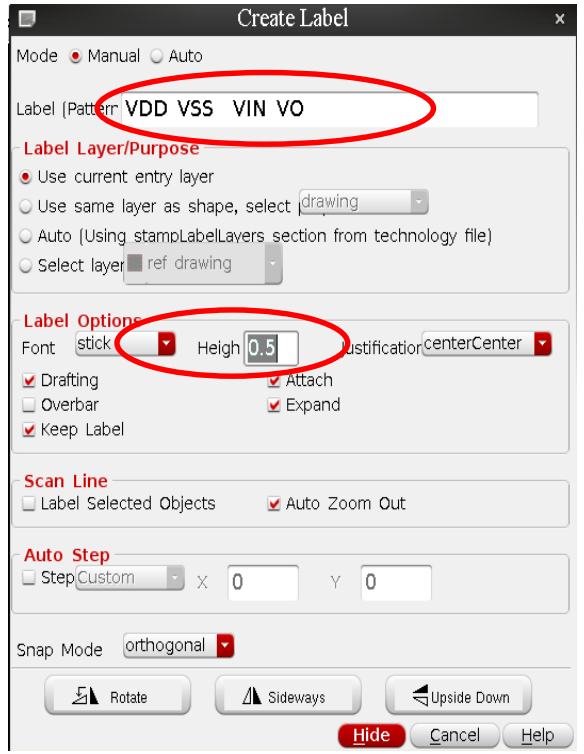
- Create Via on the POLY (M1-POLY1) using hot key “v”,
- Adjust # via >2

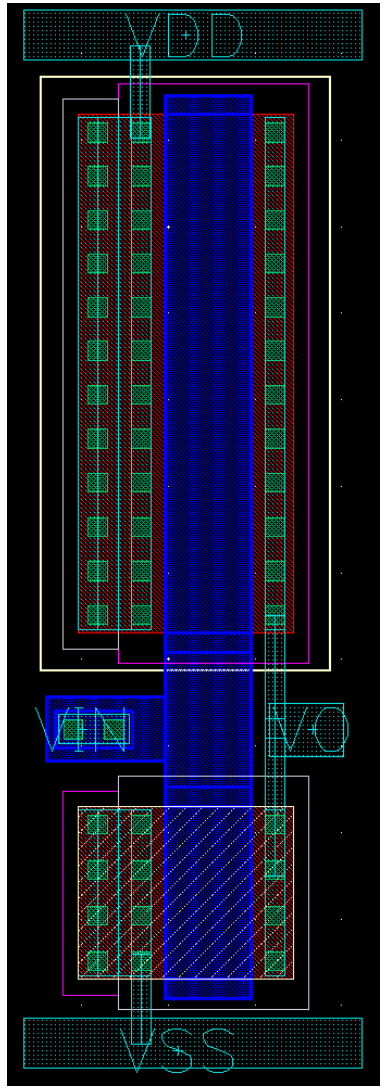




- To add the pins, please select METAL1 as pin. Then, create labels.







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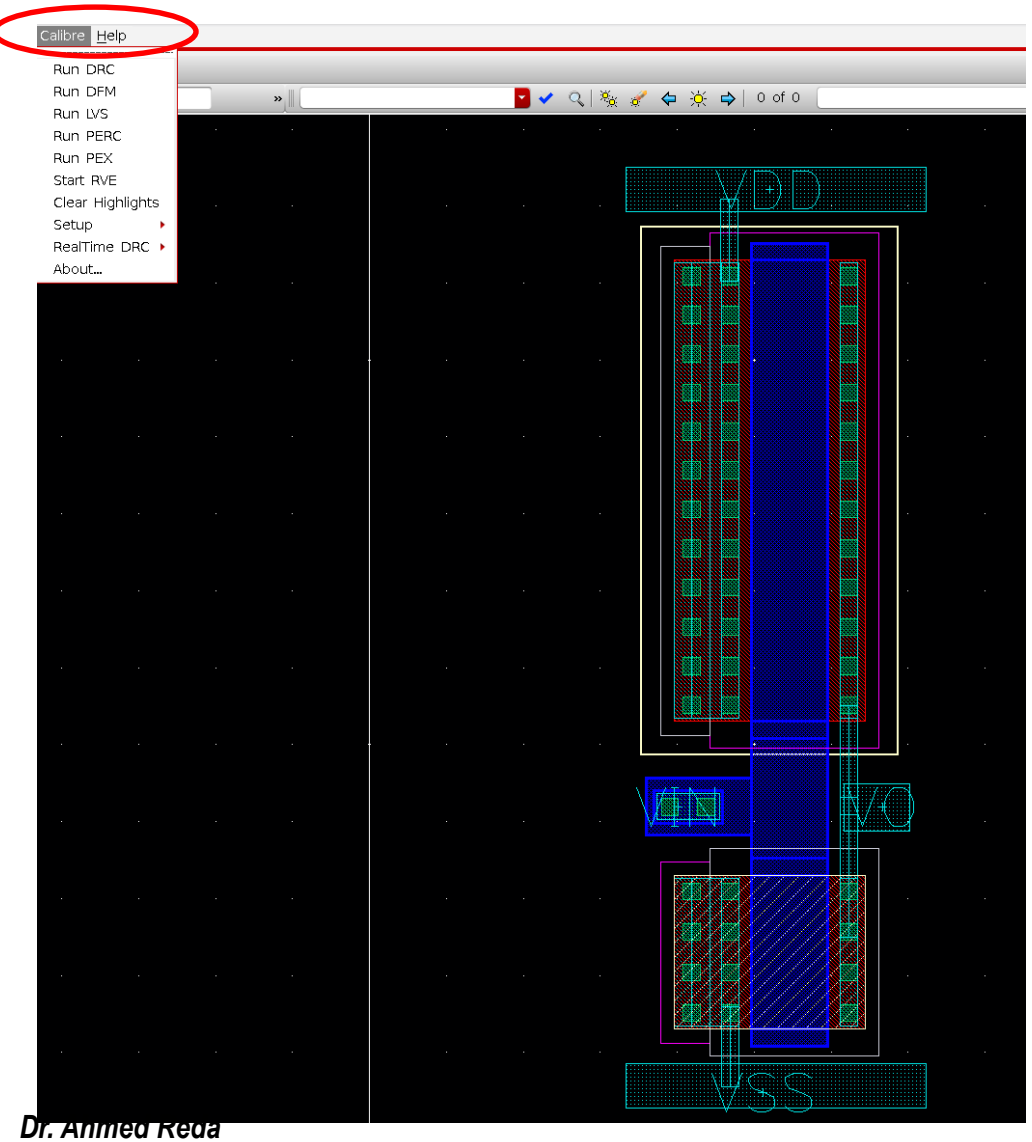
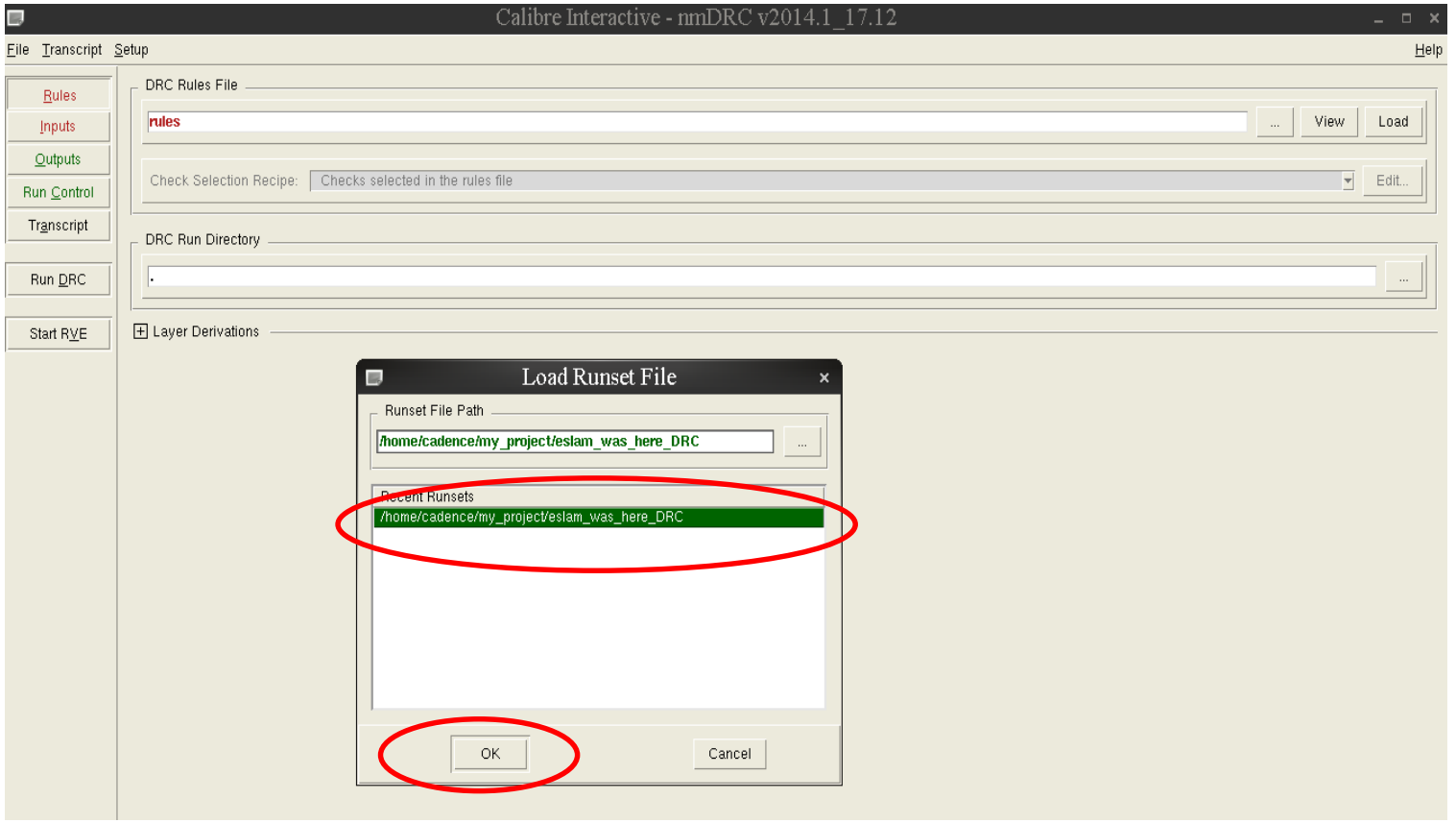
DRC(1/3)

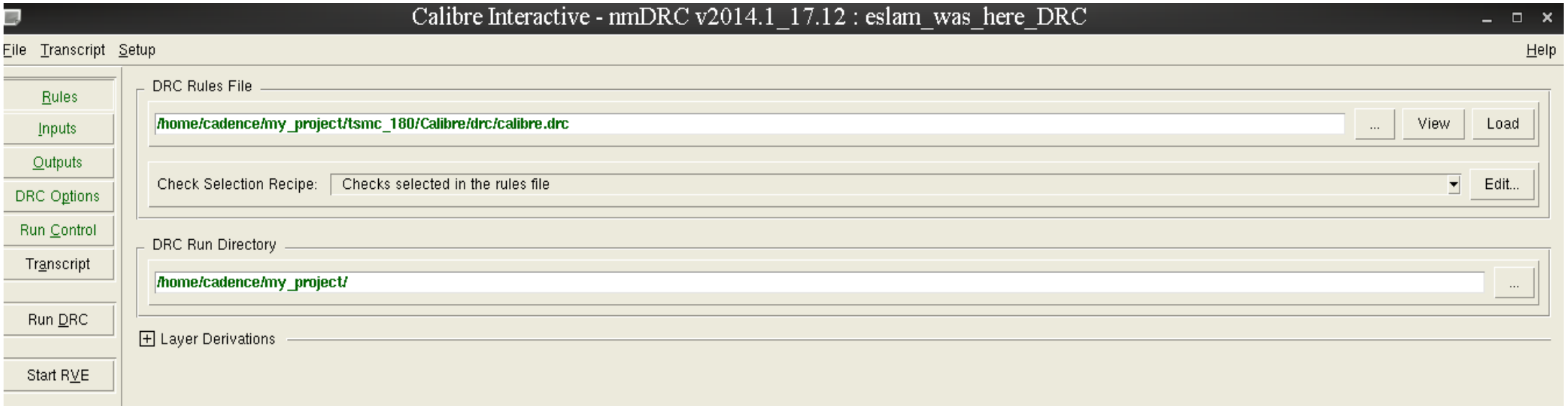
- From caliber, select Run DRC

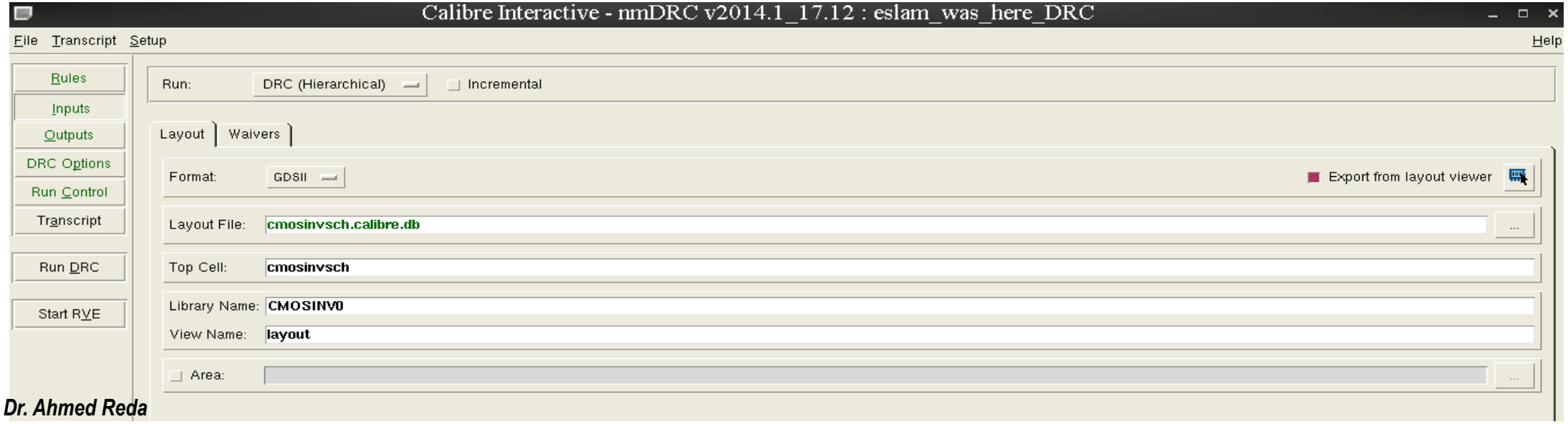




DRC(2/3)

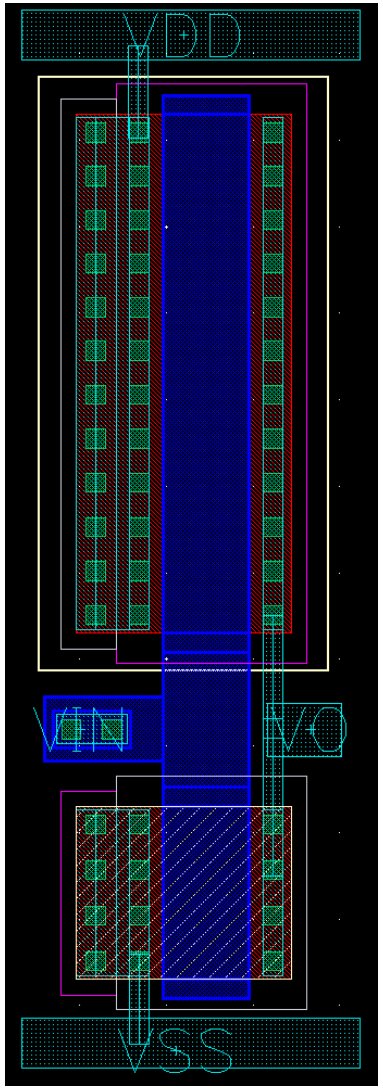
- Make sure the paths



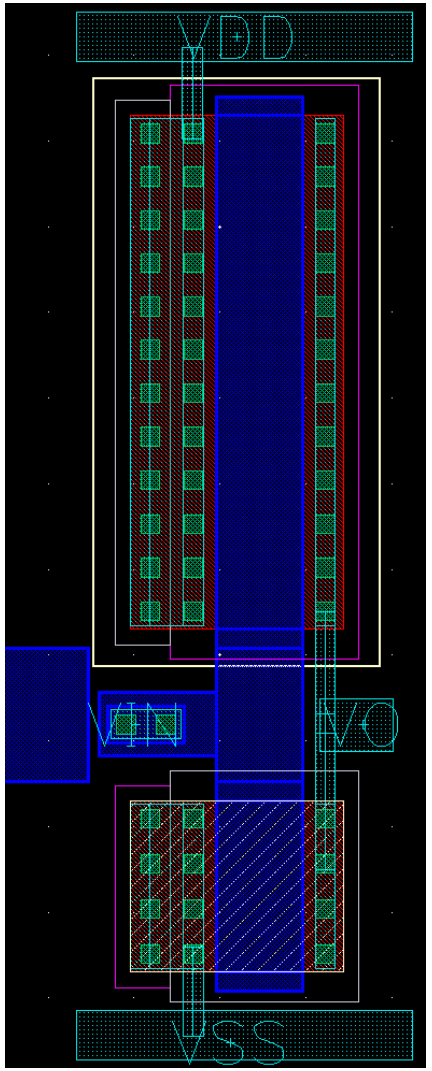


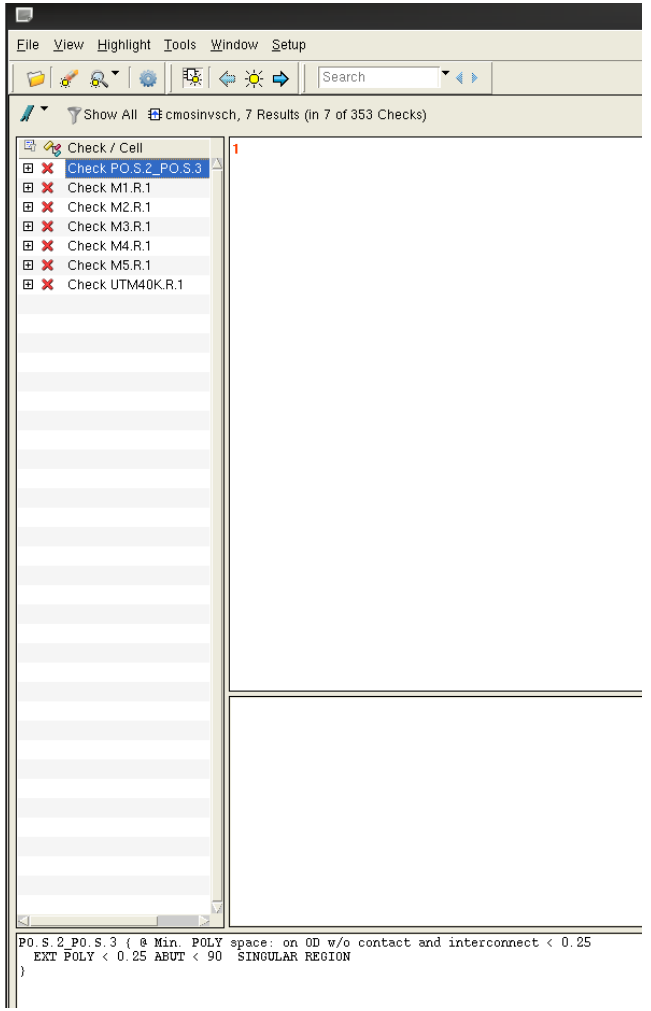
DRC(3/3)

- Make sure errors are only for density



- Example of an error as min. space



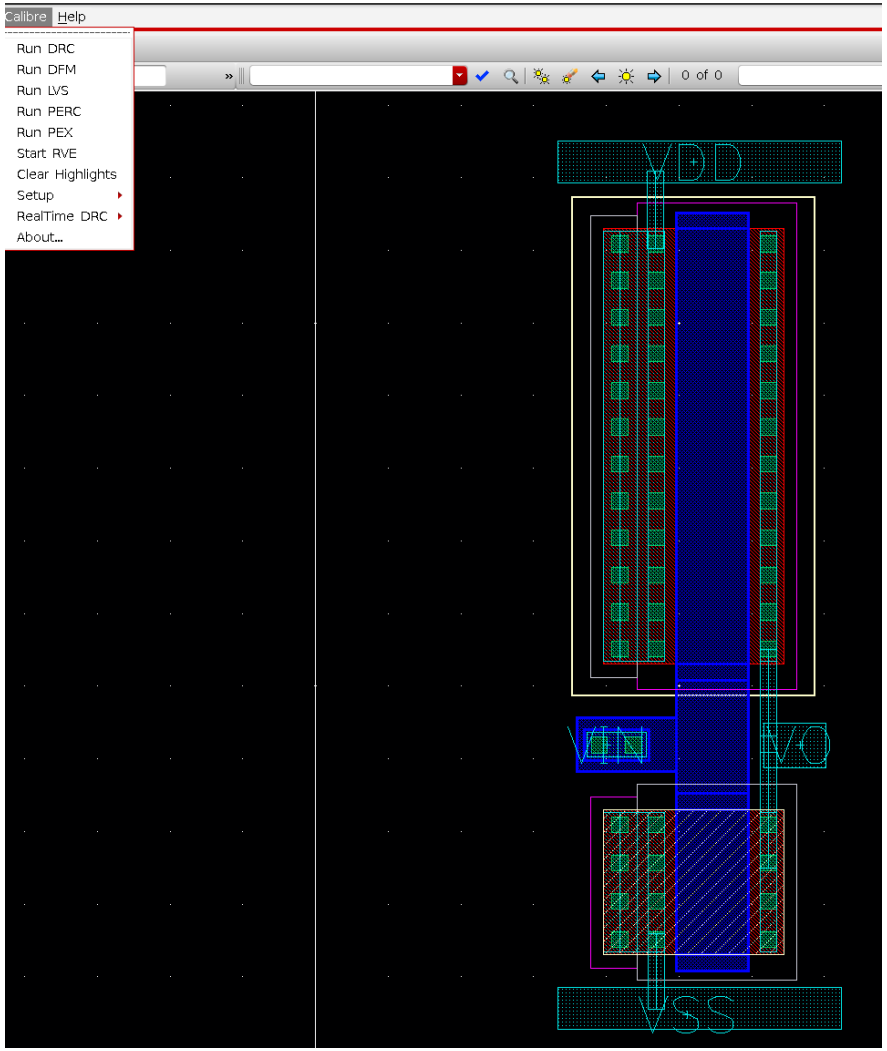


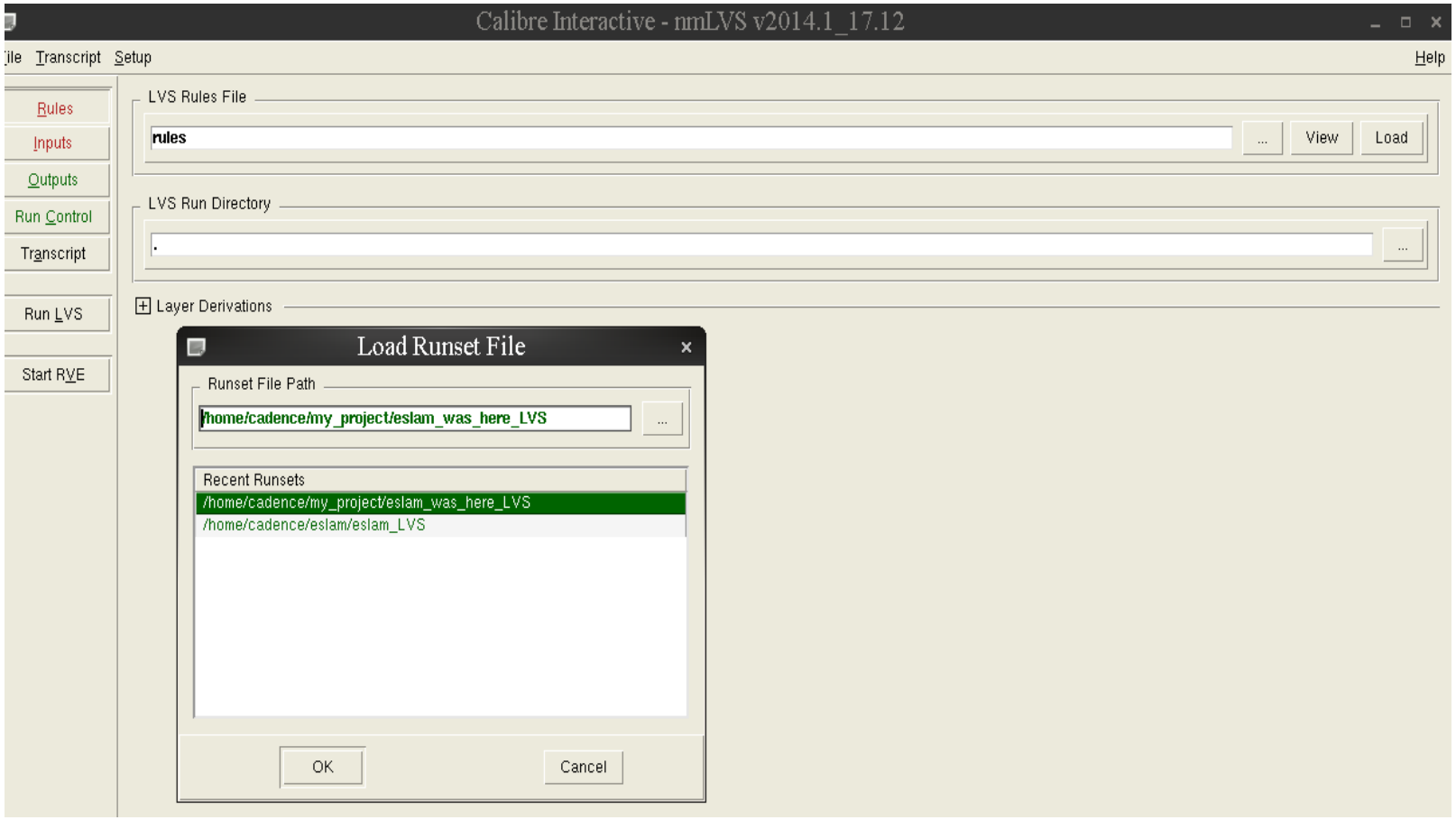
Outlines

- Living in a 3D World
- Design Rules Check
- MOSFET Layout
- CMOS Inverter
  - Layout Editor
  - DRC
  - LVS
- Cadence Hot Keys
- Discussion

LVS (1/3)

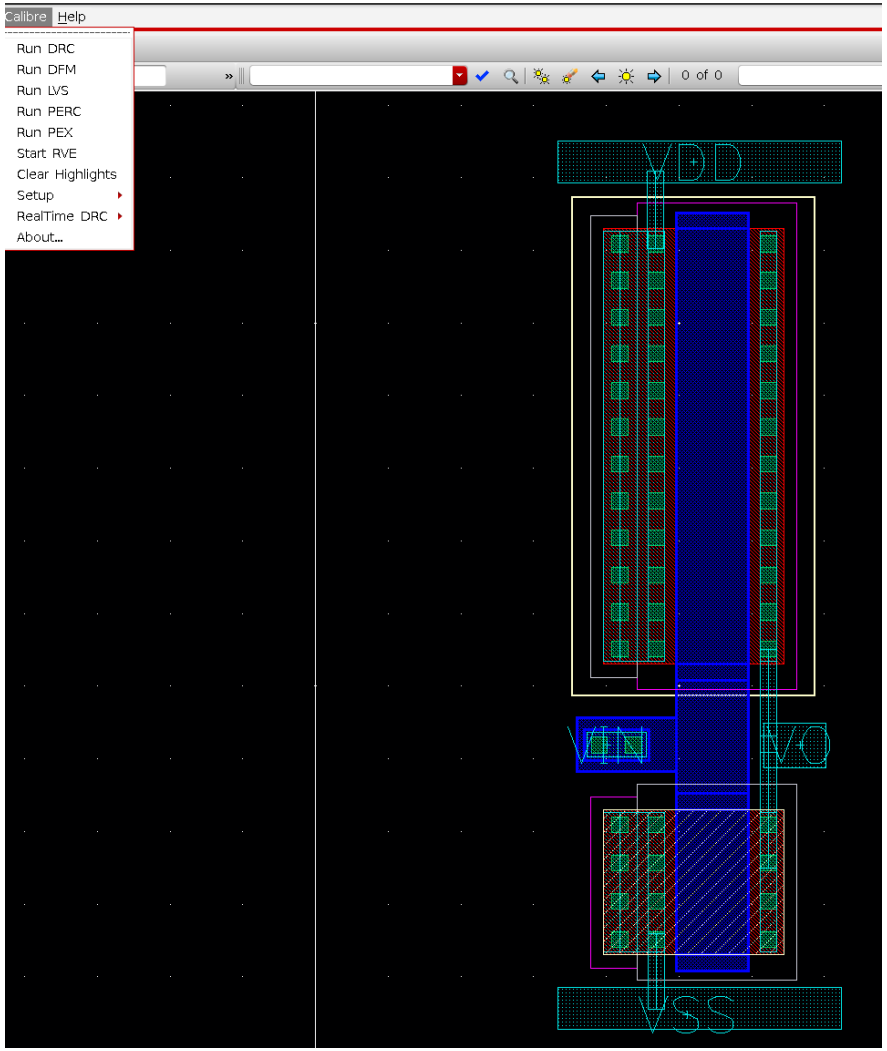
- From caliber, select Run LVS

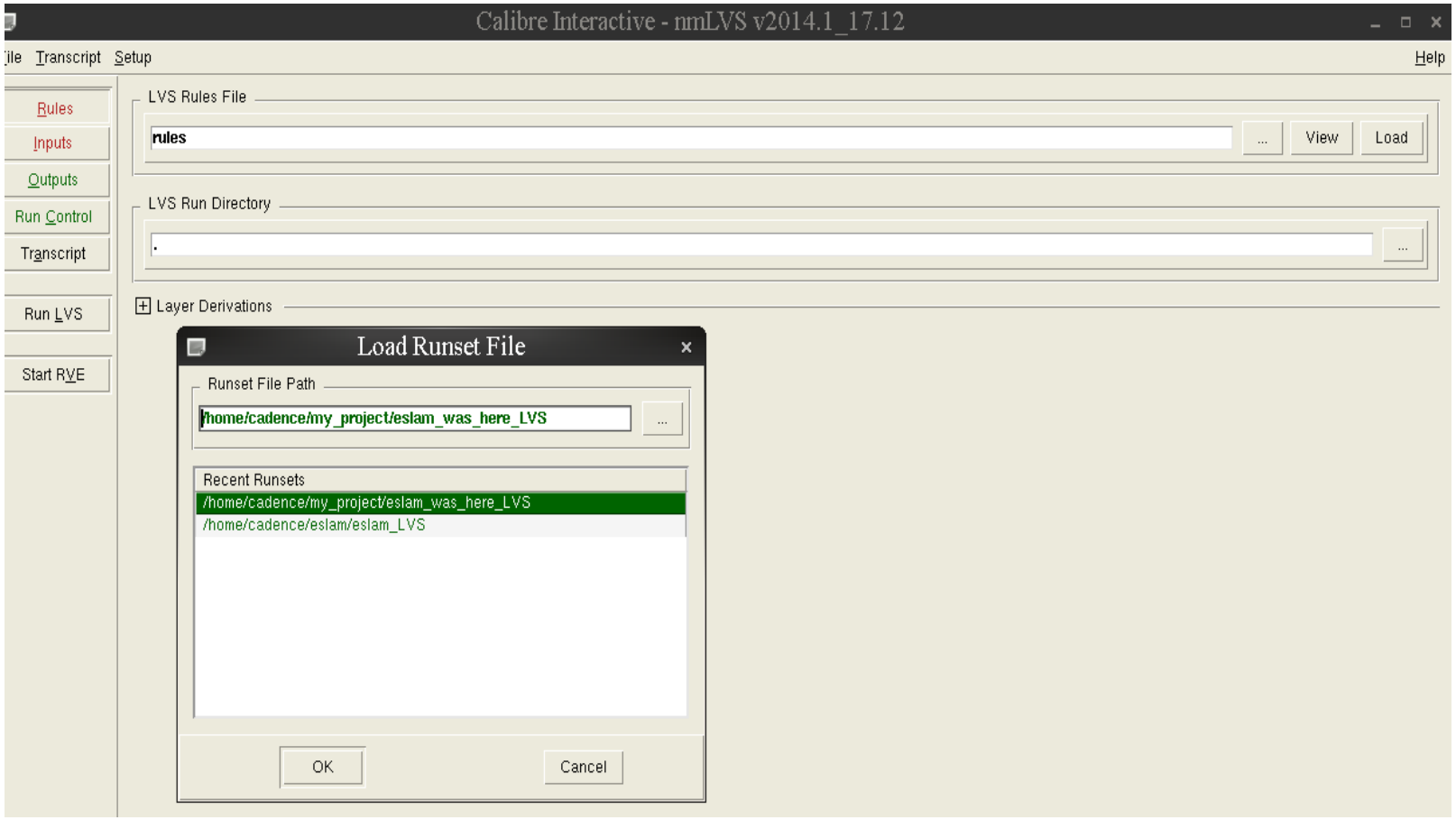




LVS (2/3)

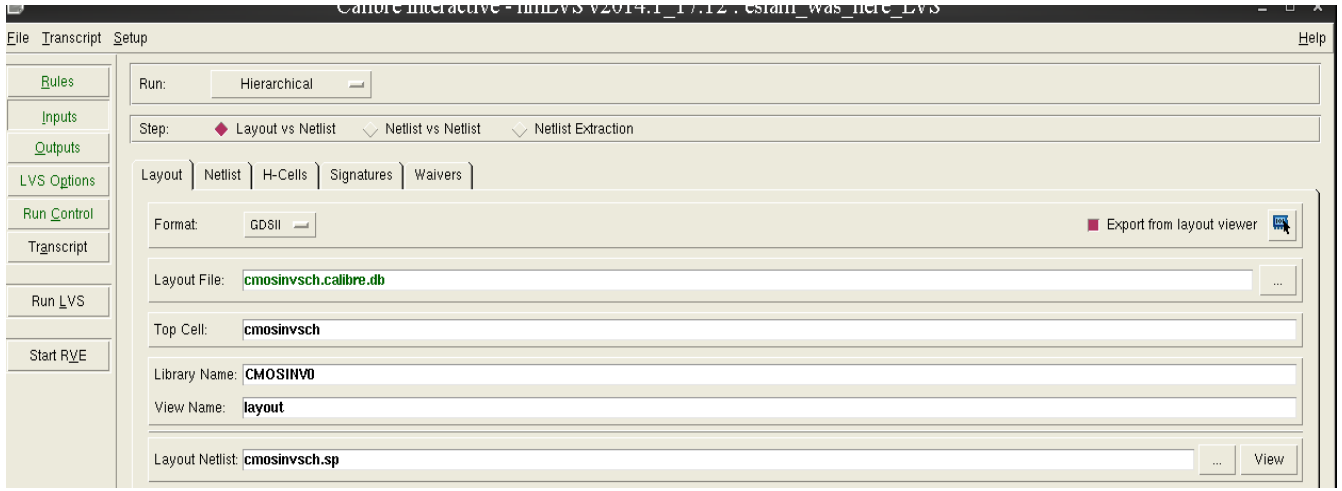
- From caliber, select Run LVS

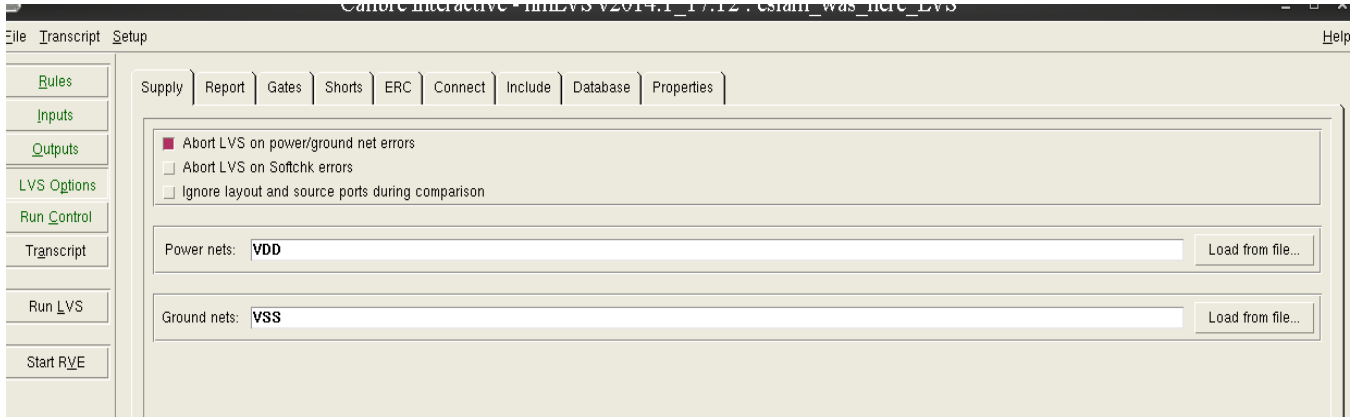


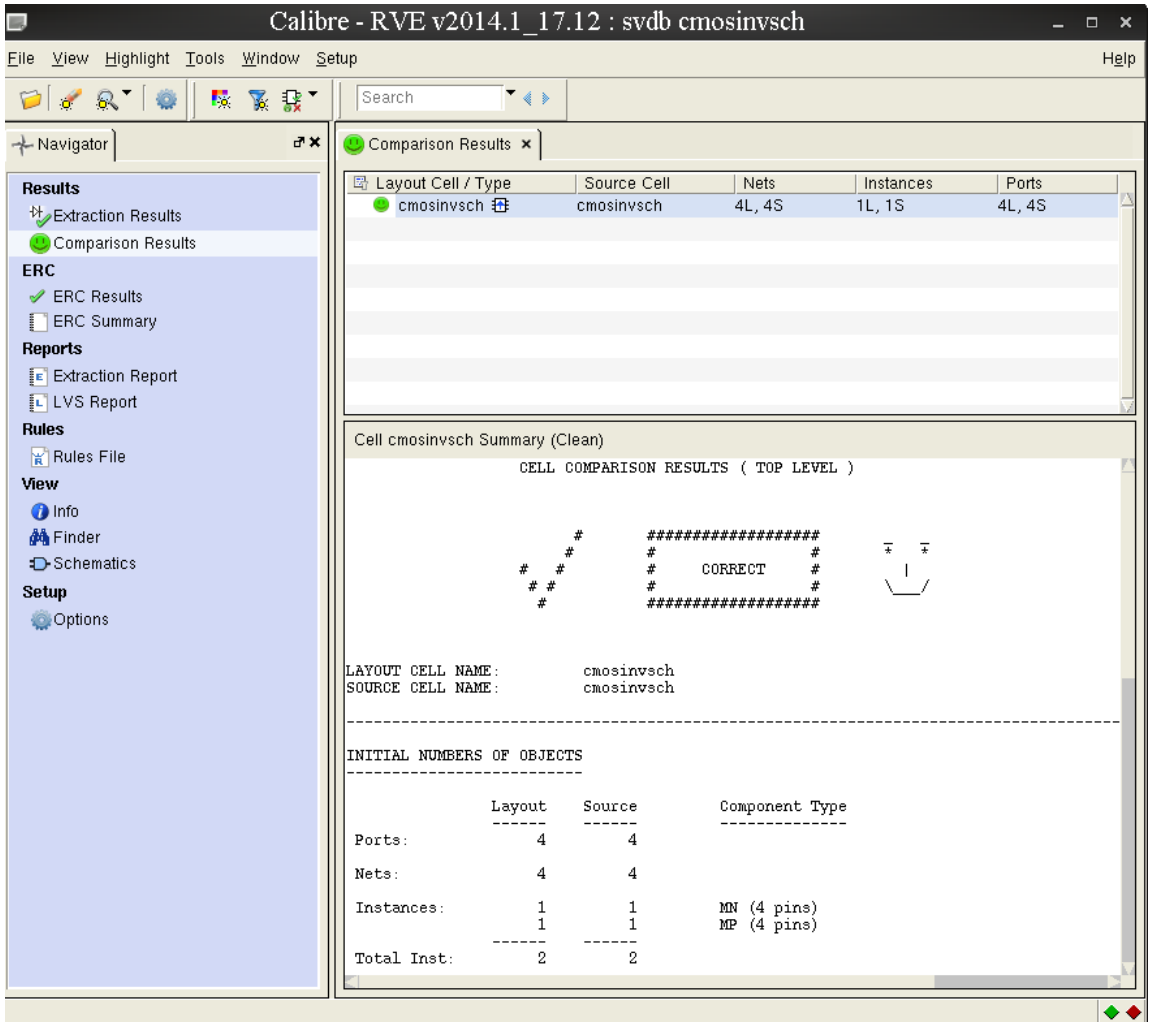


LVS (3/3)

- Open a terminal and write “virtuoso &”







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Cadence Hot Keys

Frequently used for Layout Editor

f	fit
shift-f	in hierarchical layout show all levels as if flat
ctrl-f	hide all hierarchy and show only outline of instances
r	rectangle
q	property of an object
ctrl-z/shift-z	*zoom in/zoom out*
p	*path*: makes a min width path of the layer selected in LSW
ctrl-a/ ctrl-d	select all/deselect all
c	*copy*
m	*move*: move a whole rectangle
s	*stretch*: can stretch just a side of a rectangle
k	ruler
i	add an instance
u/shift-U	*Undo/redo*
e	display options like grid size, snap size etc
f6	redraw
shift-c	*chop*: chop a rectangle, i.e., reduce its size

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Discussion

Thanks!