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King Fahd University of Petroleum & Minerals

# Schematic Design and Simulation (IC Design Flow)

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# Outlines

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- Objective
- CMOS Inverter
- Schematic Editor
- Create Symbol
- Testbench
- Cadence Hot Keys
- Discussion

# Outlines

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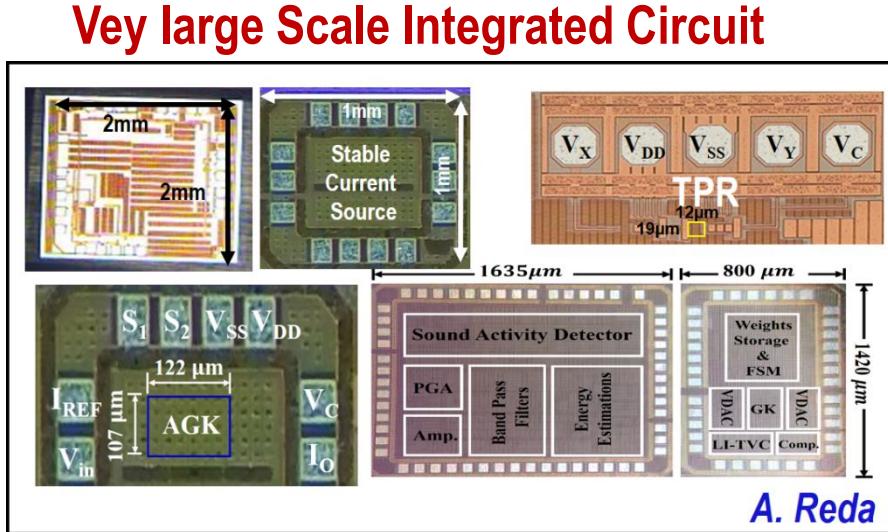
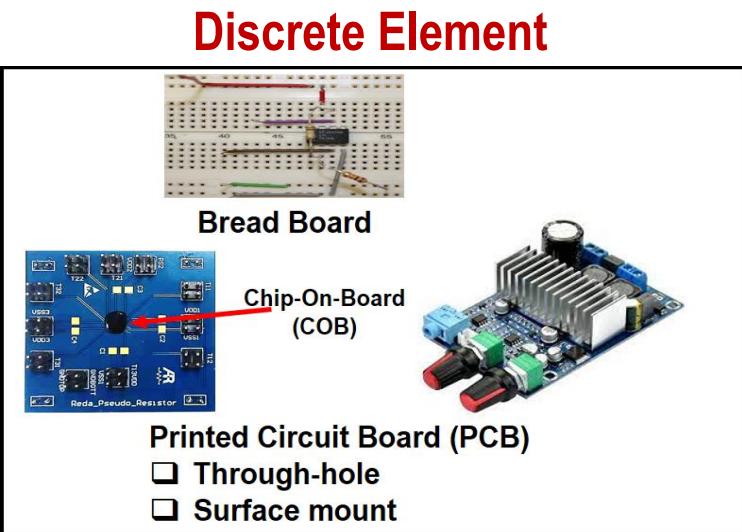


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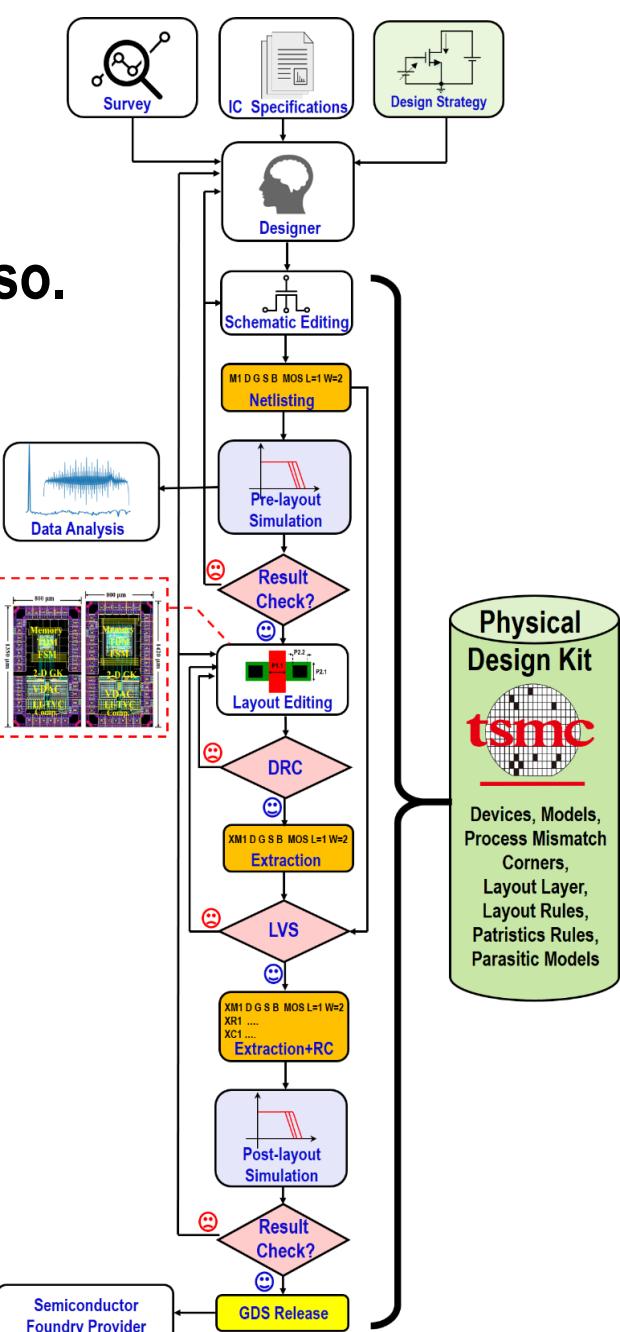
# Objective (1/2)

## □ Objective

- Create a schematic and symbol for a CMOS inverter in Cadence Virtuoso.
- Perform simulations for the inverter



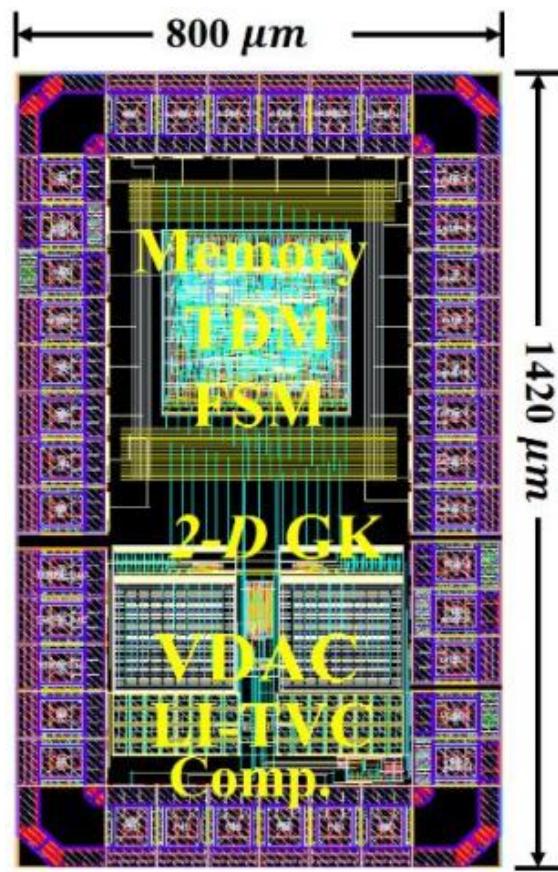
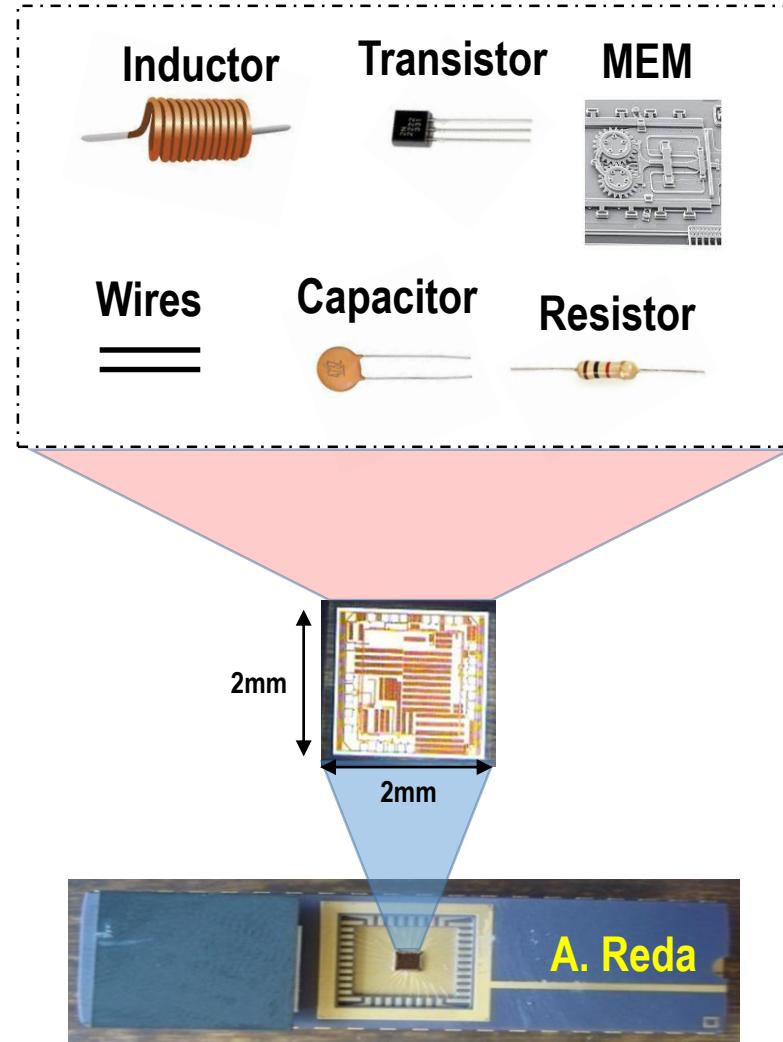
Item	Discrete Element	Very large scale Integrated Circuit
Area	Large	Small
Configuration	Easy	Complex
Price	Cheap	Expensive
Applications	Small production	Mass production
Power consumption	High	Low



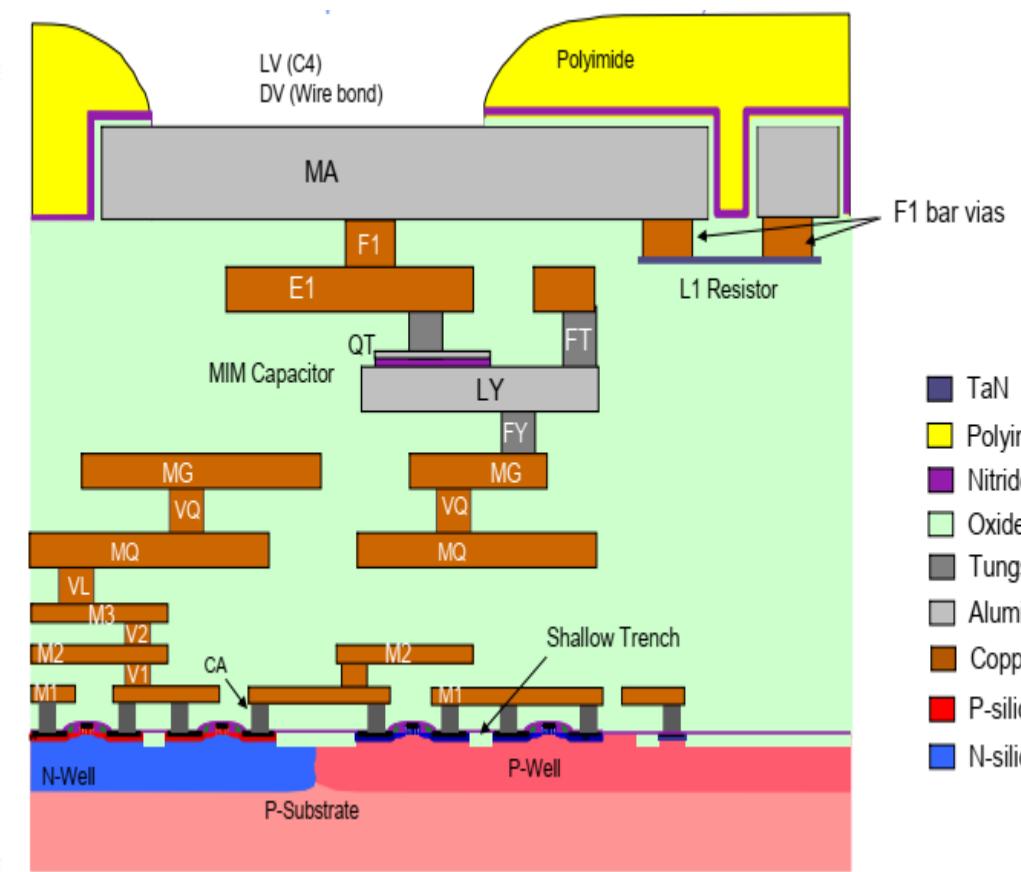
# Objective (2/2)



- An **integrated circuit (IC)** is a set of electronic circuits on one small flat piece (or "chip") of semiconductor material, usually silicon.



Layout using CAD tool



Process Cross-Section  
8 layers

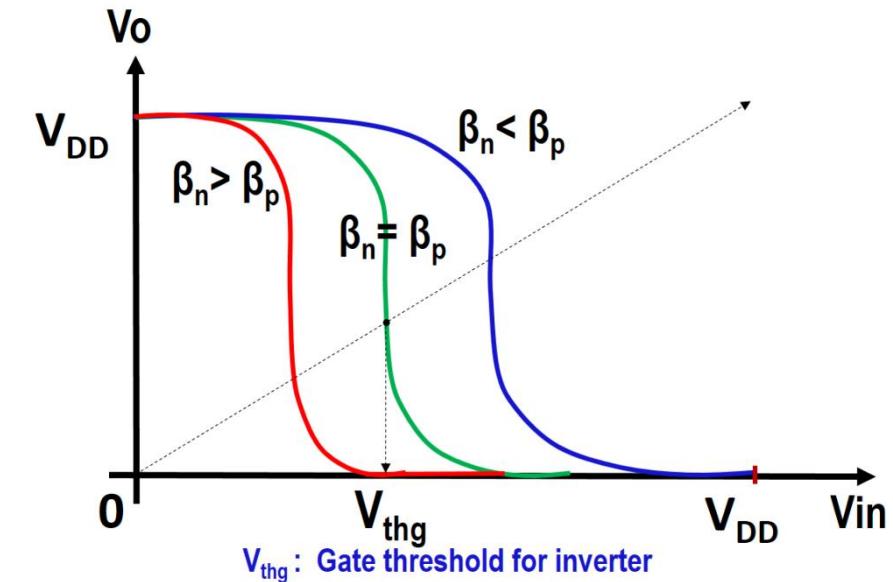
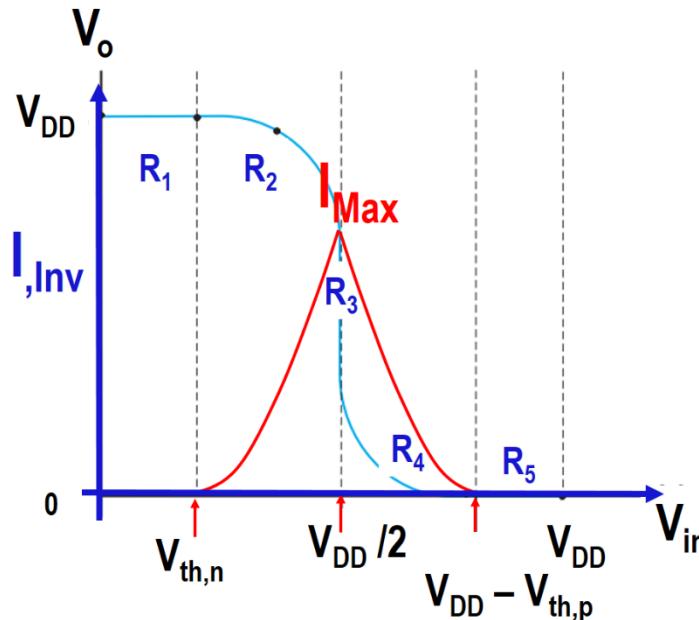
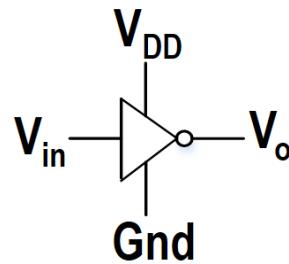
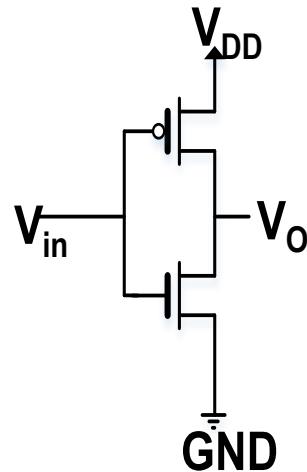
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# CMOS Inverter (1/2)



$$B_n = \mu_n C_{ox} \frac{W_n}{L_n}$$

$B_n$ : Gain process factor of n-MOSFET  
 $\mu_n$ : Mobility of Electron  
 $C_{ox}$ : Gate Oxide Capacitor/unit area  
 $W_n$ : width of transistor  
 $L_n$ : length of transistor

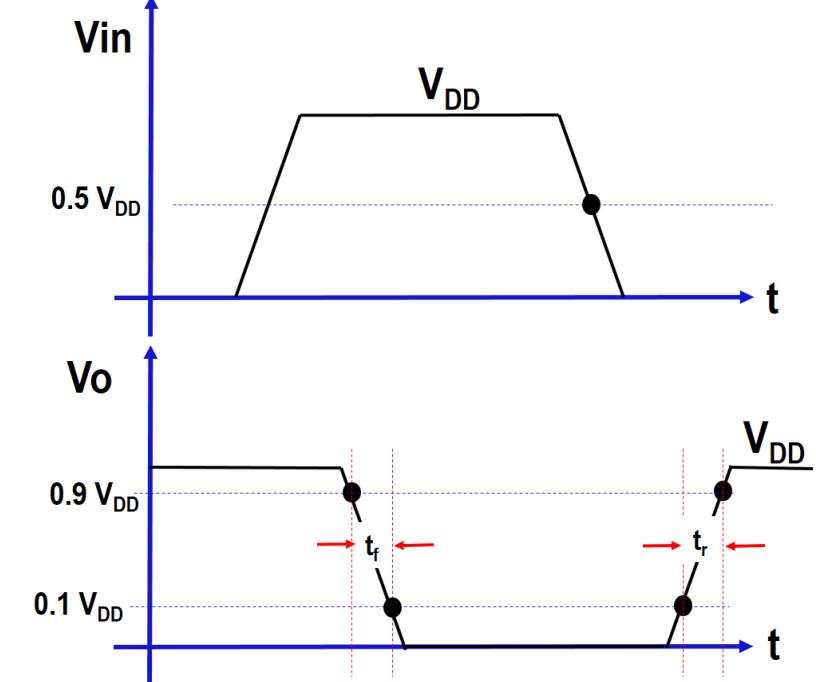
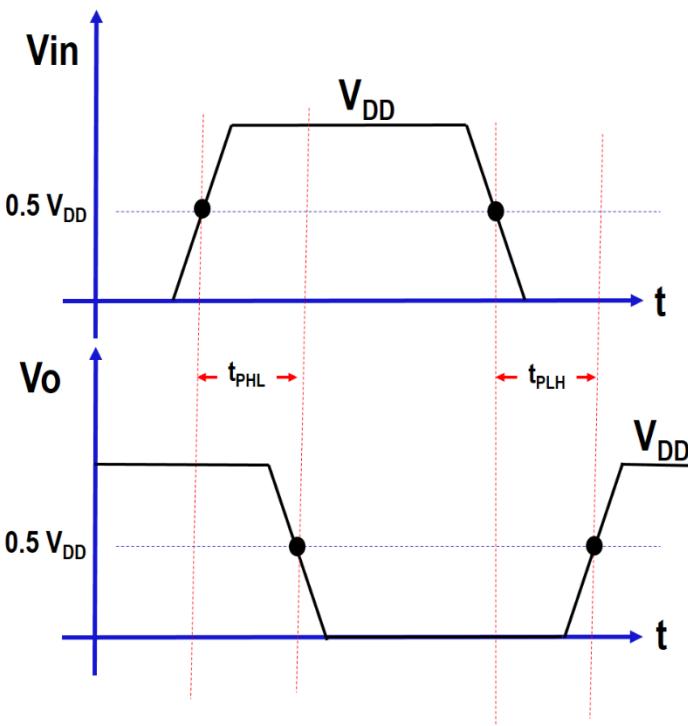
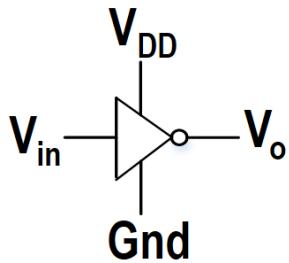
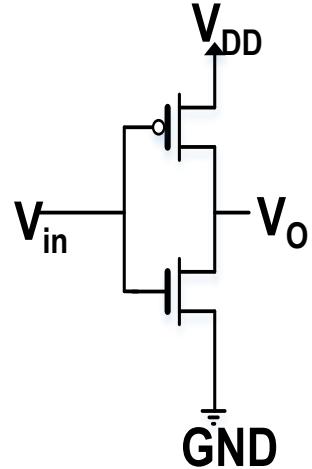
$$B_p = \mu_p C_{ox} \frac{W_p}{L_p}$$

$B_p$ : Gain process factor of p-MOSFET  
 $\mu_p$ : Mobility of Hole  
 $C_{ox}$ : Gate Oxide Capacitor/unit area  
 $W_p$ : width of transistor of p-MOSFET  
 $L_p$ : length of transistor of p-MOSFET

$$V_{thg} = \frac{V_{th,n} + r(V_{DD} + V_{th,p})}{1 + r}$$

$$\text{Where } r = \sqrt{\frac{\beta_p}{\beta_n}}$$

# CMOS Inverter (2/2)



- Propagation time ( $t_p$ ): is the time between 50 % of the input voltage to 50 % of the output.

$$t_p = \frac{(t_{PHL} + t_{PLH})}{2}$$

- $t_{PHL}$ : is the propagation time from high to low.
- $t_{PLH}$ : is the propagation time from low to high.

- Rise time ( $t_r$ ): is the time between 10% of the output voltage to 90 % of the output.

- Fall time ( $t_f$ ): is the time between 90% of the output voltage to 10% of the output

# Outlines

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- Objective
- CMOS Inverter
- **Schematic Editor**
- Create Symbol
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# Schematic Editor (1/4)



- Open a terminal and write “virtuoso &”

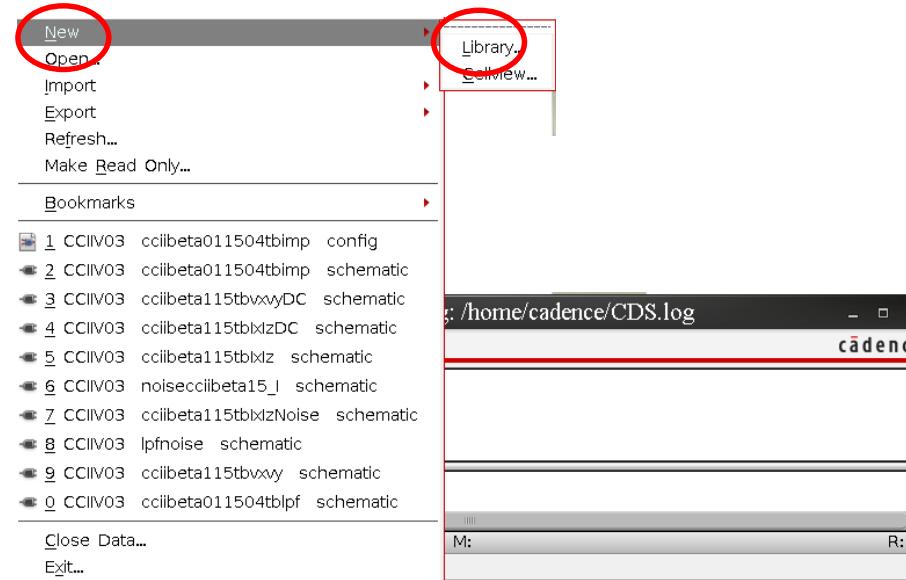


```
cadence@berkeley:~/my_project/tsmc_180
File Edit View Search Terminal Help
cadence@berkeley:~/my_project/tsmc_180$ virtuoso &
[1] 1503
```

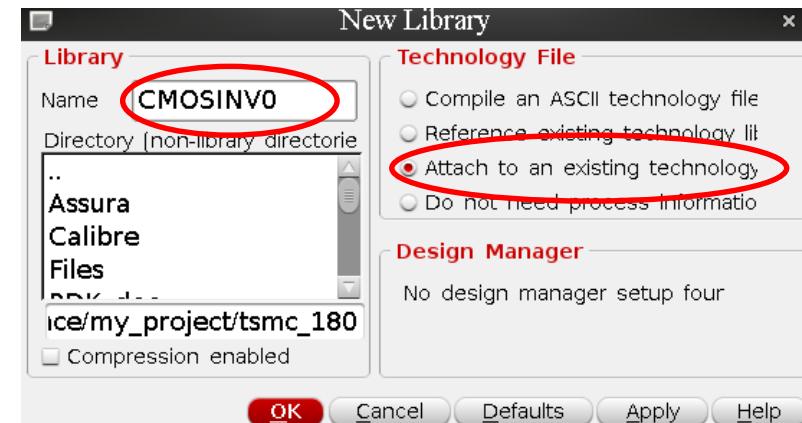
- Select “File”



- From new → library



- Write library’s name and select “attach to an existing technology”



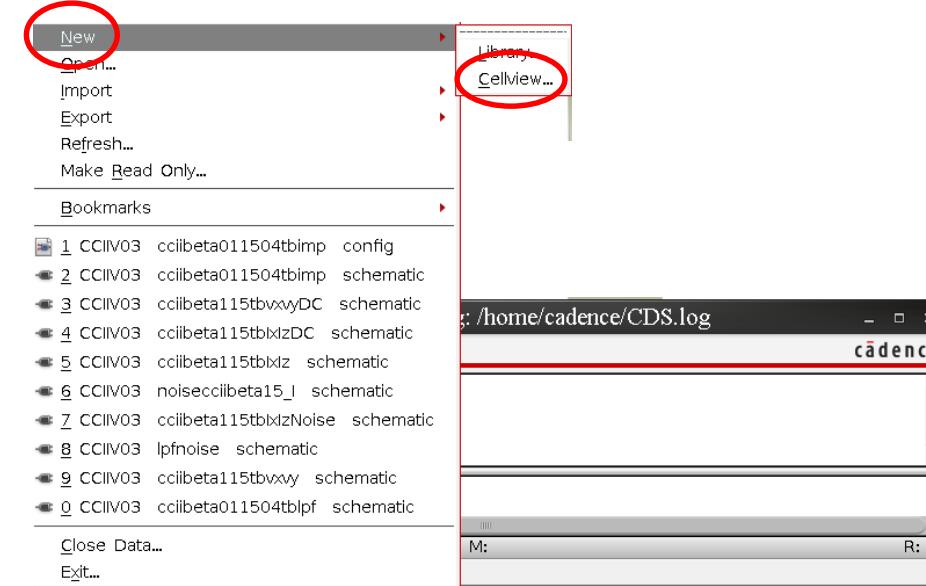
- Then, select technology library “tsmc18rf”, and press “OK”



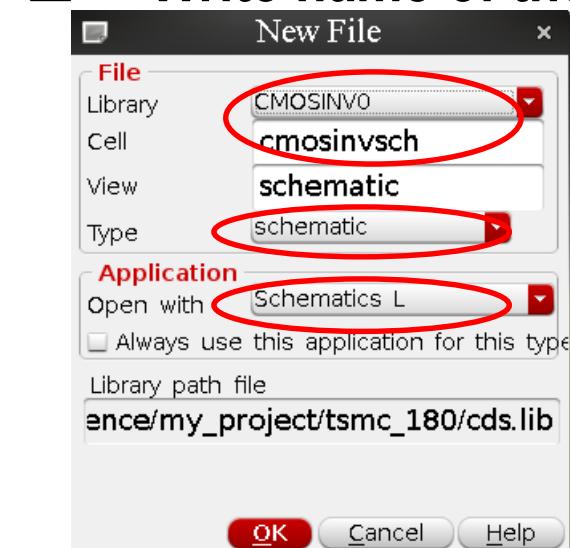
# Schematic Editor (2/4)



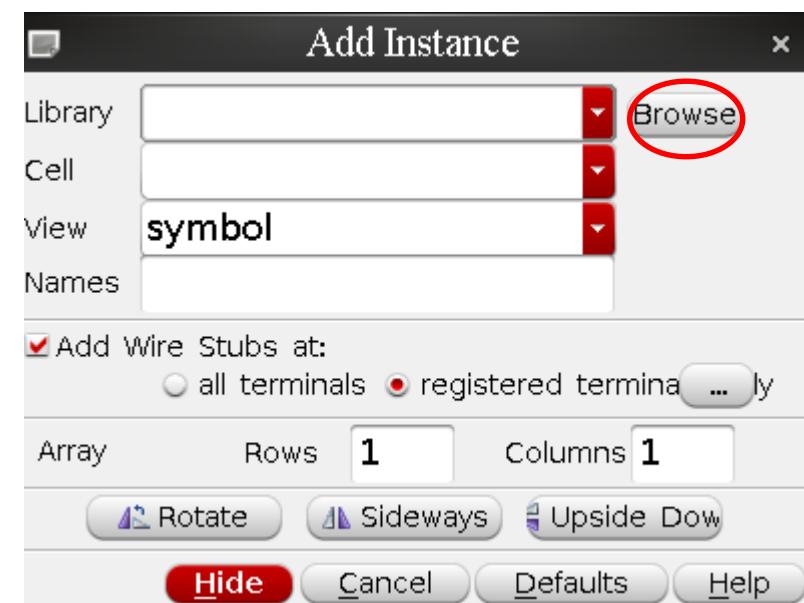
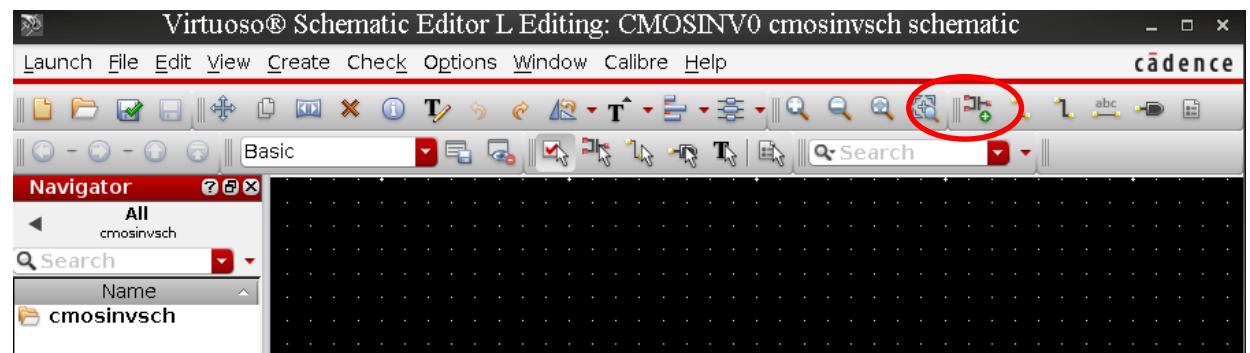
## From File→ new→ Cellview



## Write name of the cell



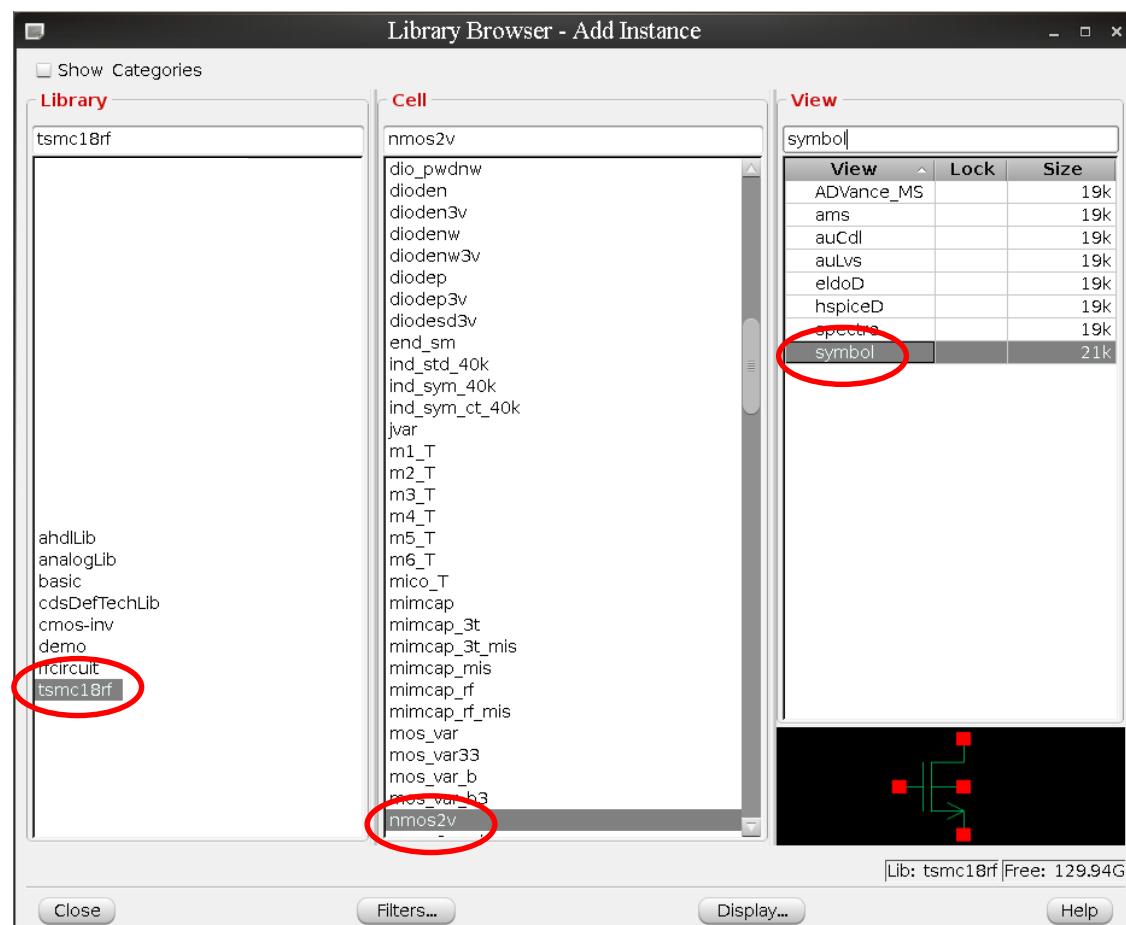
## Then, start to add the instances (MOSFET)



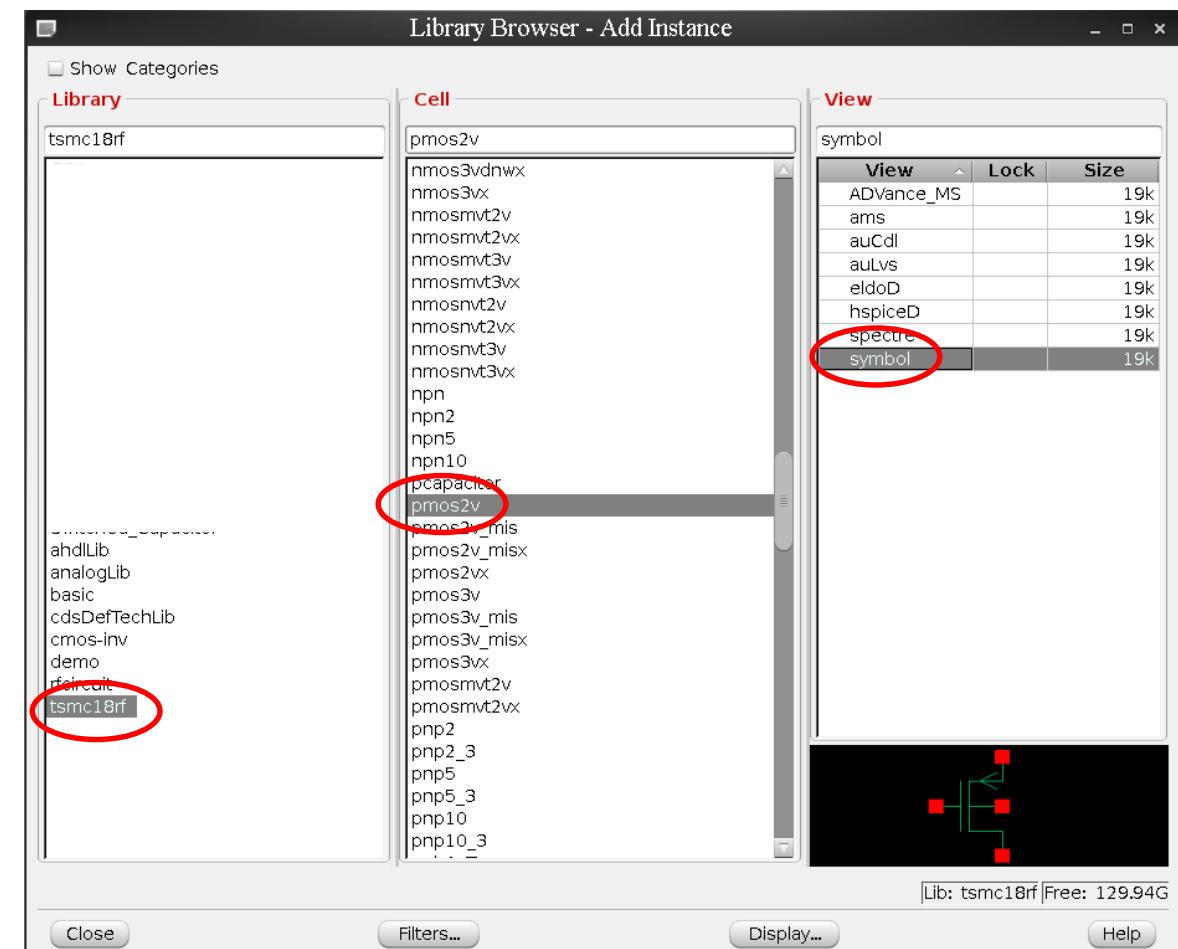
# Schematic Editor (3/4)



## □ Select tsmc18rf → nmos2v → symbol



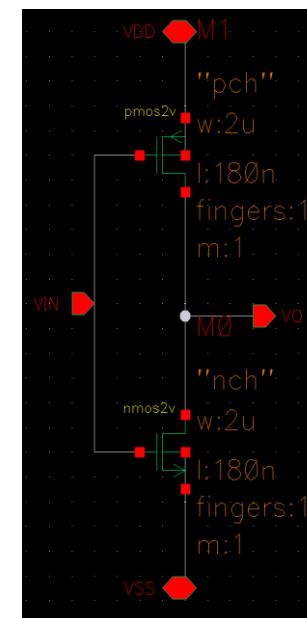
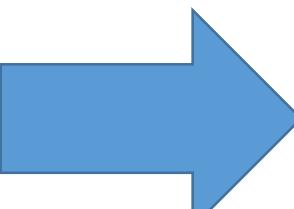
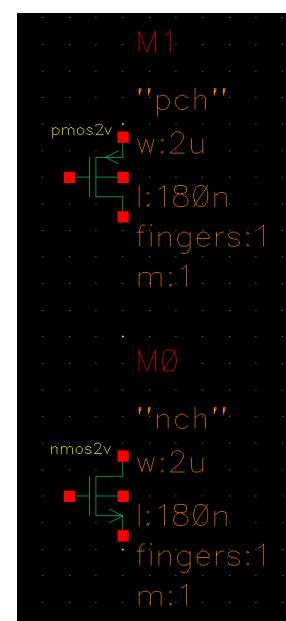
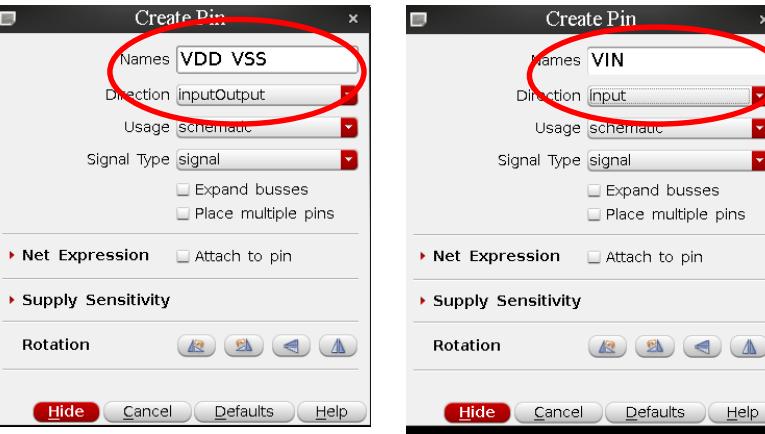
## □ Select tsmc18rf → pmos2v → symbol



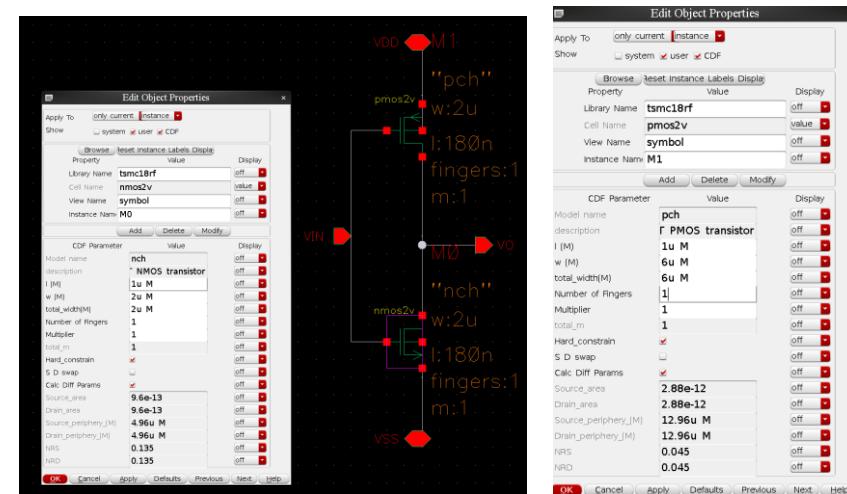
# Schematic Editor (4/4)



- Start to wire the instances using key “w” and add pins by using “p”



- Change the L and W of the MOSFETs by selecting the instance and press “q”. Do this step for NMOS and PMOS using the following table.



	L (μm)	W (μm)
M0	1	2
M1	1	6

- Check and save



# Outlines

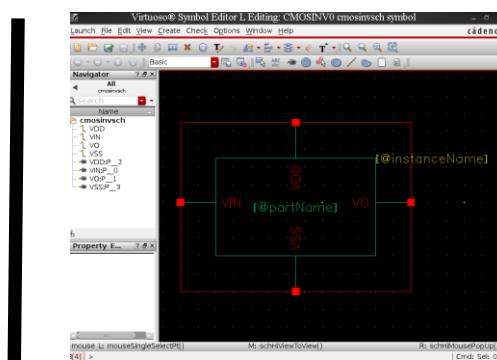
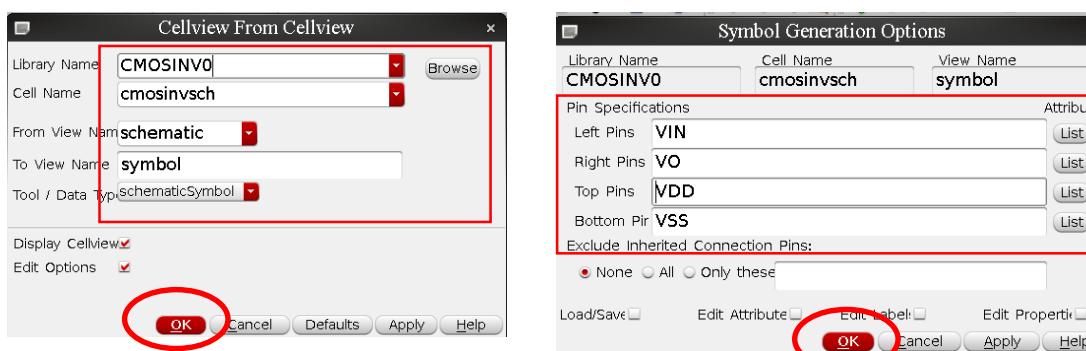
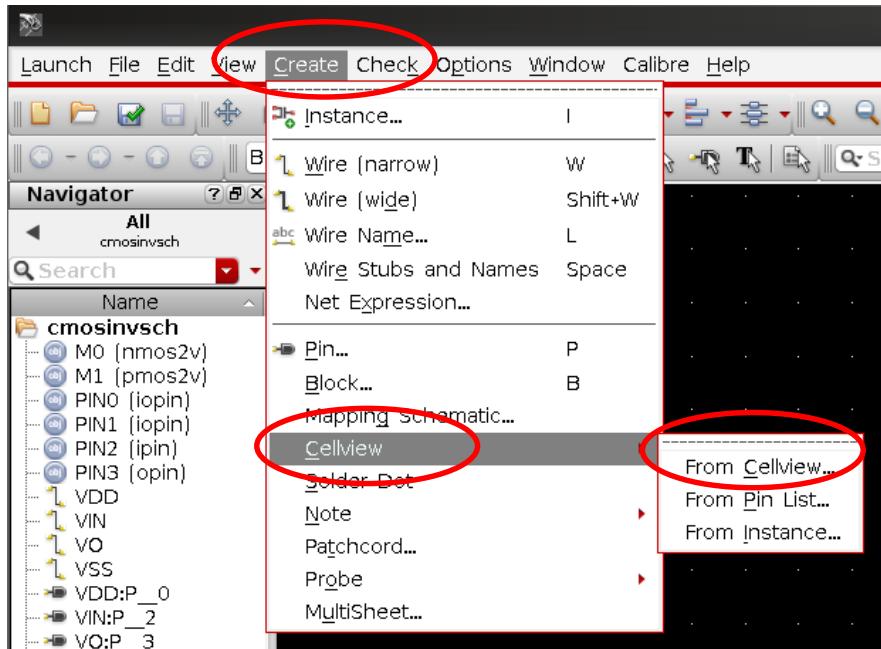
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# Create Symbol

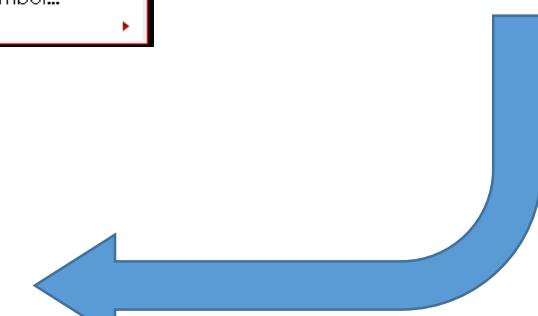
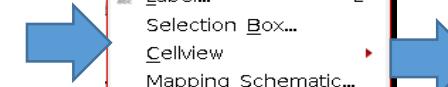
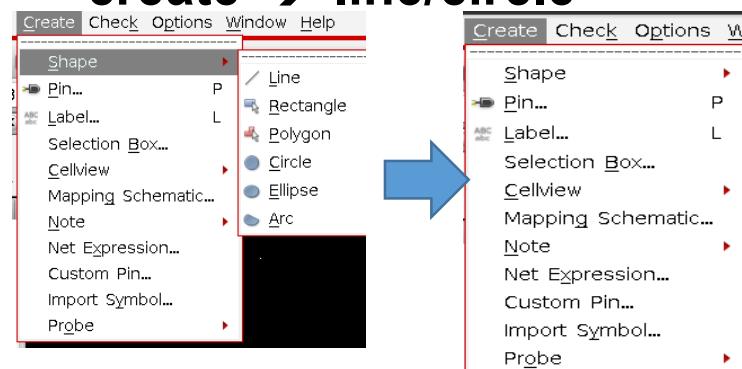
- To create a symbol create → cellview → from cellview



Remove the red box  
and green box



- Shape of the symbol can be adjusted using create → line/circle



# Outlines

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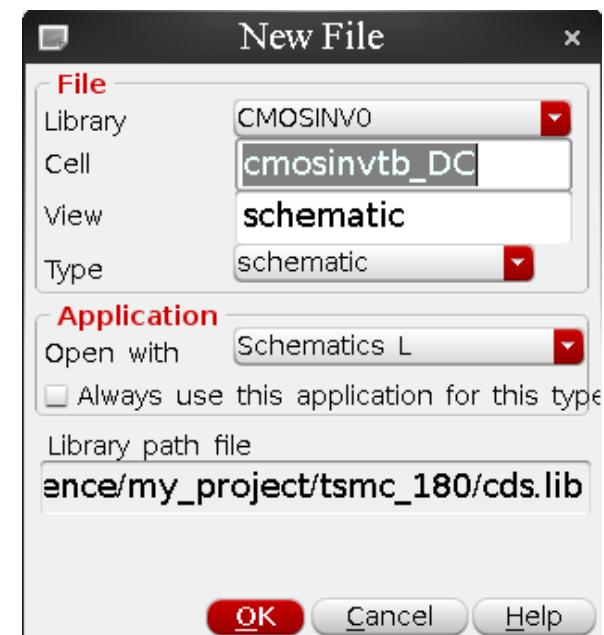
- Objective
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# Testbench (1/3)



- Create a testbench for DC sweep

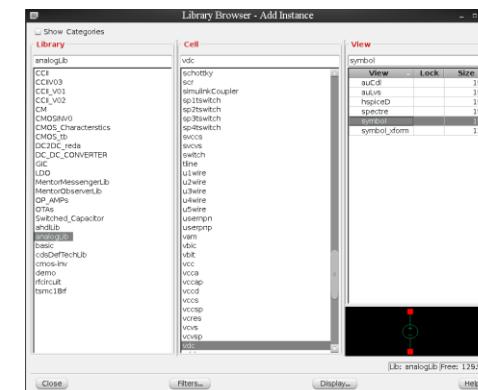
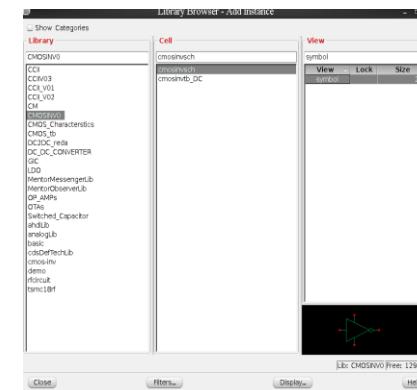
File → new → cellview



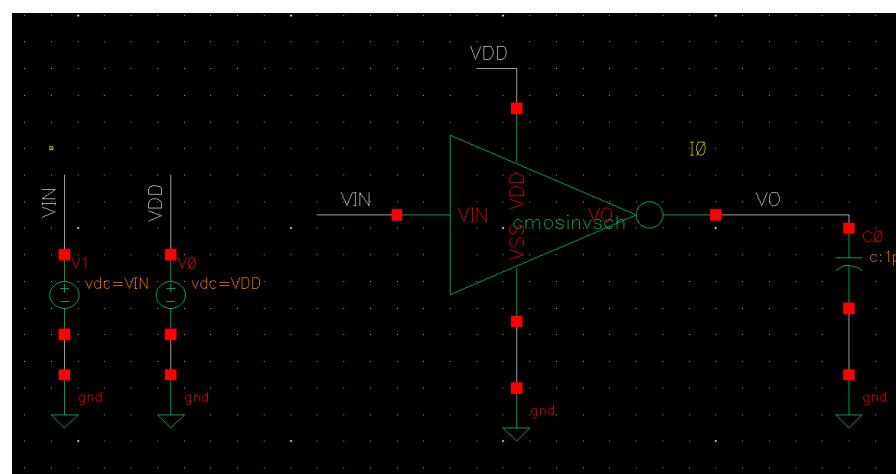
- Add your symbol



- Select your symbol lib, cell, and cell view
- Add DC power supply, gnd, and Cap from analog lib



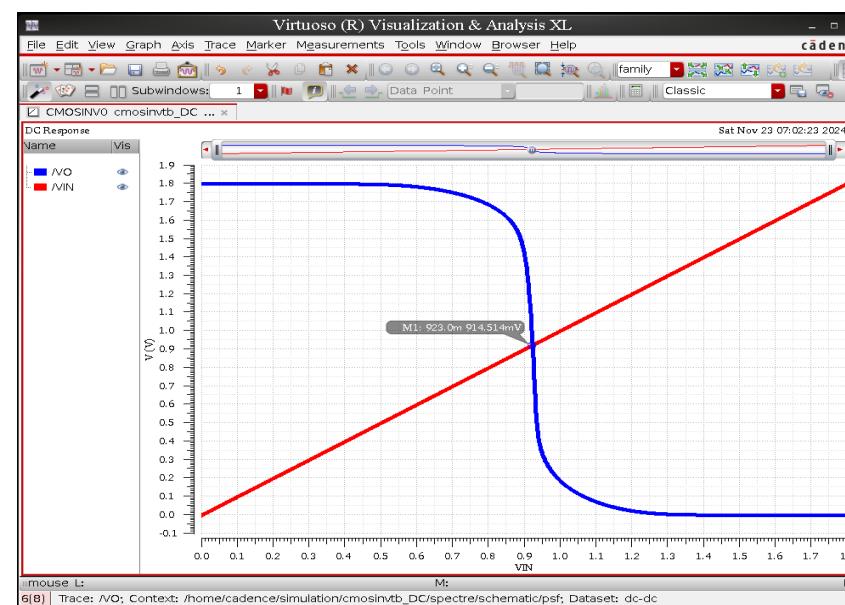
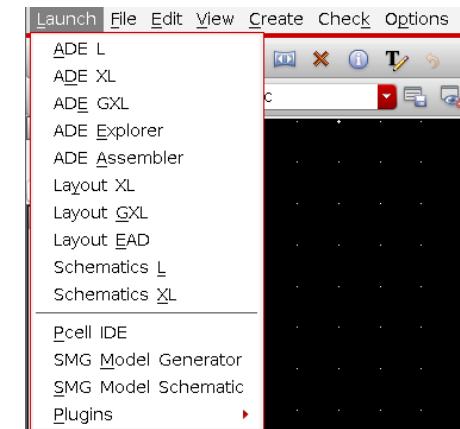
- Then, wire and add wire's labels using "l"



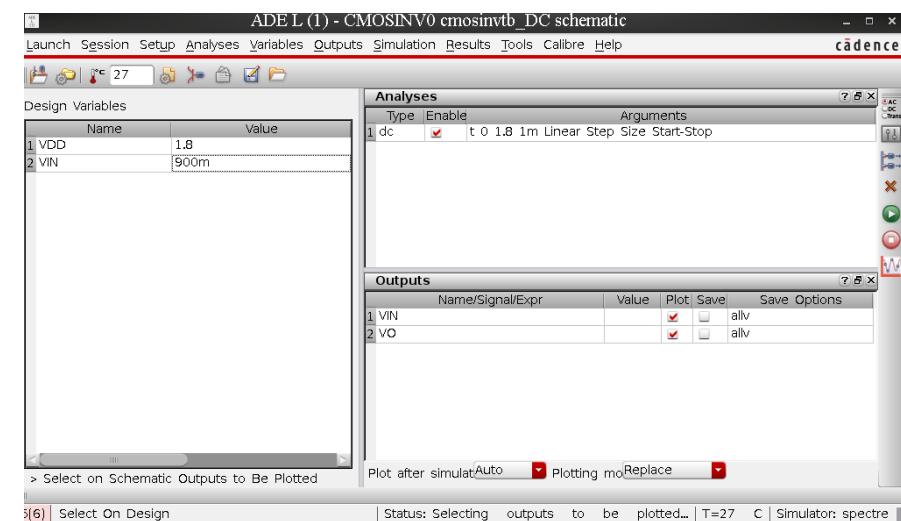
# Testbench (2/3)



## □ To start the simulation



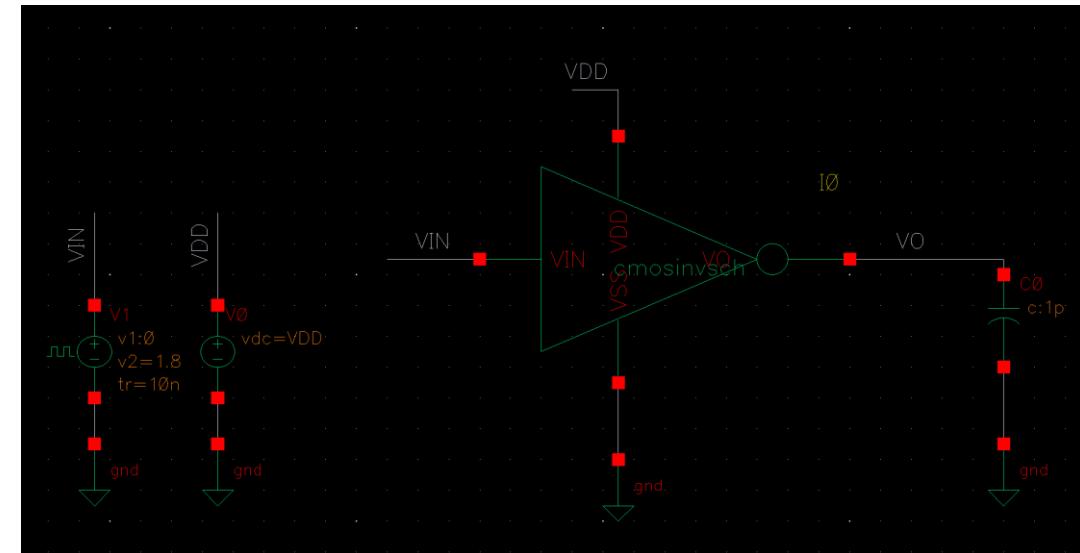
## □ Adjust the ADE as following and run



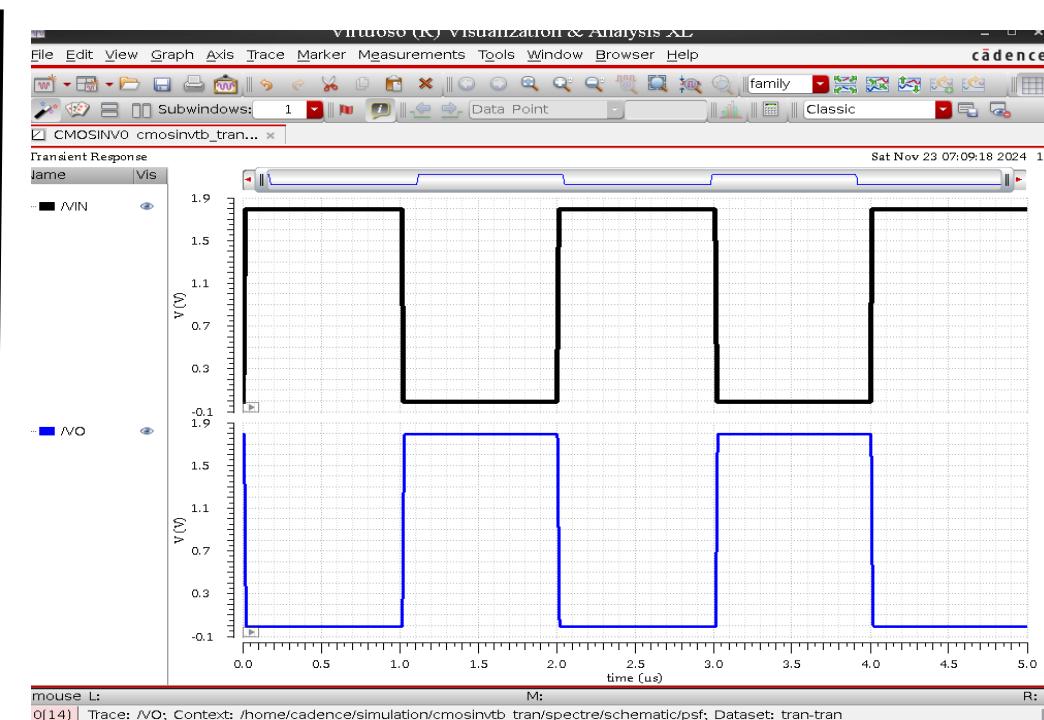
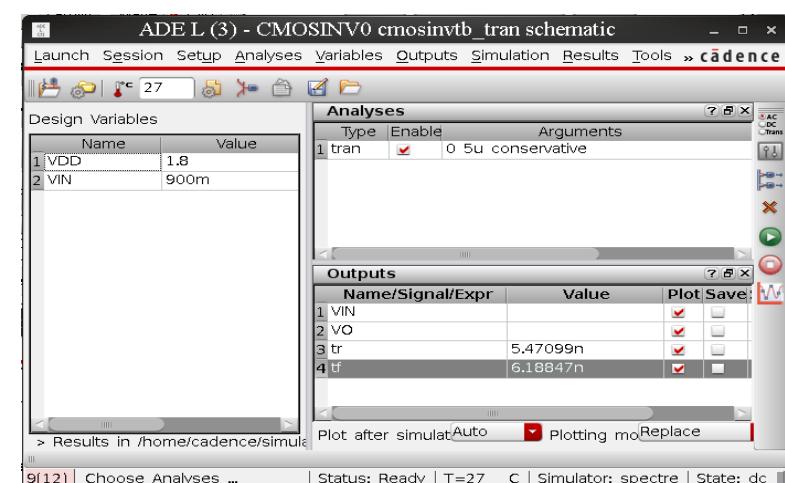
# Testbench (3/3)



## ☐ To start the transient simulation



## ☐ Adjust the ADE as following and run



```
tr= cross(v("/VO" ?result "tran") 1.62 1 "rising" nil nil ) -  
cross(v("/VO" ?result "tran") 0.18 1 "rising" nil nil )
```

```
tf=(cross(v("/VO" ?result "tran") 0.18 1 "falling" nil nil) -  
cross(v("/VO" ?result "tran") 1.62 1 "falling" nil nil))
```

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# Cadence Hot Keys



## Frequently used for schematic editor

w	add a wire
i	add an instance
p	Add a pin
l	Label to a wire
e	display options like, grid size, snap size etc
q	select an object and press q to open the property dialogue box
shift-z	zoom-out by 2x
ctrl-z	zoom-in by 2x
c	copy
m	move: if you move an object, none of the wires connected to it move to maintain connectivity
S	stretch: if you stretch an object all connections to it also extend to maintain connectivity
u /shift-U	Undo/ redo
f	fit: fits the entire schematic in the window
shift-X	descend to edit by one
b /shift-b	to go one level up / to return to top

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**Thanks!**