Post-layout Design and Simulation (IC Design Flow)

Dr. Ahmed Reda Mohamed[1,2]

[1]IRC for Communication Systems and Sensing, King Fahd University of Petroleum & Minerals, Dhahran 31261, Saudi Arabia

[2]PhD, The MoE Key Laboratory of Artificial Intelligence & Bio-Circuits and Systems Laboratory (*BiCASL*), Department of Micro-Nano Electronics, Shanghai Jiao Tong University, Shanghai, China.

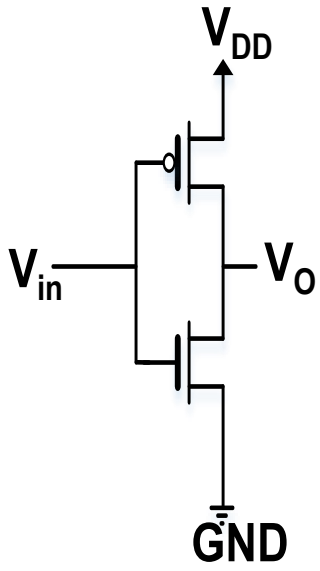
Outlines

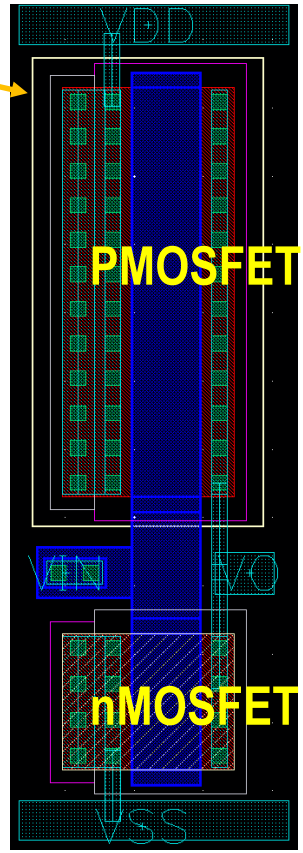
- ❑ Analog IC Design Flow
- ❑ Cadence Steps
- ❑ Conclusion

Outlines

- Analog IC Design Flow
- Cadence Steps
- Conclusion

Analog IC Design Flow

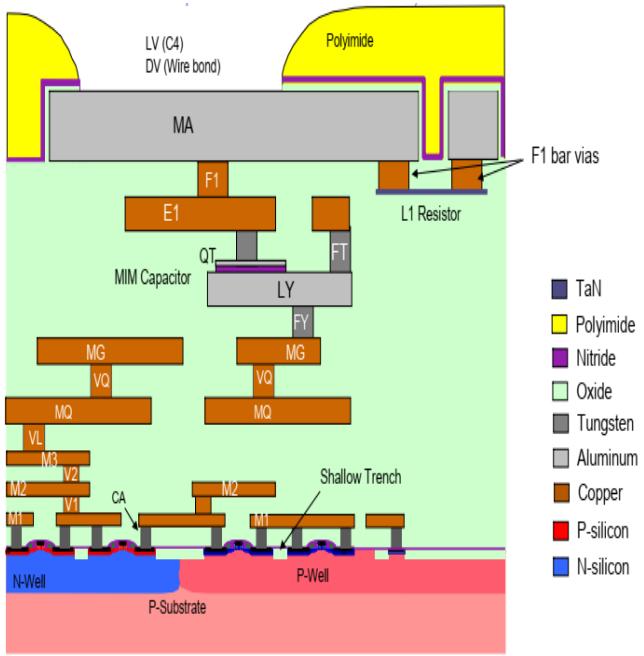




DRC Clean

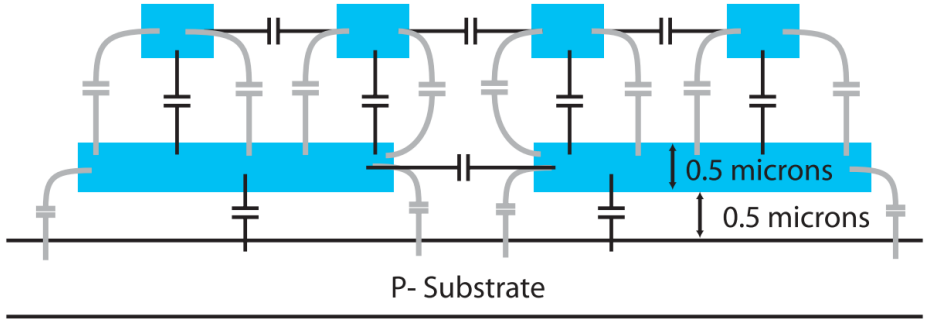
LVS Clean

PEX Clean ?

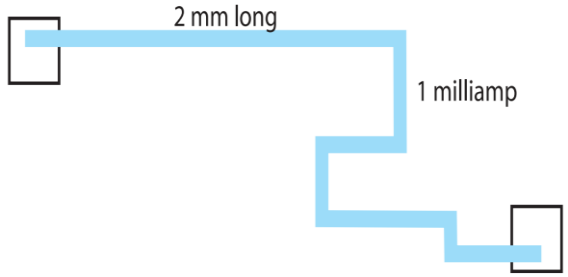


Process Cross-Section

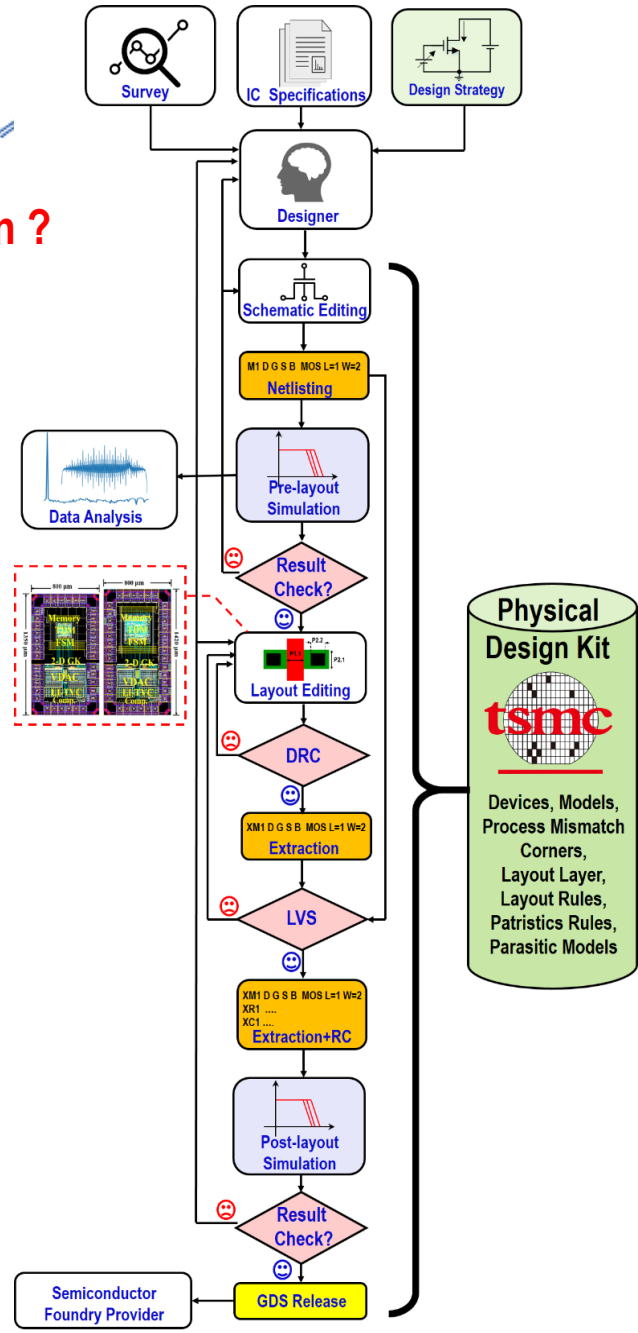
8 layers



Capacitance is everywhere



Parasitic Resistance



Analog IC design flow

Outlines

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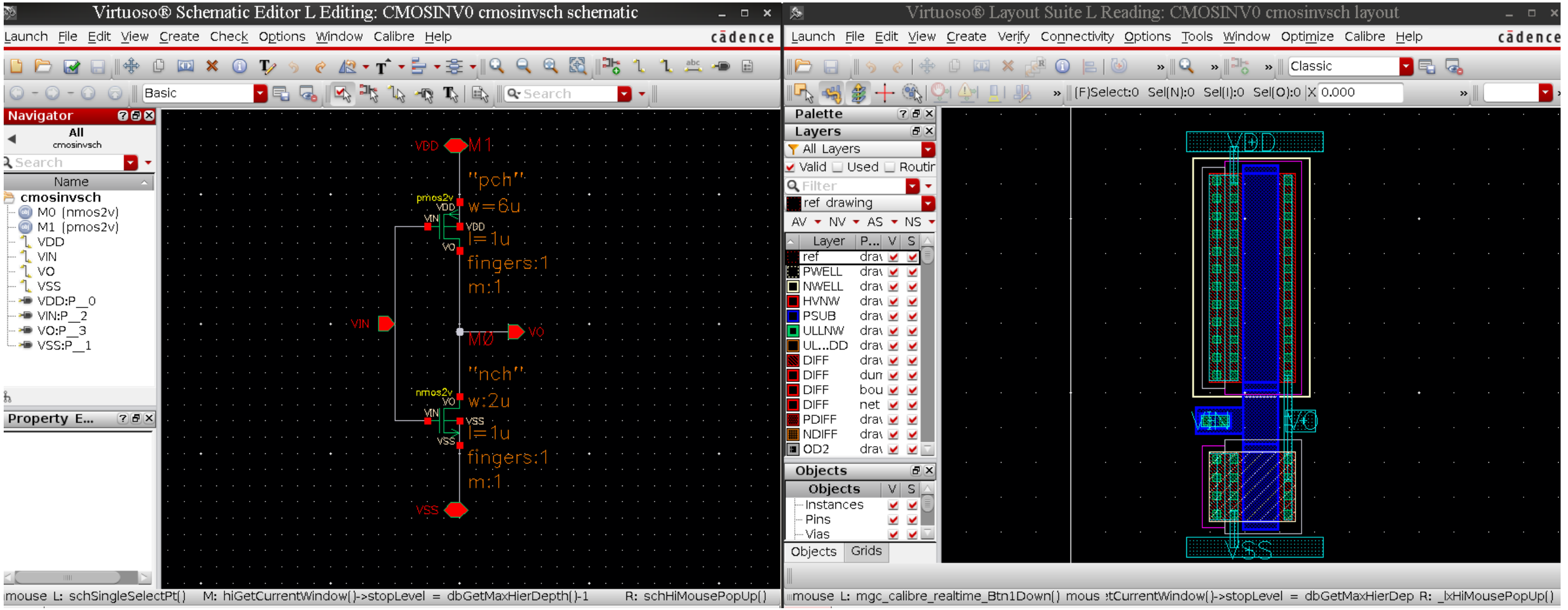
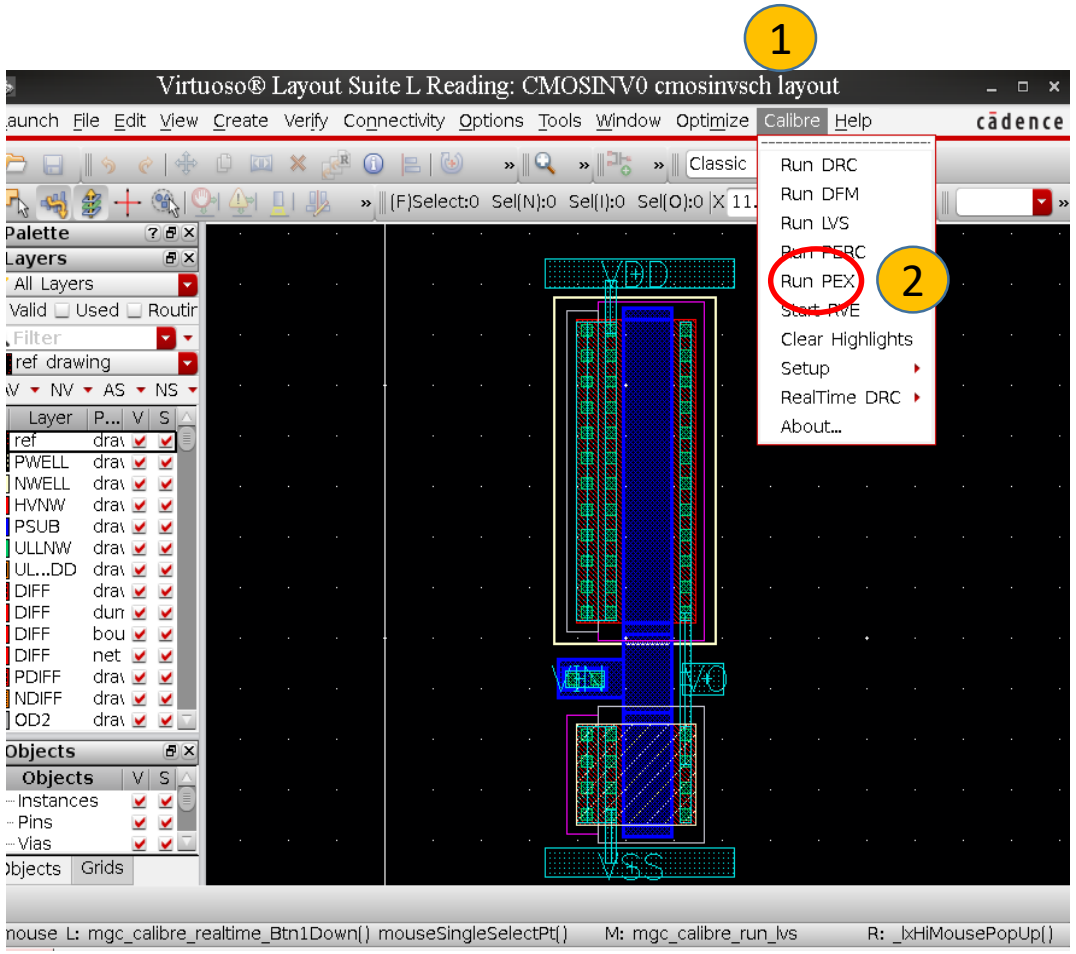
Steps (1/12)

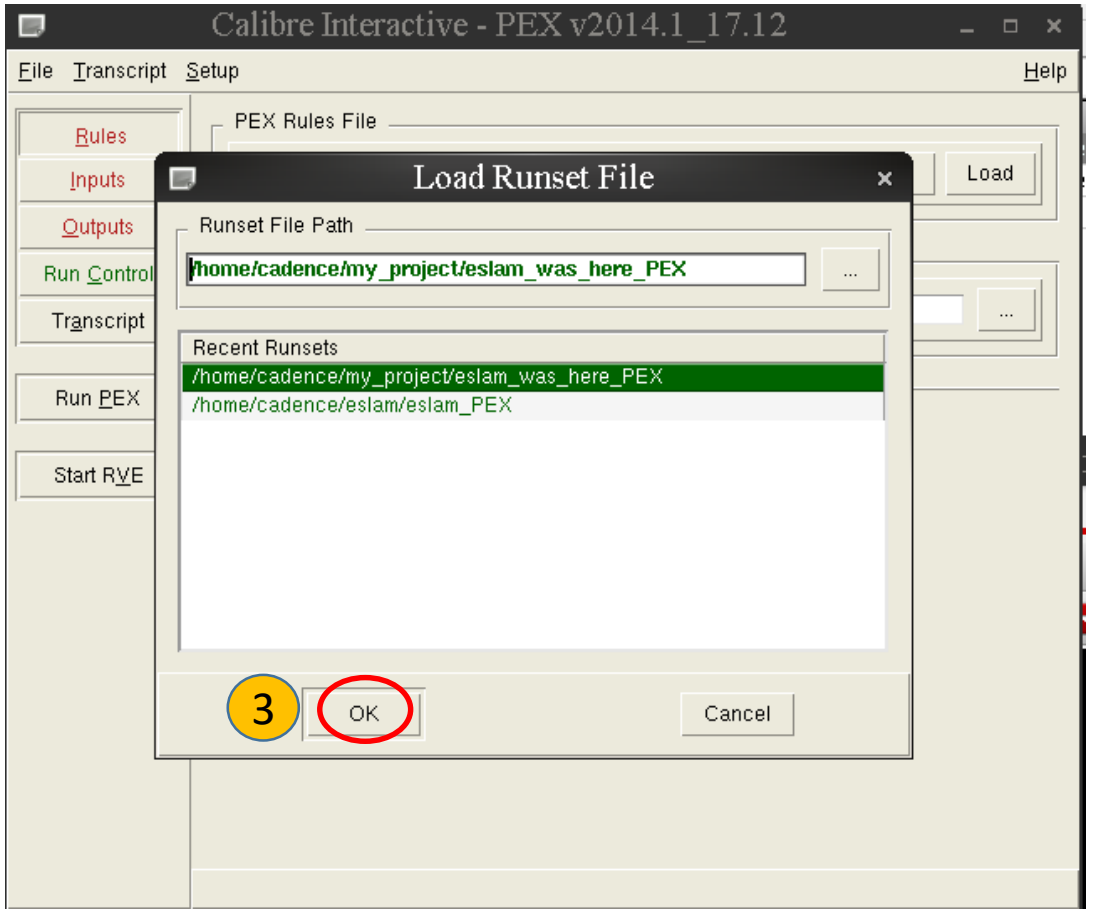


DRC Clean

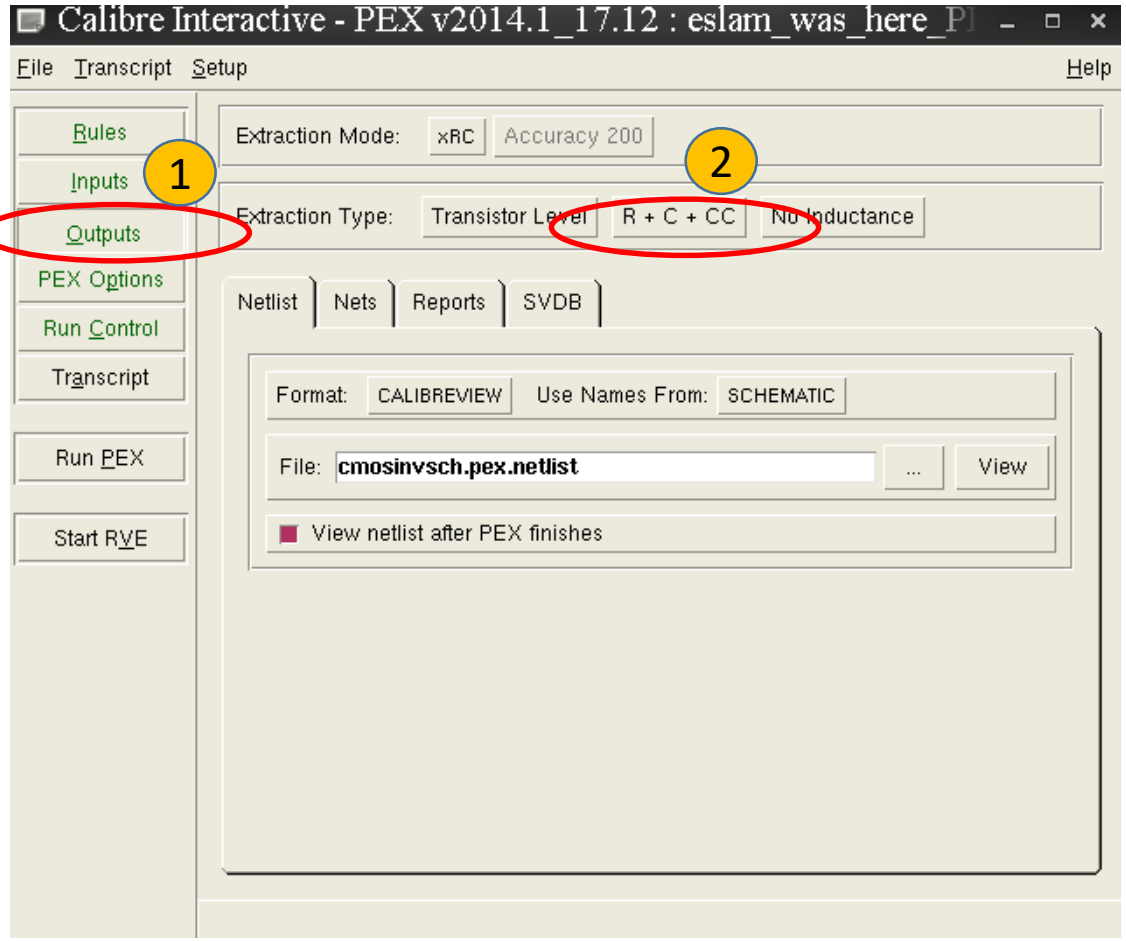
LVS Clean

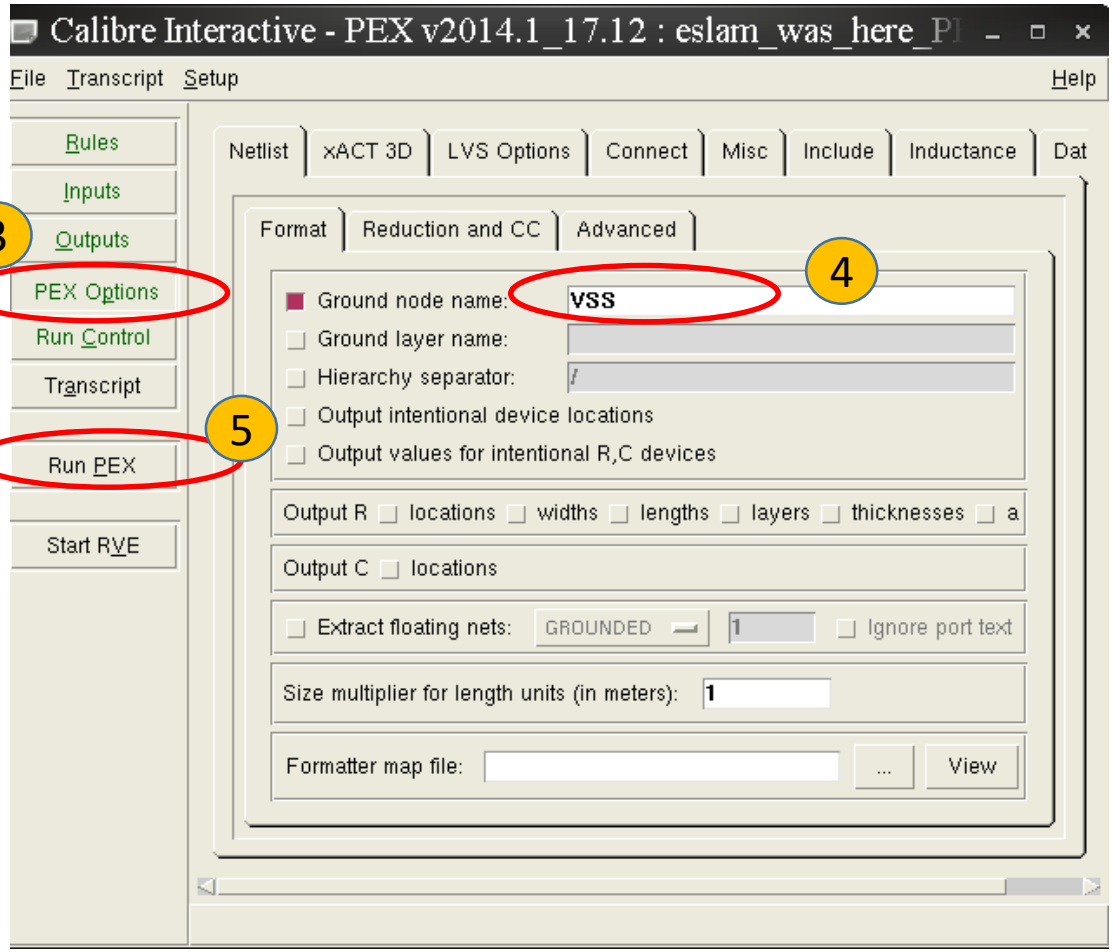
Steps (2/12)


1
Virtuoso® Layout Suite L Reading: CMOSINV0 cmosinvsch layout
Launch File Edit View Create Verify Connectivity Options Tools Window Optimize Calibre Help
cadence
Run DRC
Run DFM
Run LVS
Run PERC
Run PEX
Start RVE
Clear Highlights
Setup
RealTime DRC
About...
2
VDD
VSS
Palette
Layers
All Layers
Objects
Instances
Pins
Vias
Grids

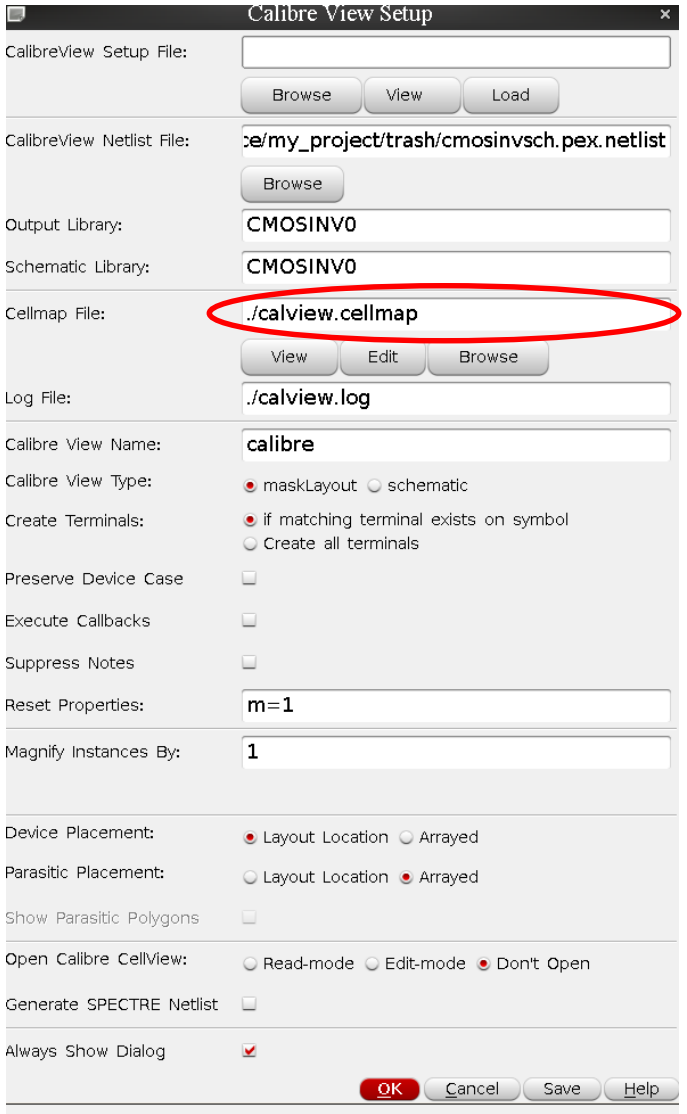

Calibre Interactive - PEX v2014.1_17.12
File Transcript Setup Help
Rules
Inputs
Outputs
Run Control
Transcript
Run PEX
Start RVE
PEX Rules File
Load
Load Runset File
Runset File Path
/home/cadence/my_project/eslam_was_here_PEX
Recent Runsets
/home/cadence/my_project/eslam_was_here_PEX
/home/cadence/eslam/eslam_PEX
3
OK
Cancel

Steps (3/12)

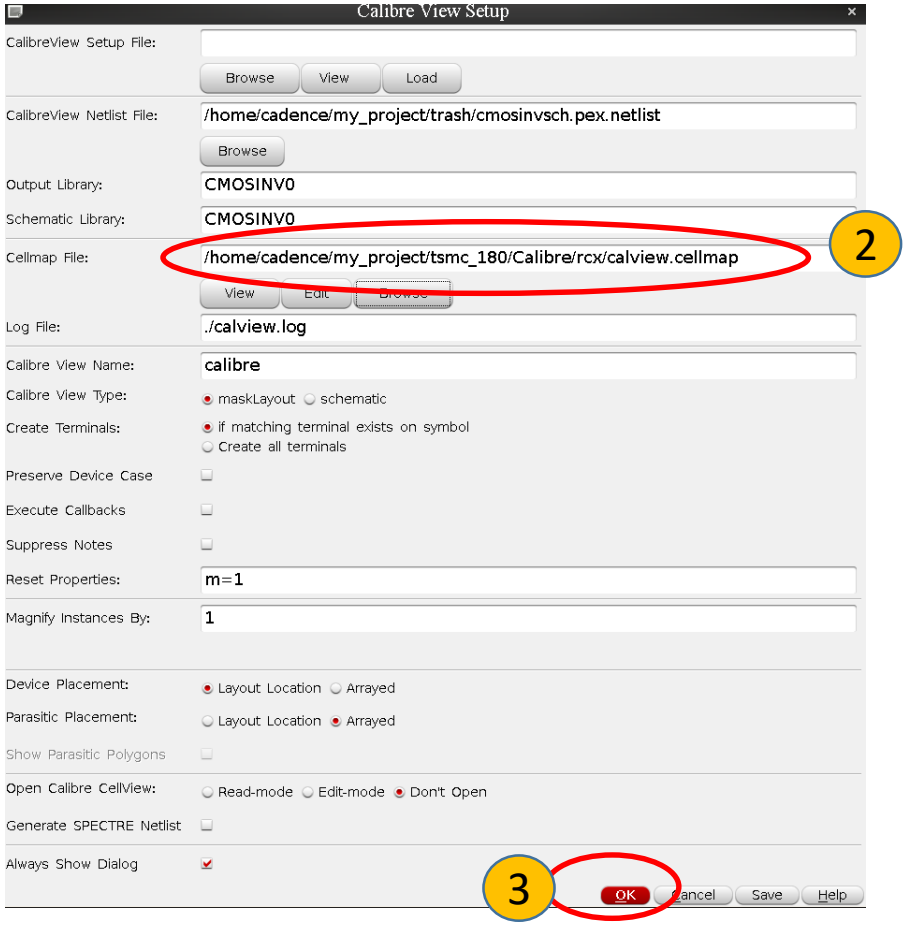

Calibre Interactive - PEX v2014.1_17.12 : eslam_was_here_P
File Transcript Setup Help
Rules
Inputs
Outputs
PEX Options
Run Control
Transcript
Run PEX
Start RVE
1
Extraction Mode: xRC Accuracy 200
2
Extraction Type: Transistor Level R + C + CC No Inductance
Netlist Nets Reports SVDB
Format: CALIBREVIEW Use Names From: SCHEMATIC
File: cmosinvsch.pex.netlist ... View
View netlist after PEX finishes


Calibre Interactive - PEX v2014.1_17.12 : eslam_was_here_P
File Transcript Setup Help
Rules
Inputs
3
Outputs
PEX Options
Run Control
Transcript
5
Run PEX
Start RVE
Netlist xACT 3D LVS Options Connect Misc Include Inductance Dat
Format Reduction and CC Advanced
4
Ground node name: VSS
Ground layer name:
Hierarchy separator: /
Output intentional device locations
Output values for intentional R,C devices
Output R locations widths lengths layers thicknesses a
Output C locations
Extract floating nets: GROUNDED 1 Ignore port text
Size multiplier for length units (in meters): 1
Formatter map file: ... View

Steps (4/12)

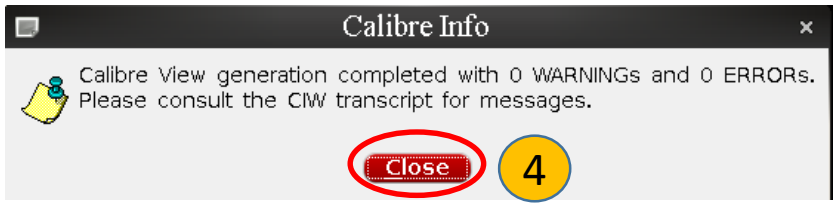


1



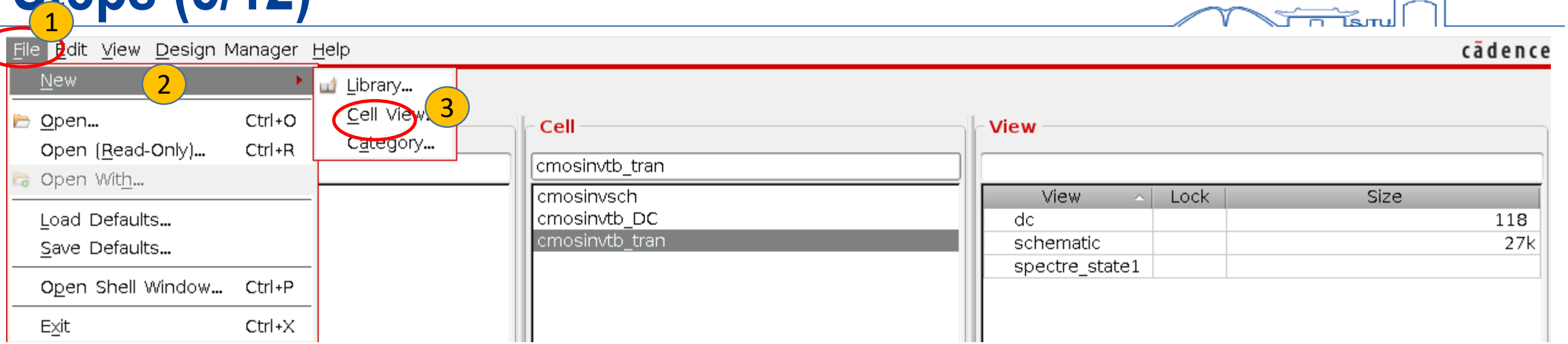
2

3

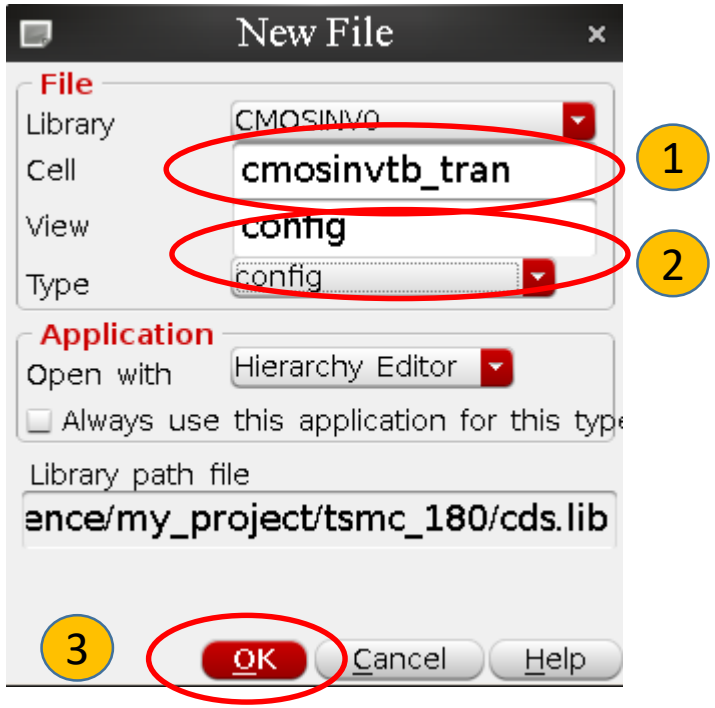


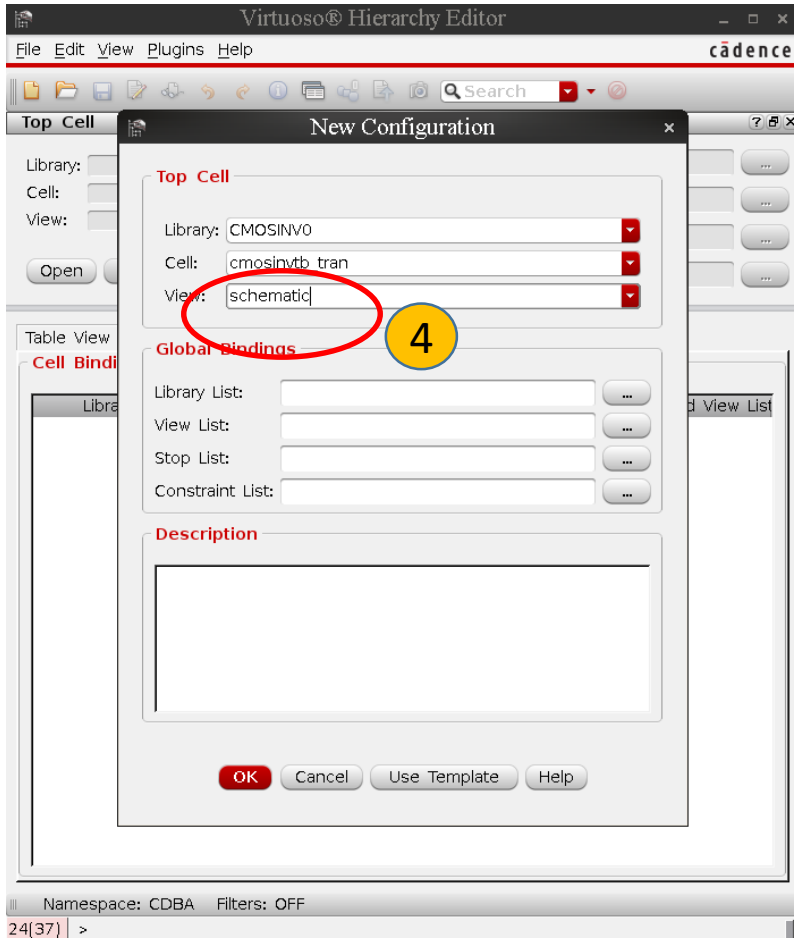
4

Steps (5/12)

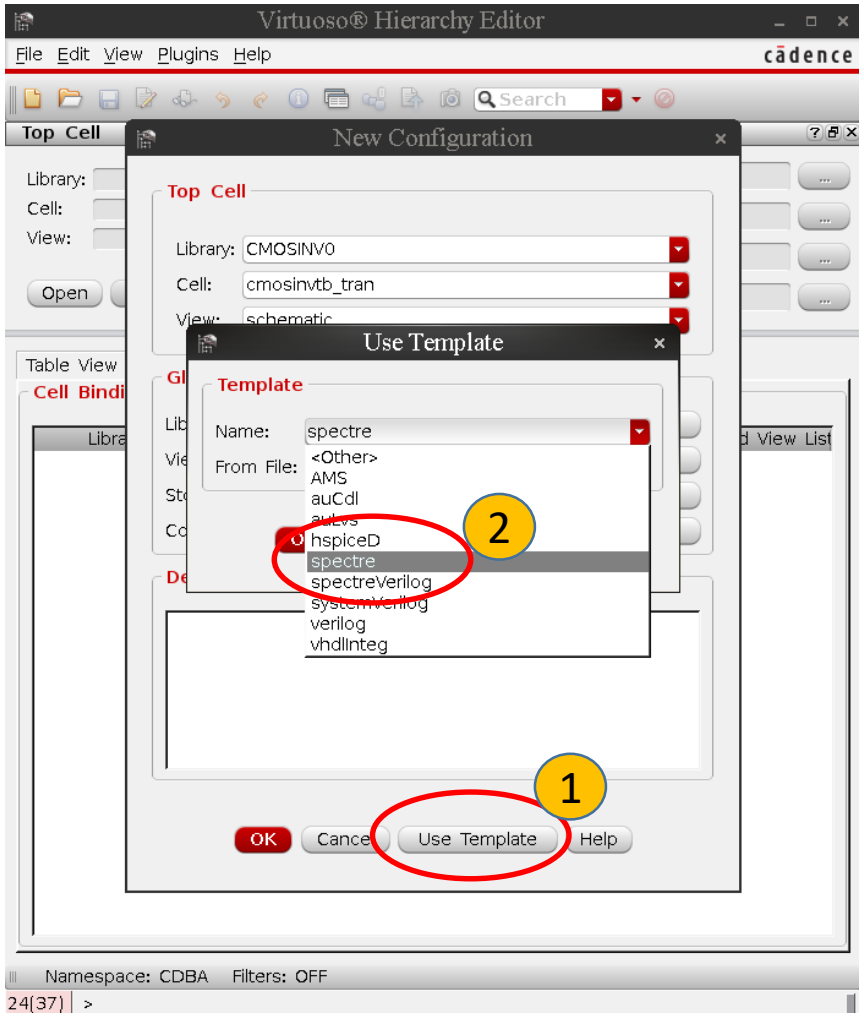

1
File Edit View Design Manager Help
cadence
New
2
Open... Ctrl+O
Open (Read-Only)... Ctrl+R
Open With...
Load Defaults...
Save Defaults...
Open Shell Window... Ctrl+P
Exit Ctrl+X
Library...
Cell View...
Category...
3
Cell
cmosinvtb_tran
cmosinvsch
cmosinvtb_DC
cmosinvtb_tran
View
View
Lock
Size
dc
118
schematic
27k
spectre_state1

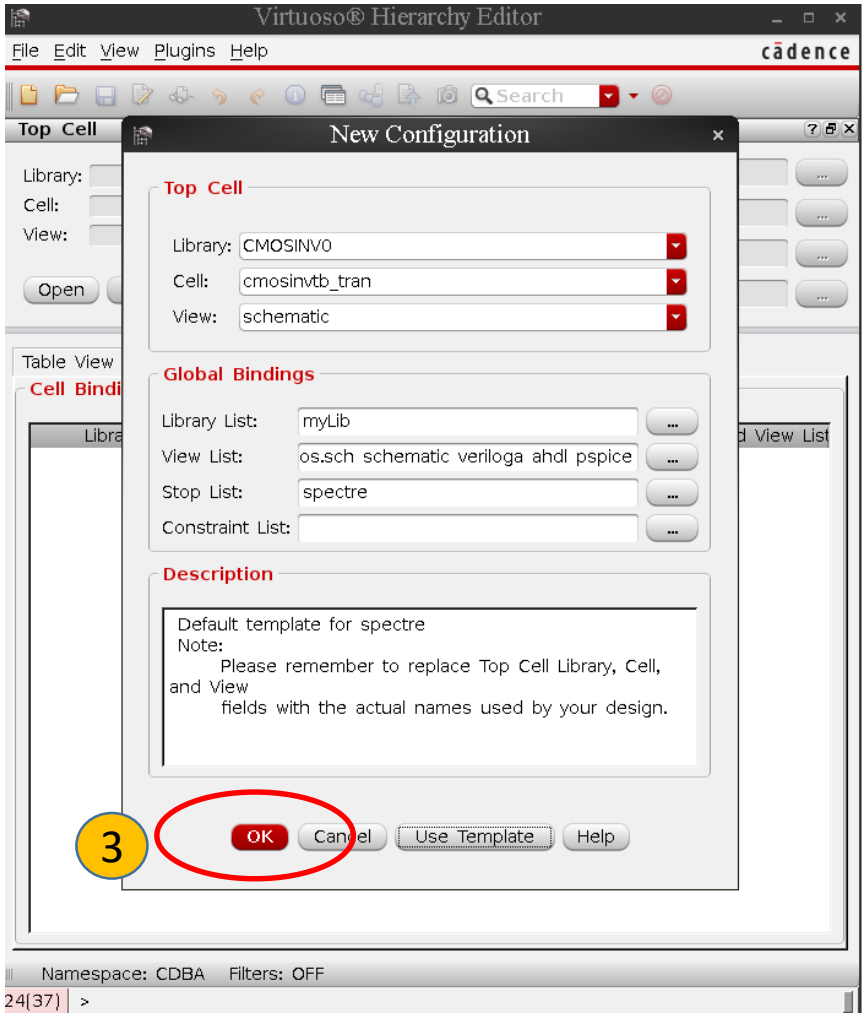
Steps (6/12)


New File
File
Library
CMOSINV0
Cell
cmosinvtb_tran
View
config
Type
config
Application
Open with
Hierarchy Editor
Always use this application for this type
Library path file
ence/my_project/tsmc_180/cds.lib
OK
Cancel
Help
1
2
3

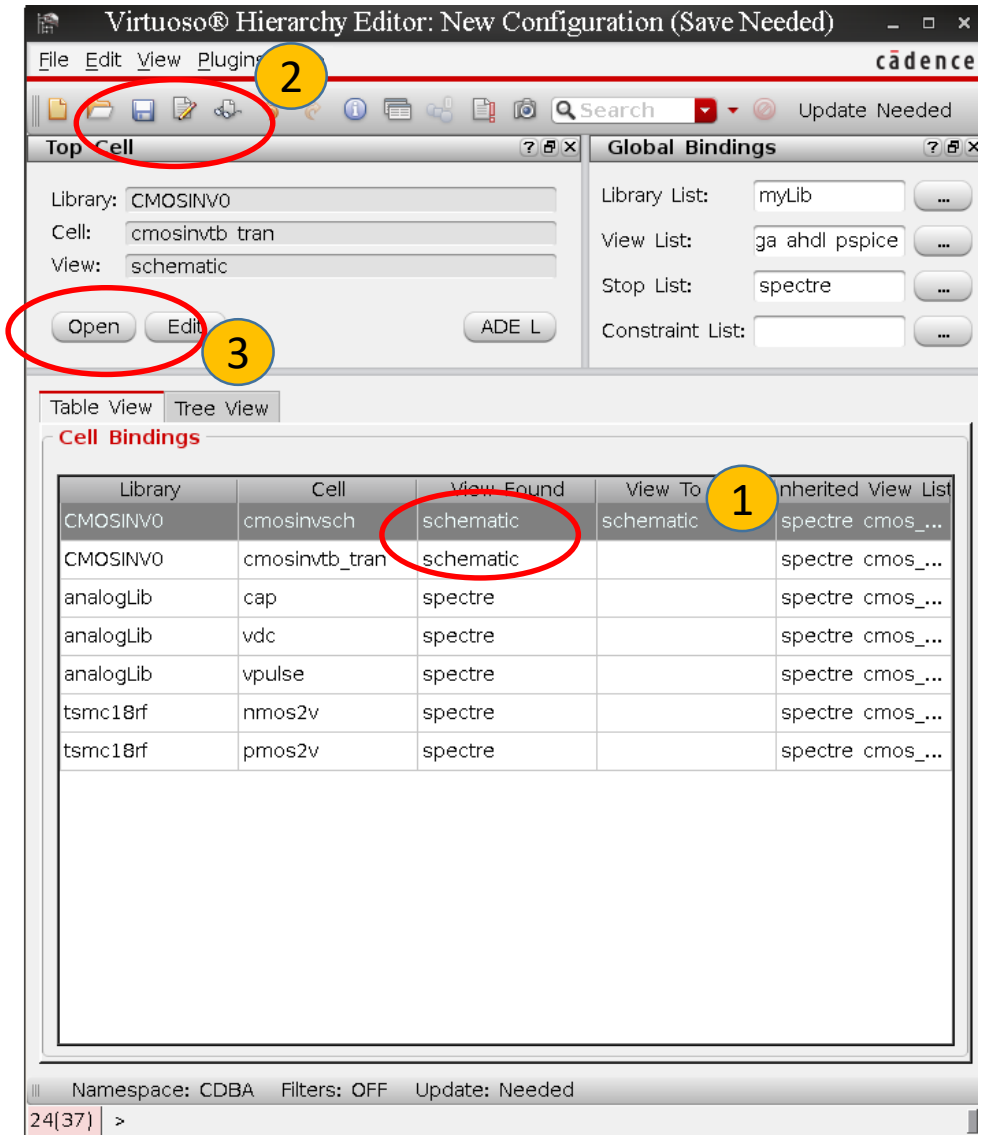

Virtuoso® Hierarchy Editor
File Edit View Plugins Help
cadence
Search
Top Cell
Library:
Cell:
View:
Open
Table View
Cell Bindi
New Configuration
Top Cell
Library: CMOSINV0
Cell: cmosinvtb_tran
View: schematic
Global Bindings
Library List:
View List:
Stop List:
Constraint List:
Description
OK
Cancel
Use Template
Help
4
Namespace: CDBA
Filters: OFF
24[37]

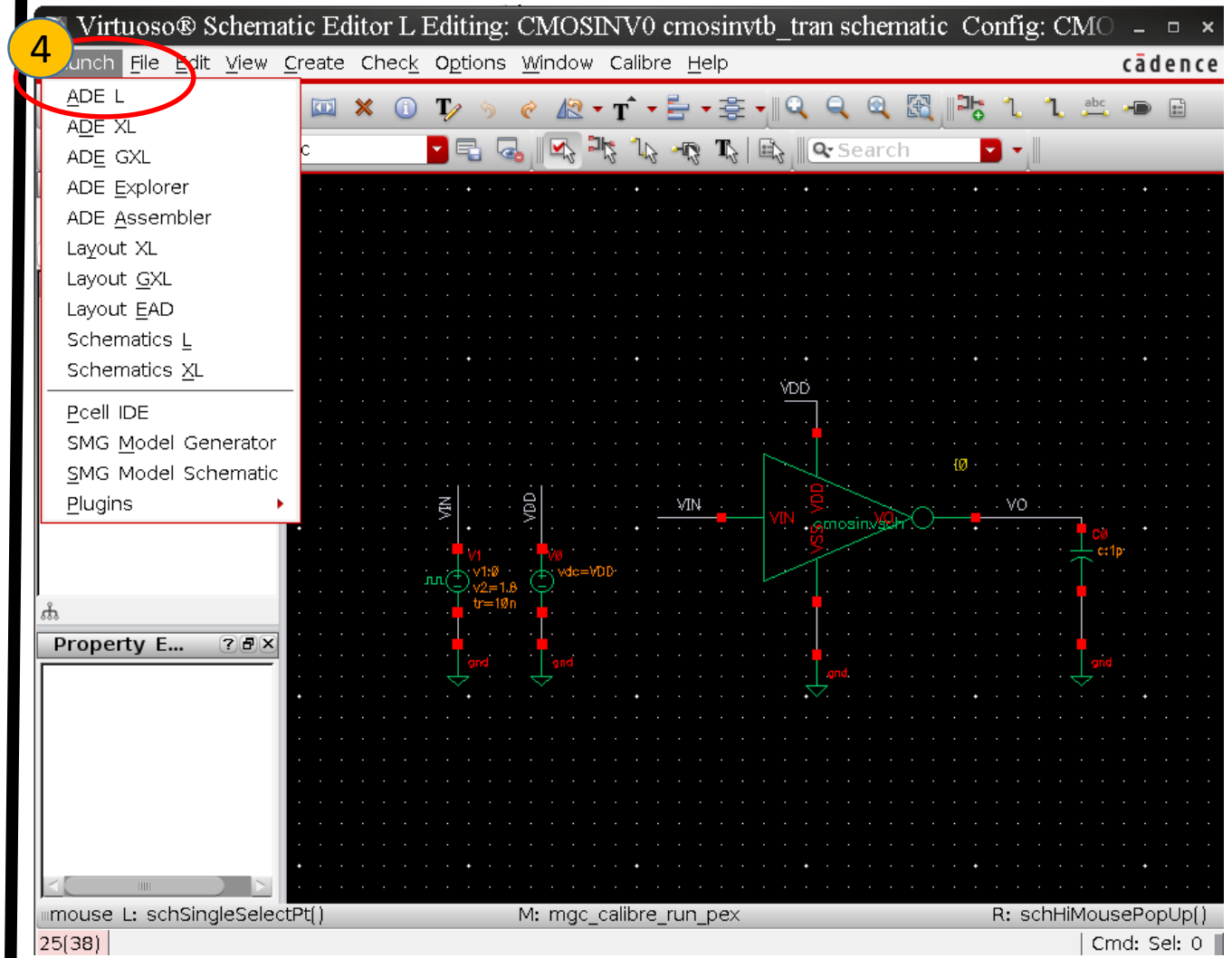
Steps (7/12)


Virtuoso® Hierarchy Editor
File Edit View Plugins Help
cadence
Top Cell
New Configuration
Top Cell
Library: CMOSINV0
Cell: cmosinvtb_tran
View: schematic
Use Template
Template
Name: spectre
From File:
<Other>
AMS
auCdl
hspiceD
spectre
spectreVerilog
verilog
vhdlInteg
1
2
OK
Cancel
Use Template
Help
Table View
Cell Bindi
Namespace: CDBA Filters: OFF
24(37) >

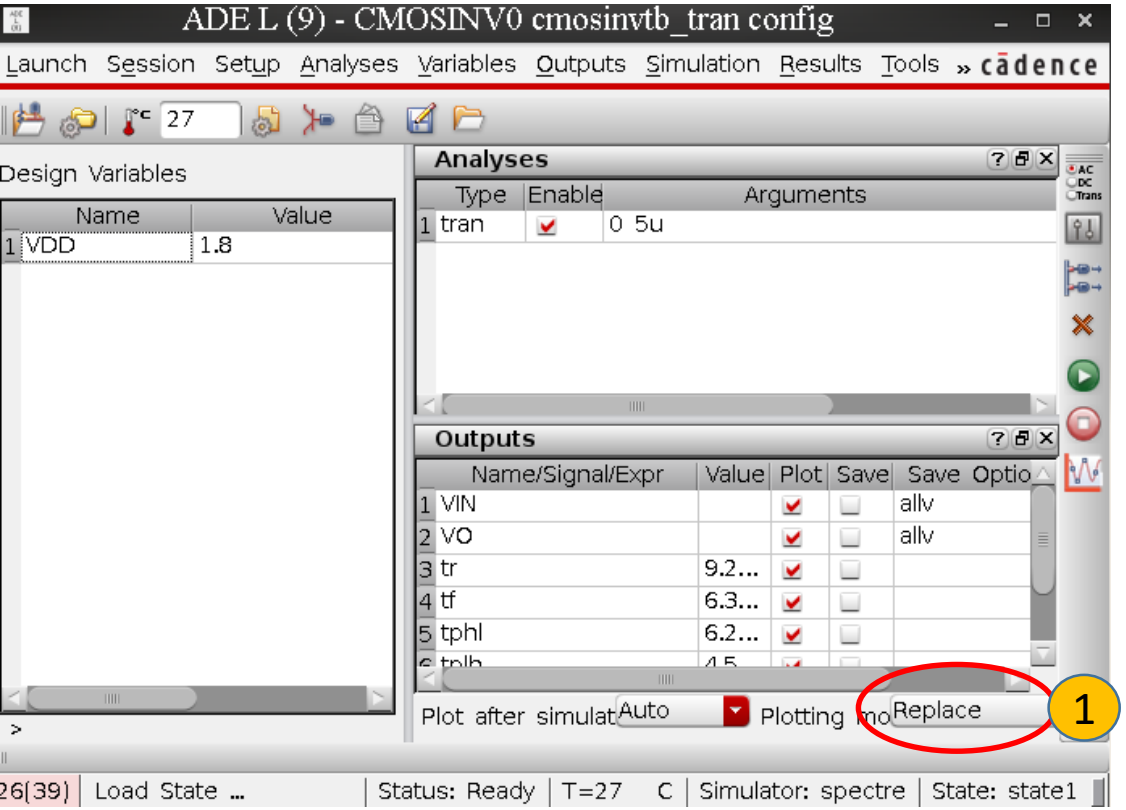

Virtuoso® Hierarchy Editor
File Edit View Plugins Help
cadence
Top Cell
New Configuration
Top Cell
Library: CMOSINV0
Cell: cmosinvtb_tran
View: schematic
Global Bindings
Library List: myLib
View List: os.sch schematic veriloga ahdl pspice
Stop List: spectre
Constraint List:
Description
Default template for spectre
Note:
Please remember to replace Top Cell Library, Cell, and View
fields with the actual names used by your design.
3
OK
Cancel
Use Template
Help
Table View
Cell Bindi
Namespace: CDBA Filters: OFF
24(37) >

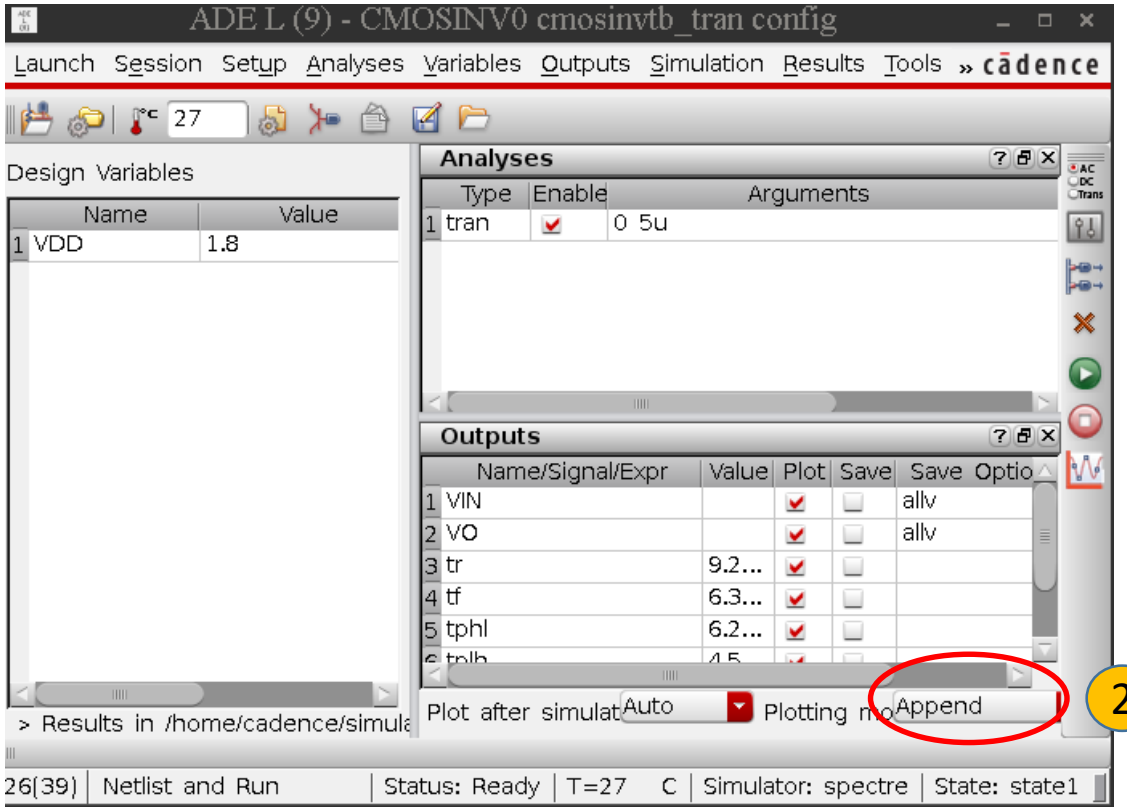
Steps (8/12)


Virtuoso® Hierarchy Editor: New Configuration (Save Needed)
File Edit View Plugins
cadence
Search
Update Needed
Top Cell
Library: CMOSINV0
Cell: cmosinvtb_tran
View: schematic
Open
Edit
ADE L
Global Bindings
Library List: myLib
View List: ga ahdl pspice
Stop List: spectre
Constraint List:
Table View
Tree View
Cell Bindings
Library Cell View Found View To Inherited View List
CMOSINV0 cmosinvsch schematic schematic spectre cmos_...
CMOSINV0 cmosinvtb_tran schematic spectre cmos_...
analogLib cap spectre spectre cmos_...
analogLib vdc spectre spectre cmos_...
analogLib vpulse spectre spectre cmos_...
tsmc18rf nmos2v spectre spectre cmos_...
tsmc18rf pmos2v spectre spectre cmos_...
Namespace: CDBA Filters: OFF Update: Needed
24(37)
1
2
3

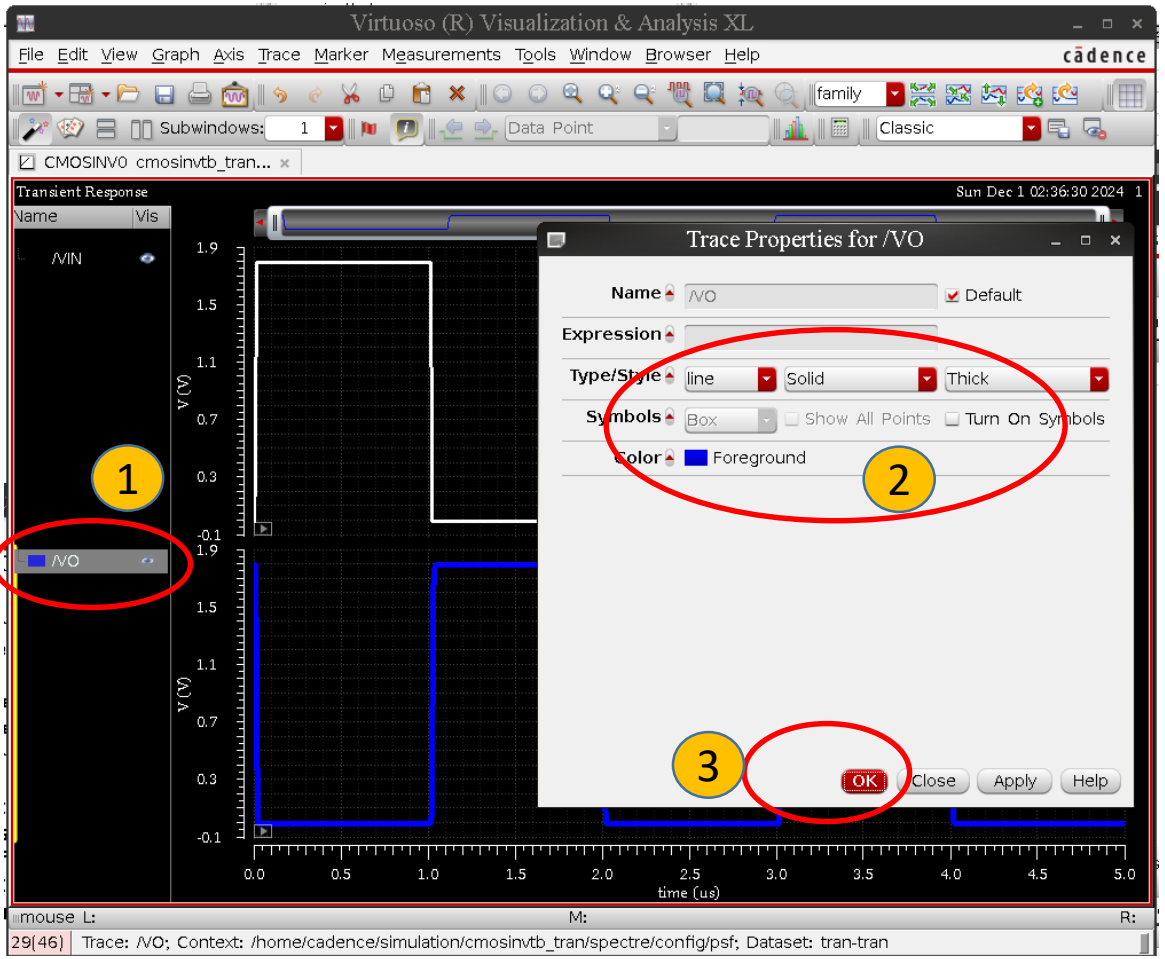

Virtuoso® Schematic Editor L Editing: CMOSINV0 cmosinvtb_tran schematic Config: CMO
Launch File Edit View Create Check Options Window Calibre Help
cadence
ADE L
ADE XL
ADE GXL
ADE Explorer
ADE Assembler
Layout XL
Layout GXL
Layout EAD
Schematics L
Schematics XL
Pcell IDE
SMG Model Generator
SMG Model Schematic
Plugins
Property E...
Search
VDD
VIN
VO
mouse L: schSingleSelectPt()
M: mgc_calibre_run_pex
R: schHiMousePopUp()
25(38)
Cmd: Sel: 0
4

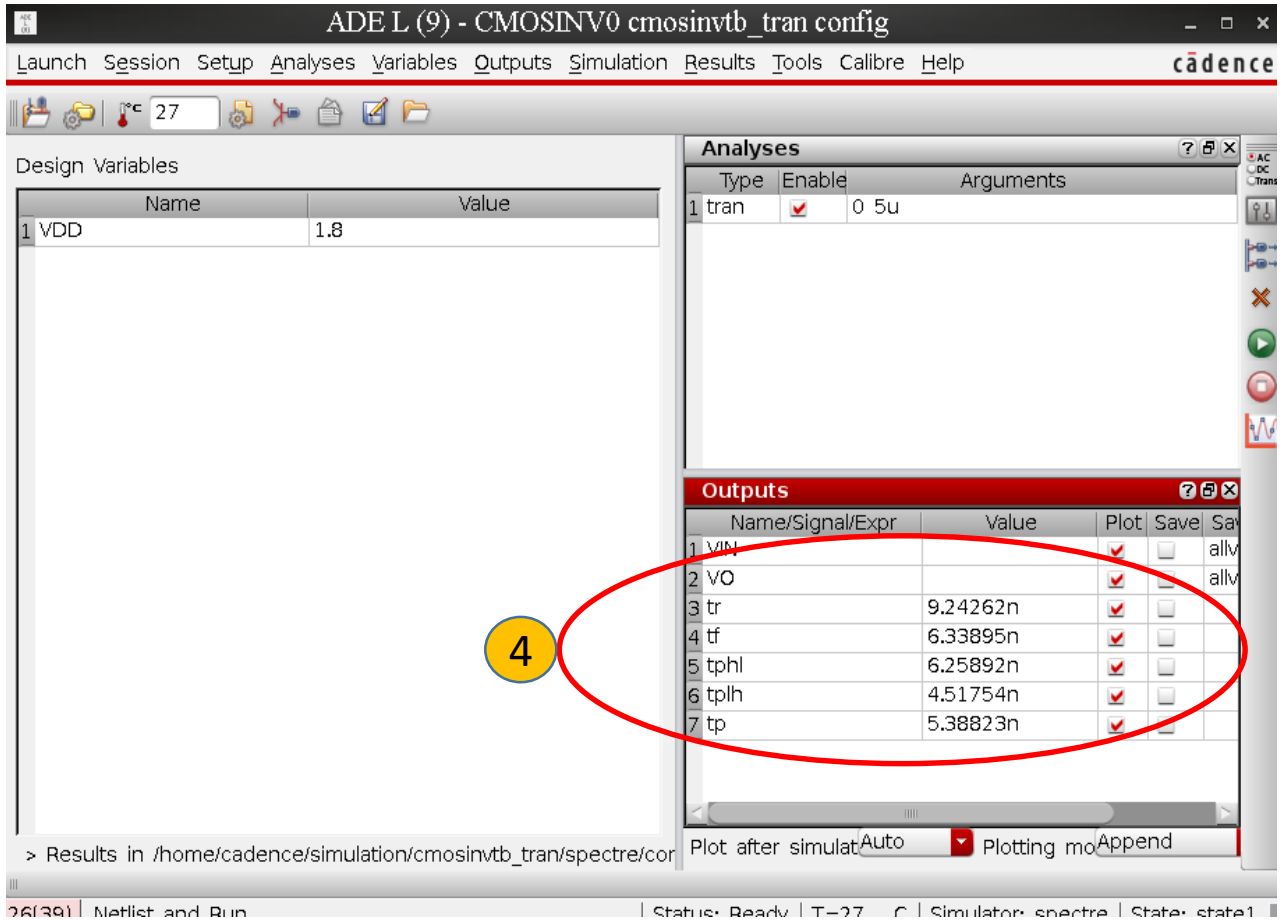
Steps (9/12)


ADE L (9) - CMOSINV0 cmosinvtb_tran config
Launch Session Setup Analyses Variables Outputs Simulation Results Tools » cadence
Design Variables
Name Value
1 VDD 1.8
Analyses
Type Enable Arguments
1 tran 0 5u
Outputs
Name/Signal/Expr Value Plot Save Save Optio
1 VIN allv
2 VO allv
3 tr 9.2...
4 tf 6.3...
5 tphl 6.2...
Plot after simulat Auto Plotting mo Replace
1
26(39) Load State ... Status: Ready T=27 C Simulator: spectre State: state1

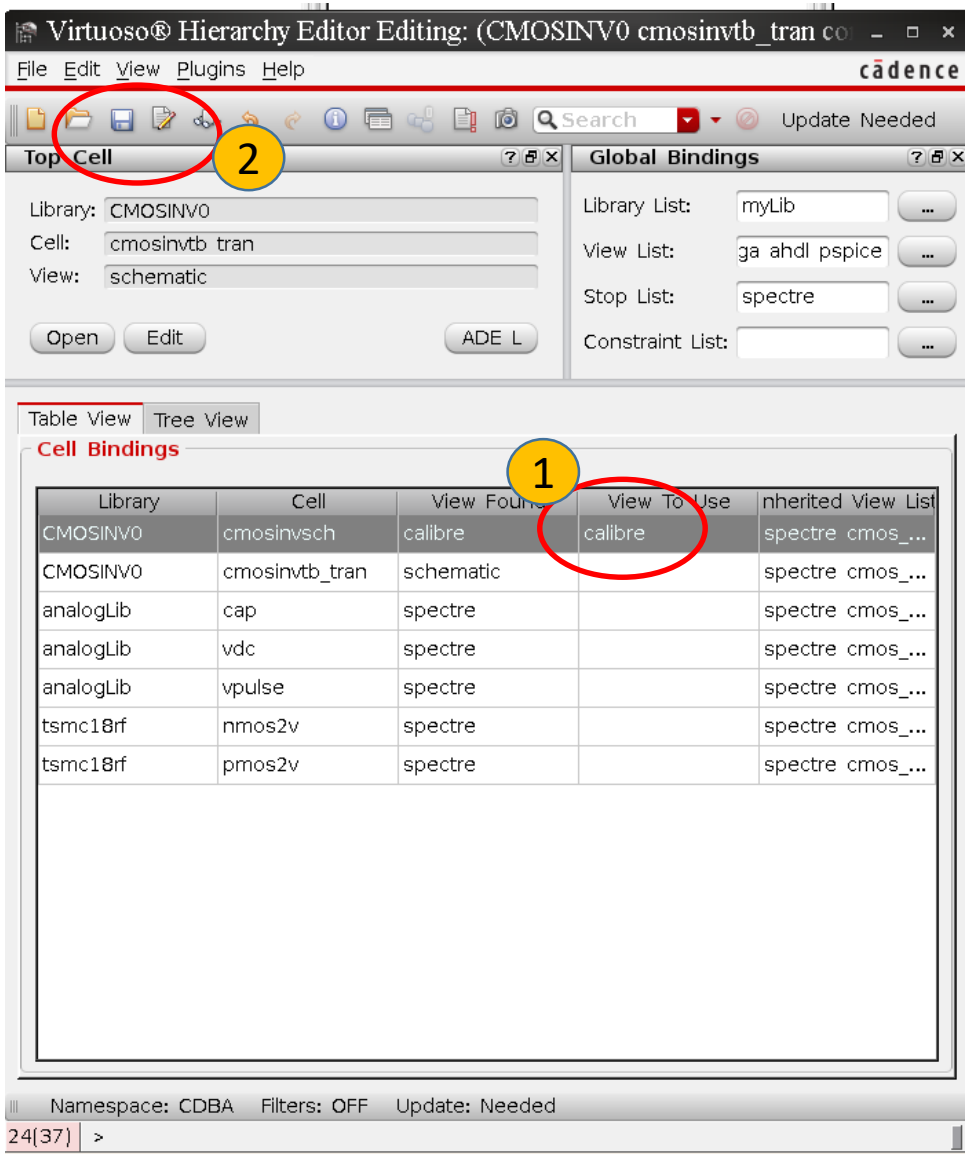

ADE L (9) - CMOSINV0 cmosinvtb_tran config
Launch Session Setup Analyses Variables Outputs Simulation Results Tools » cadence
Design Variables
Name Value
1 VDD 1.8
Analyses
Type Enable Arguments
1 tran 0 5u
Outputs
Name/Signal/Expr Value Plot Save Save Optio
1 VIN allv
2 VO allv
3 tr 9.2...
4 tf 6.3...
5 tphl 6.2...
> Results in /home/cadence/simula
Plot after simulat Auto Plotting mo Append
2
26(39) Netlist and Run Status: Ready T=27 C Simulator: spectre State: state1

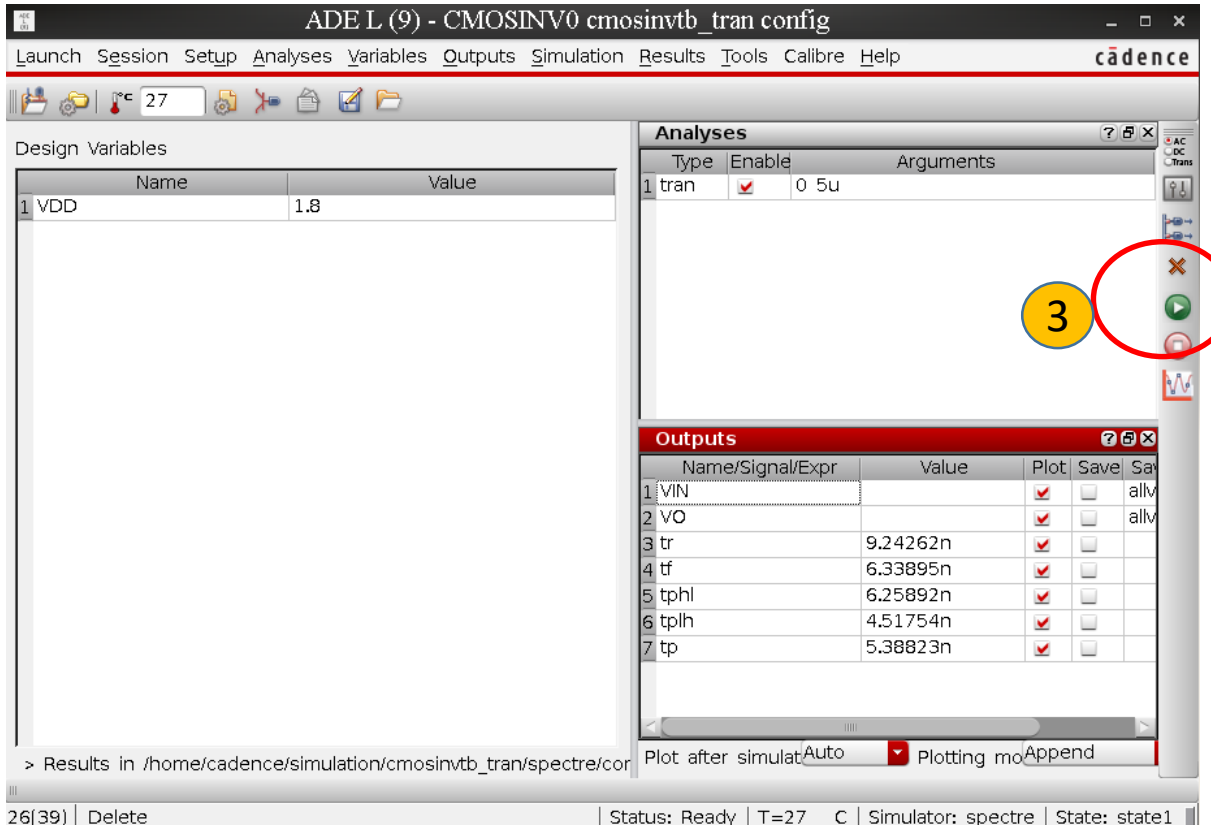
Steps (10/12)


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Transient Response
Sun Dec 1 02:36:30 2024
/VIN
/VO
Trace Properties for /VO
Name /VO Default
Expression
Type/Style line Solid Thick
Symbols Box Show All Points Turn On Symbols
Color Foreground
OK Close Apply Help
1
2
3
time (us)
mouse L: M: R:
29(46) Trace: /VO; Context: /home/cadence/simulation/cmosinvtb_tran/spectre/config/psf; Dataset: tran-tran

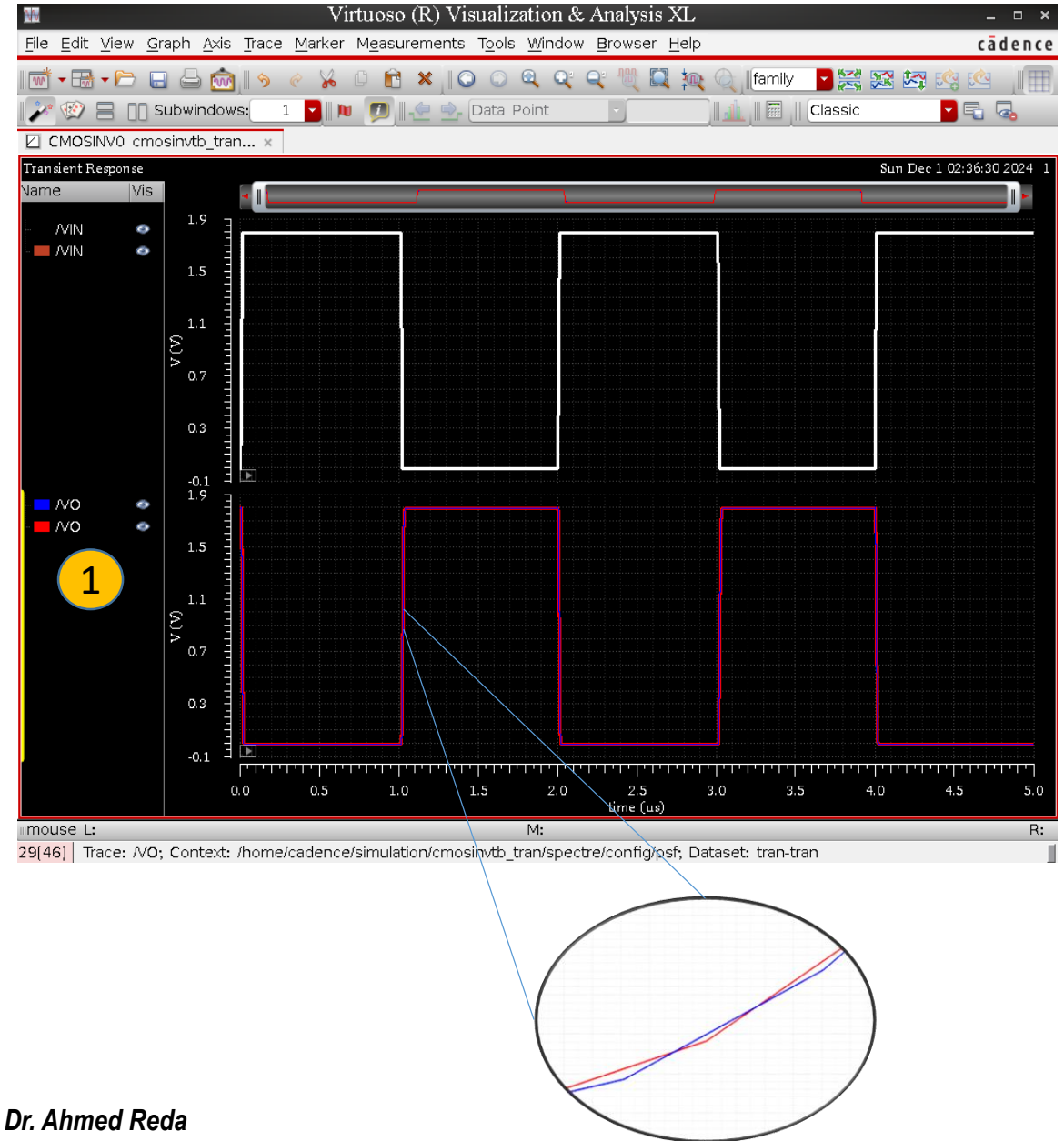

ADE L (9) - CMOSINV0 cmosinvtb_tran config
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cadence
Design Variables
Name Value
1 VDD 1.8
Analyses
Type Enable Arguments
1 tran 0 5u
Outputs
Name/Signal/Expr Value Plot Save
1 VIN
2 VO
3 tr 9.24262n
4 tf 6.33895n
5 tphl 6.25892n
6 tplh 4.51754n
7 tp 5.38823n
4
> Results in /home/cadence/simulation/cmosinvtb_tran/spectre/cor
Plot after simulat Auto Plotting mo Append

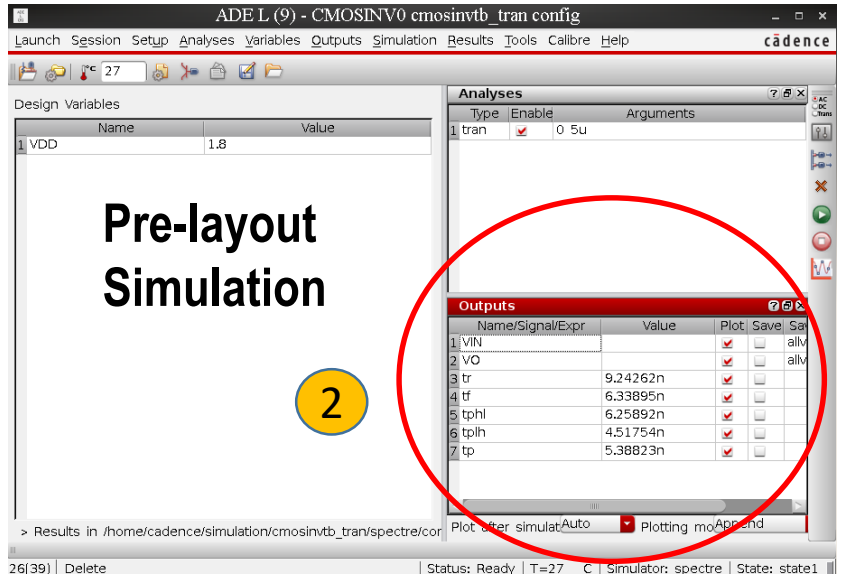
Steps (11/12)

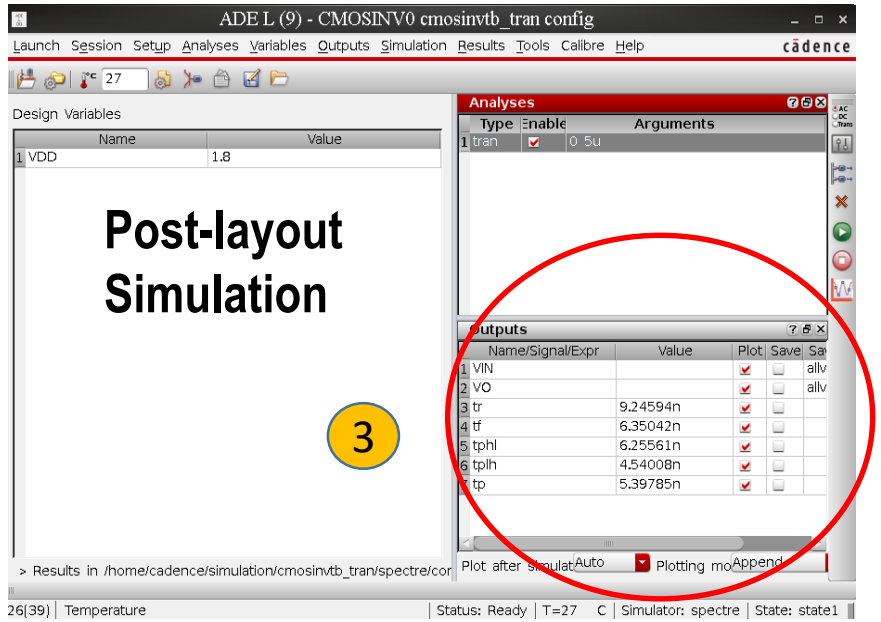

Virtuoso® Hierarchy Editor Editing: (CMOSINV0 cmosinvtb_tran co
File Edit View Plugins Help
cadence
Search
Update Needed
Top Cell
2
Library: CMOSINV0
Cell: cmosinvtb_tran
View: schematic
Open
Edit
ADE L
Global Bindings
Library List: myLib
View List: ga ahdl pspice
Stop List: spectre
Constraint List:
Table View
Tree View
Cell Bindings
1
Library
Cell
View Found
View To Use
nherited View List
CMOSINV0 cmosinvsch calibre calibre spectre cmos_...
CMOSINV0 cmosinvtb_tran schematic spectre cmos_...
analogLib cap spectre spectre cmos_...
analogLib vdc spectre spectre cmos_...
analogLib vpulse spectre spectre cmos_...
tsmc18rf nmos2v spectre spectre cmos_...
tsmc18rf pmos2v spectre spectre cmos_...
Namespace: CDBA Filters: OFF Update: Needed
24(37) >


ADE L (9) - CMOSINV0 cmosinvtb_tran config
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cadence
Design Variables
Name Value
1 VDD 1.8
Analyses
Type Enable Arguments
1 tran 0 5u
3
Outputs
Name/Signal/Expr Value Plot Save
1 VIN
2 VO
3 tr 9.24262n
4 tf 6.33895n
5 tphl 6.25892n
6 tplh 4.51754n
7 tp 5.38823n
> Results in /home/cadence/simulation/cmosinvtb_tran/spectre/cor
Plot after simulat Auto
Plotting mo Append
26(39) Delete
Status: Ready T=27 C Simulator: spectre State: state1

Steps (12/12)


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindows: 1
Data Point
Classic
CMOSINV0 cmosinvtb_tran...
Transient Response
Sun Dec 1 02:36:30 2024 1
Name Vis
/VIN
/VIN
/VO
/VO
1
V (V)
time (us)
mouse L: M: R:
29(46) Trace: /VO; Context: /home/cadence/simulation/cmosinvtb_tran/spectre/config/psf; Dataset: tran-tran

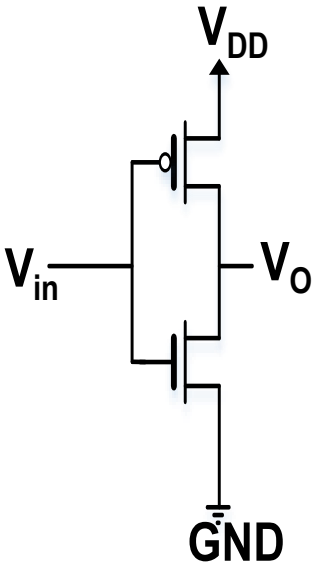

ADE L (9) - CMOSINV0 cmosinvtb_tran config
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cadence
Design Variables
Name Value
1 VDD 1.8
Pre-layout Simulation
2
Analyses
Type Enable Arguments
1 tran 0 5u
Outputs
Name/Signal/Expr Value Plot Save
1 VIN
2 VO
3 tr 9.24262n
4 tf 6.33895n
5 tphl 6.25892n
6 tplh 4.51754n
7 tp 5.38823n
> Results in /home/cadence/simulation/cmosinvtb_tran/spectre/cor
26(39) Delete
Status: Ready T=27 C Simulator: spectre State: state1

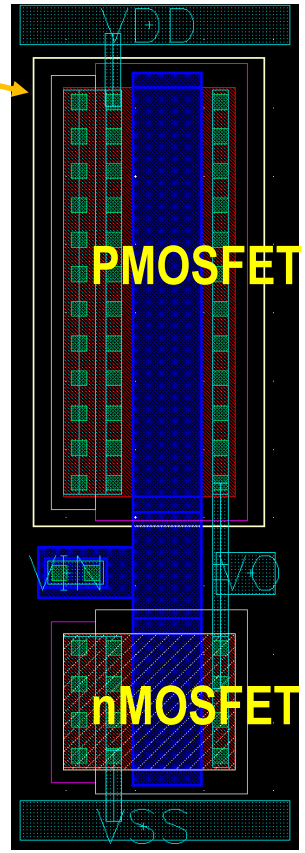

ADE L (9) - CMOSINV0 cmosinvtb_tran config
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cadence
Design Variables
Name Value
1 VDD 1.8
Post-layout Simulation
3
Analyses
Type Enable Arguments
1 tran 0 5u
Outputs
Name/Signal/Expr Value Plot Save
1 VIN
2 VO
3 tr 9.24594n
4 tf 6.35042n
5 tphl 6.25561n
6 tplh 4.54008n
7 tp 5.39785n
> Results in /home/cadence/simulation/cmosinvtb_tran/spectre/cor
26(39) Temperature
Status: Ready T=27 C Simulator: spectre State: state1

Outlines

- ❑ Analog IC Design Flow
- ❑ Cadence Steps
- ❑ Conclusion

Conclusion

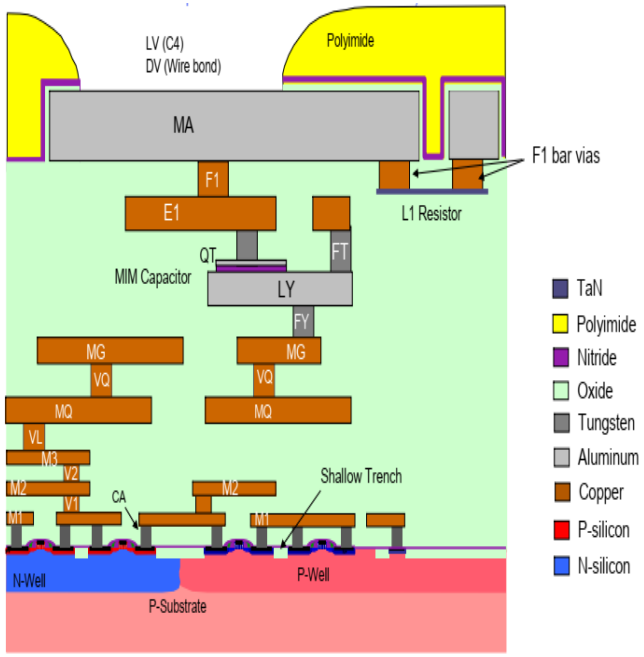




DRC Clean

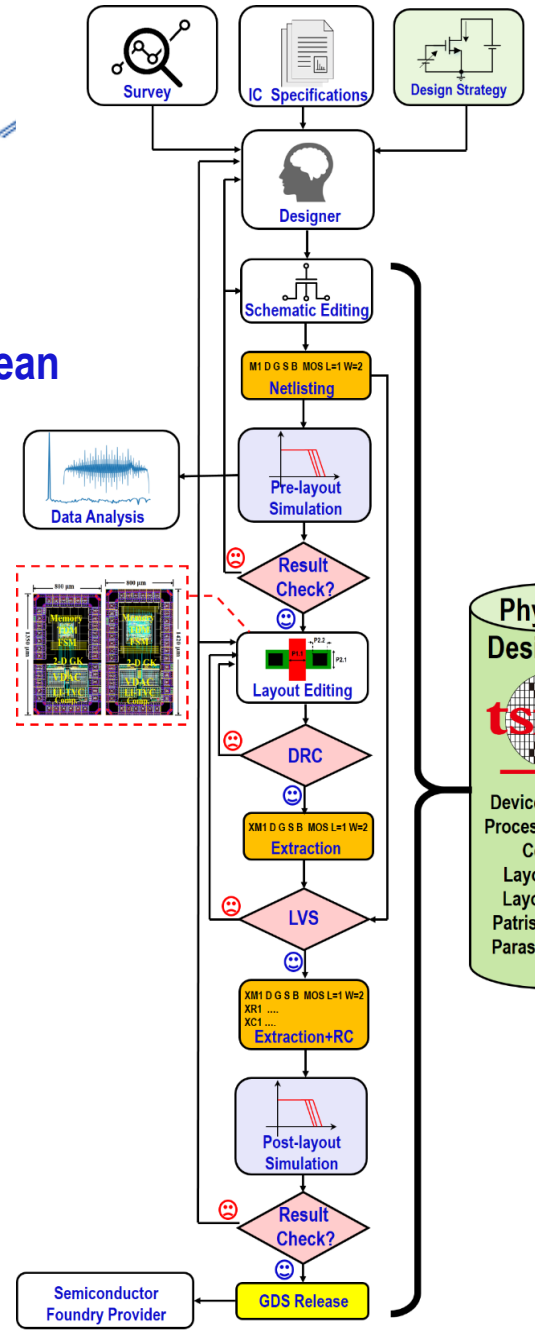
LVS Clean

PEX Clean



Process Cross-Section

8 layers



Analog IC design flow

Thanks!