Digital Design (SET111)
L12
FSM and Counter

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Outlines

- ❑ Finite State Machine
- ❑ Asynchronous Counter
- ❑ Synchronous Counter
- ❑ Design of Synchronous Counters
- ❑ Exersice_01
- ❑ Exersice_02
- ❑ Exersice_03
- ❑ Exersice_04

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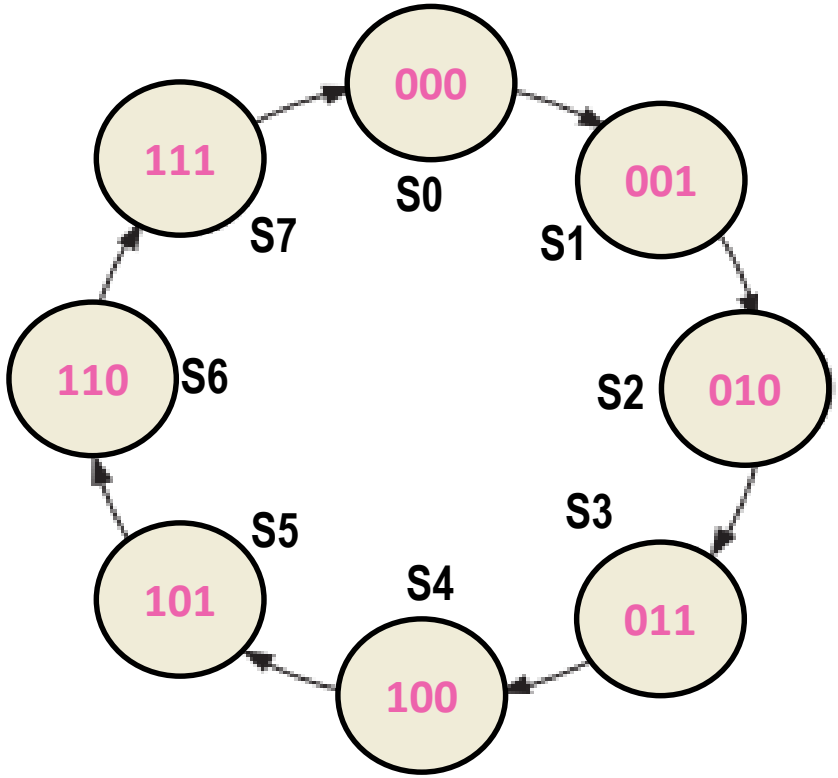
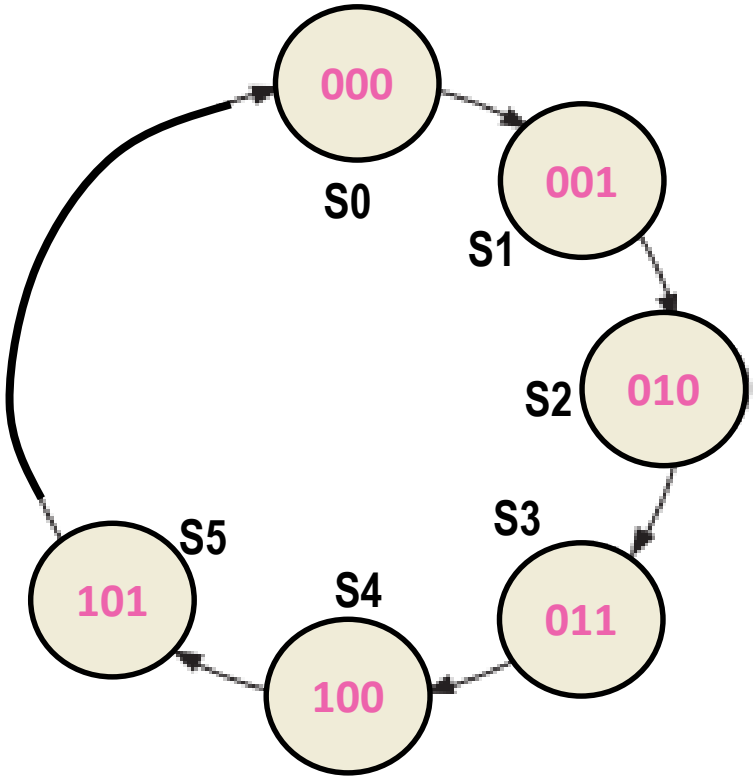
- ❑ Exersice_04

Finite State Machine

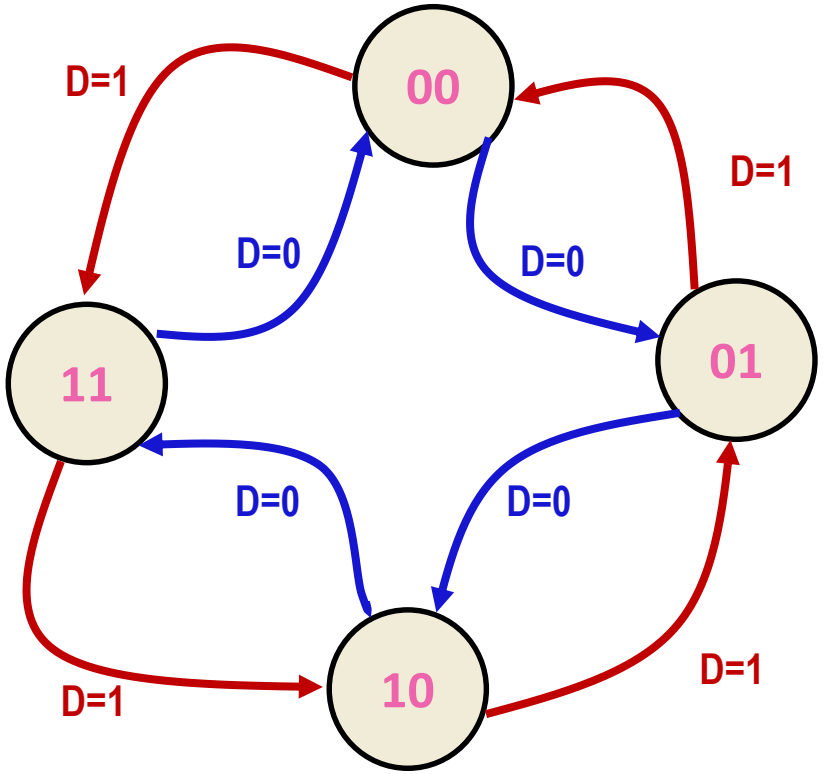
- A **state machine** is a sequential circuit having a limited (**finite**) number of states occurring in a prescribed **order**, so it is called Finite State Machine (**FSM**).
- A **counter** is an example of a state machine, the number of states is called the ***modulus***
- Two basic types of counters are the **Asynchronous** and **Synchronous** counter.



State Diagram
MOD-8 FSM



State Diagram
MOD-6 FSM



State Diagram
MOD-4 FSM

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- Finite State Machine
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- Exersice_02
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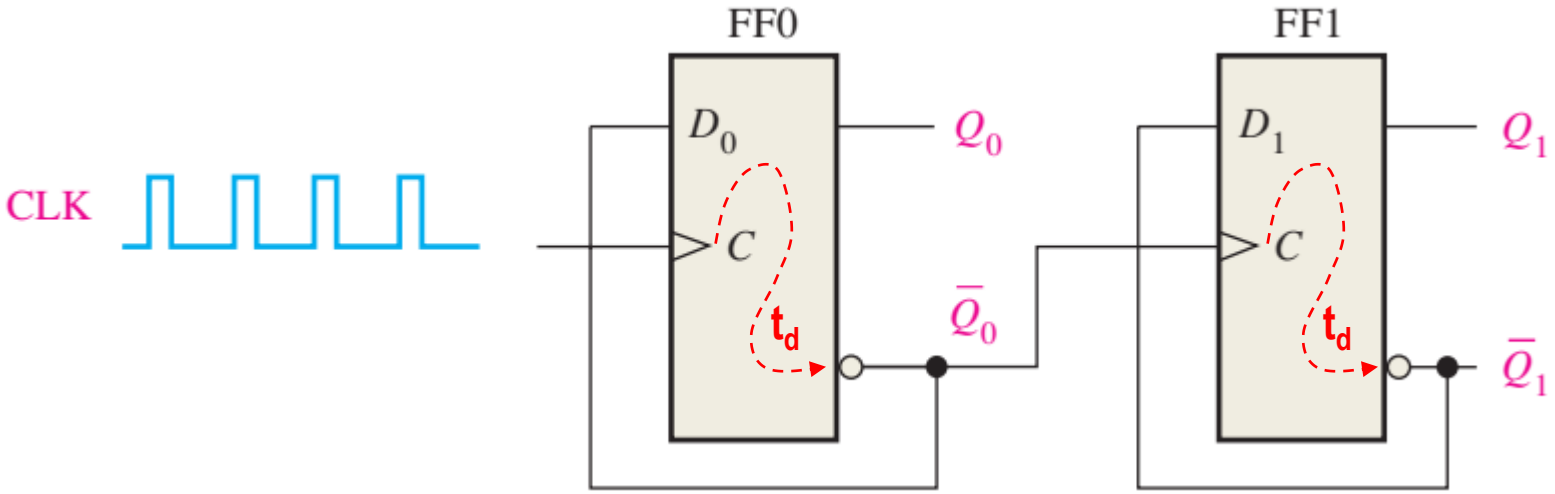
- Exersice_04

Asynchronous Counter

- The term **asynchronous** refers to events that **do not occur at the same time.**
- An **asynchronous counter** is one in which the flip-flops (FF) within the counter **do not change states** at exactly the same time because they **do not have a common clock pulse**.



A 2-Bit Asynchronous Binary Counter

The clock input of an asynchronous counter is always connected only to the LSB flip-flop

- Notice that the clock (CLK) is applied to the clock input (*C*) of ***only* the first flip-flop**, FF0, which is always the least significant bit (LSB). The second flip-flop, FF1, is triggered by the $\overline{Q_0}$ output of FF0.
- Because of the inherent propagation delay time (**td**) through a flip-flop, a transition of the input clock pulse (CLK) and a transition of the $\overline{Q_0}$ output of FF0 can never occur at exactly the same time.

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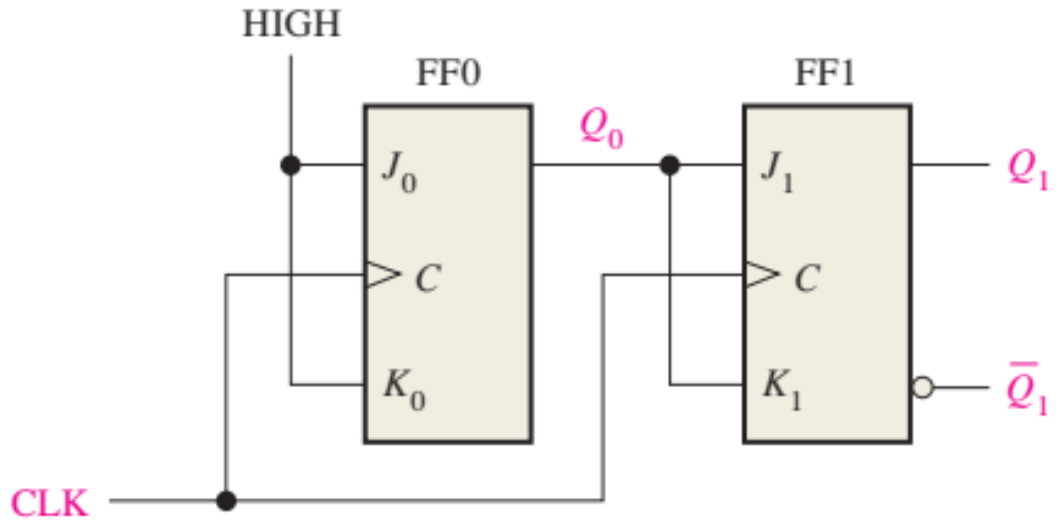
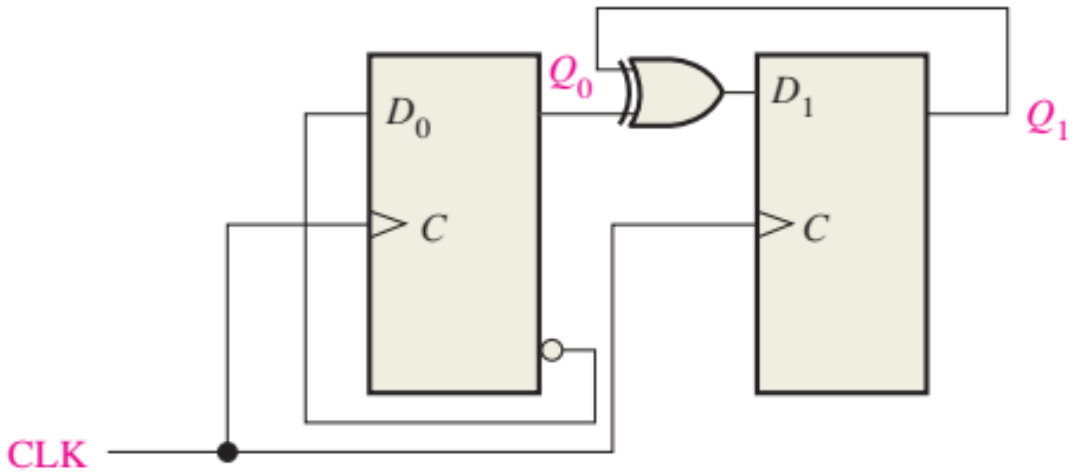
Synchronous Counter (1/4)

- The term **synchronous** refers to events that **occurs at the same time.**
- An **synchronous counter** is one in which the flip-flops (FF) within the counter changes states at exactly the same time because all the flip-flops in the counter are clocked by a **common clock pulse**.



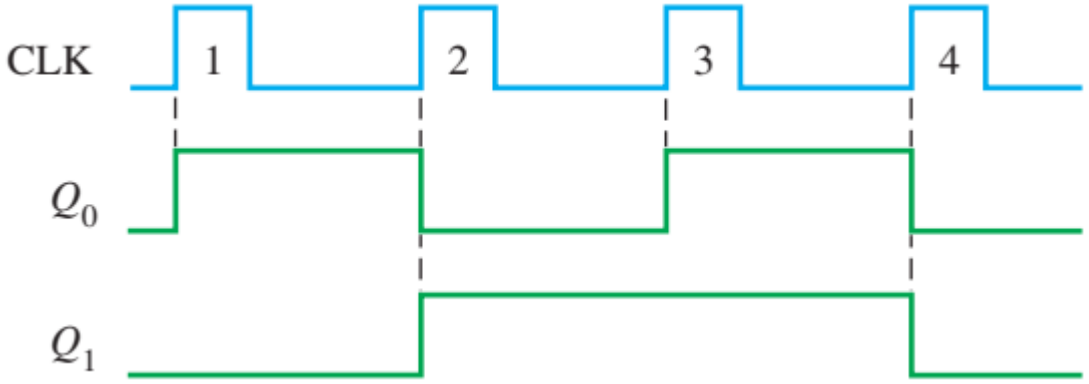
A 2-Bit Synchronous Binary Counter using (JK Flip Flop)

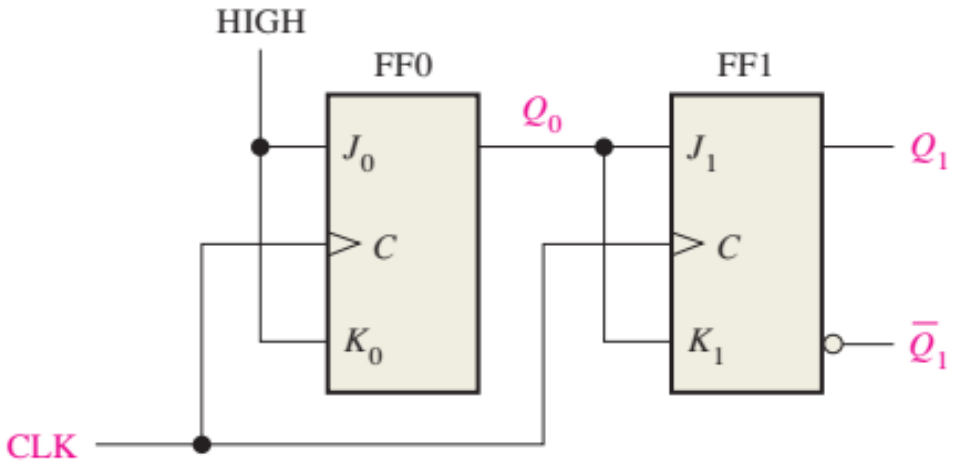


A 2-Bit Synchronous Binary Counter using (D-Flip Flop)

- J-K flip-flops are used to illustrate most synchronous counters.
- D flip-flops can also be used but generally require **more logic** because of having no direct toggle or no-change states.

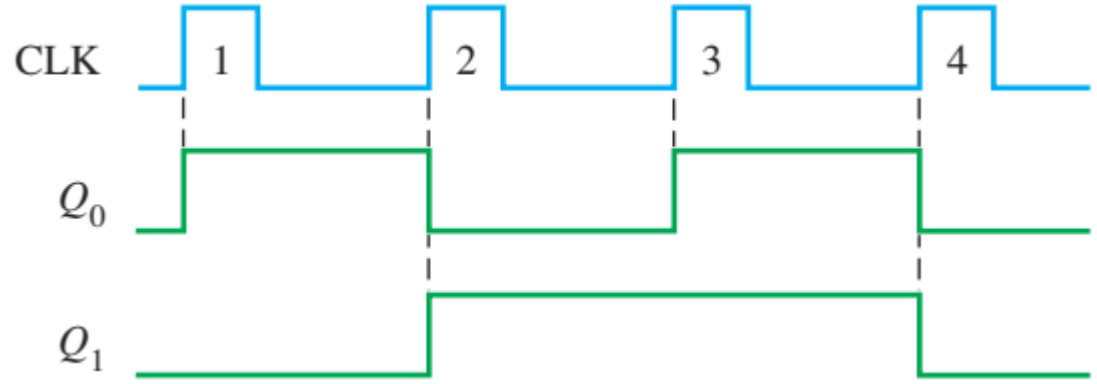
Synchronous Counter (2/4)

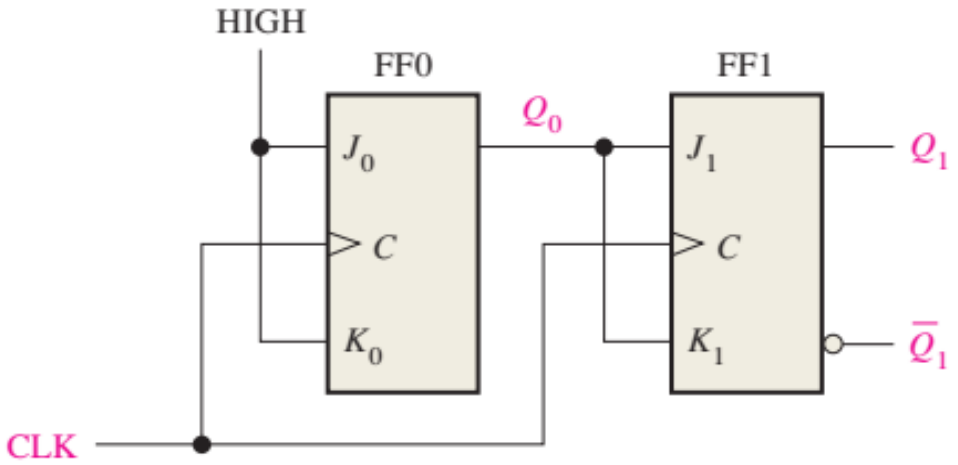




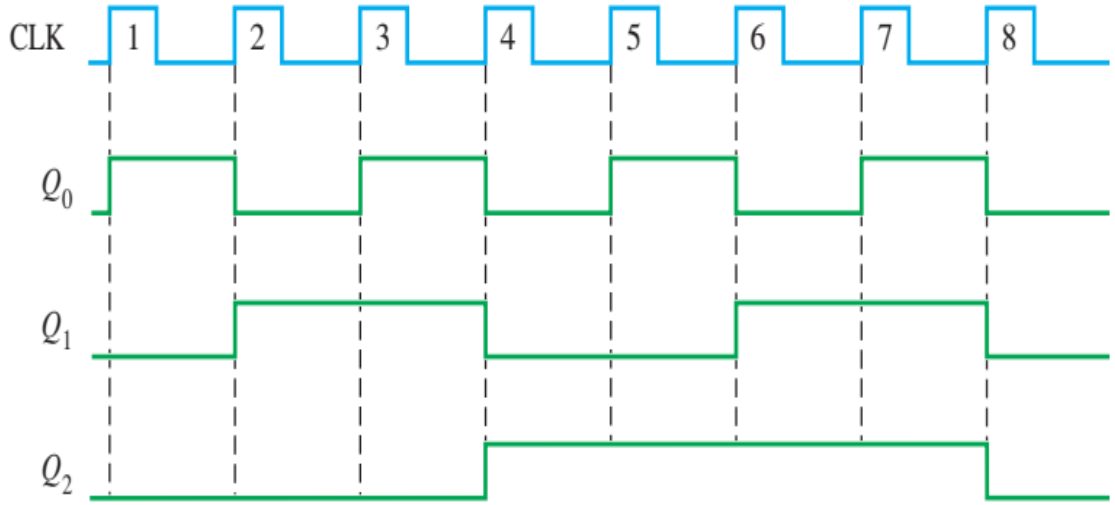
A 2-Bit Synchronous Binary Counter using (JK Flip Flop)

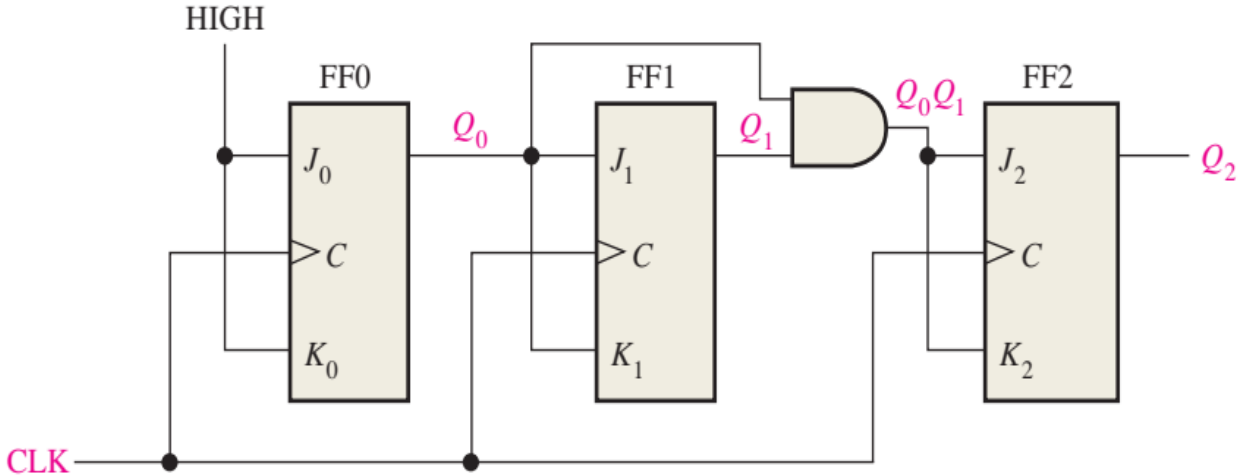
Synchronous Counter (3/4)





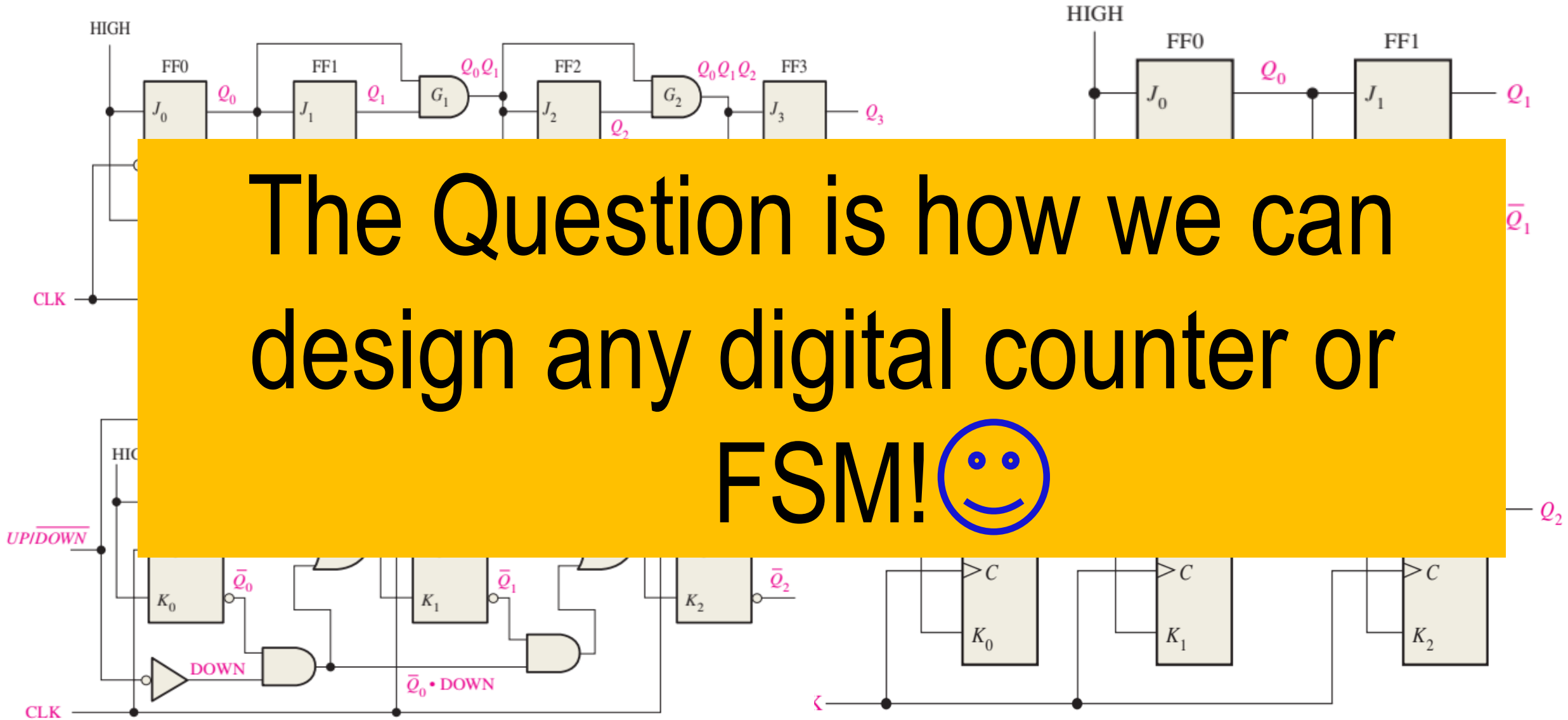
A 2-Bit Synchronous Binary Counter using (JK Flip Flop)





A 3-Bit Synchronous Binary Counter using (JK Flip Flop)

Synchronous Counter (4/4)



The Question is how we can design any digital counter or FSM!☺

Up/Down 3-Bit Synchronous Binary Counter

A 3-Bit Synchronous Binary Counter using

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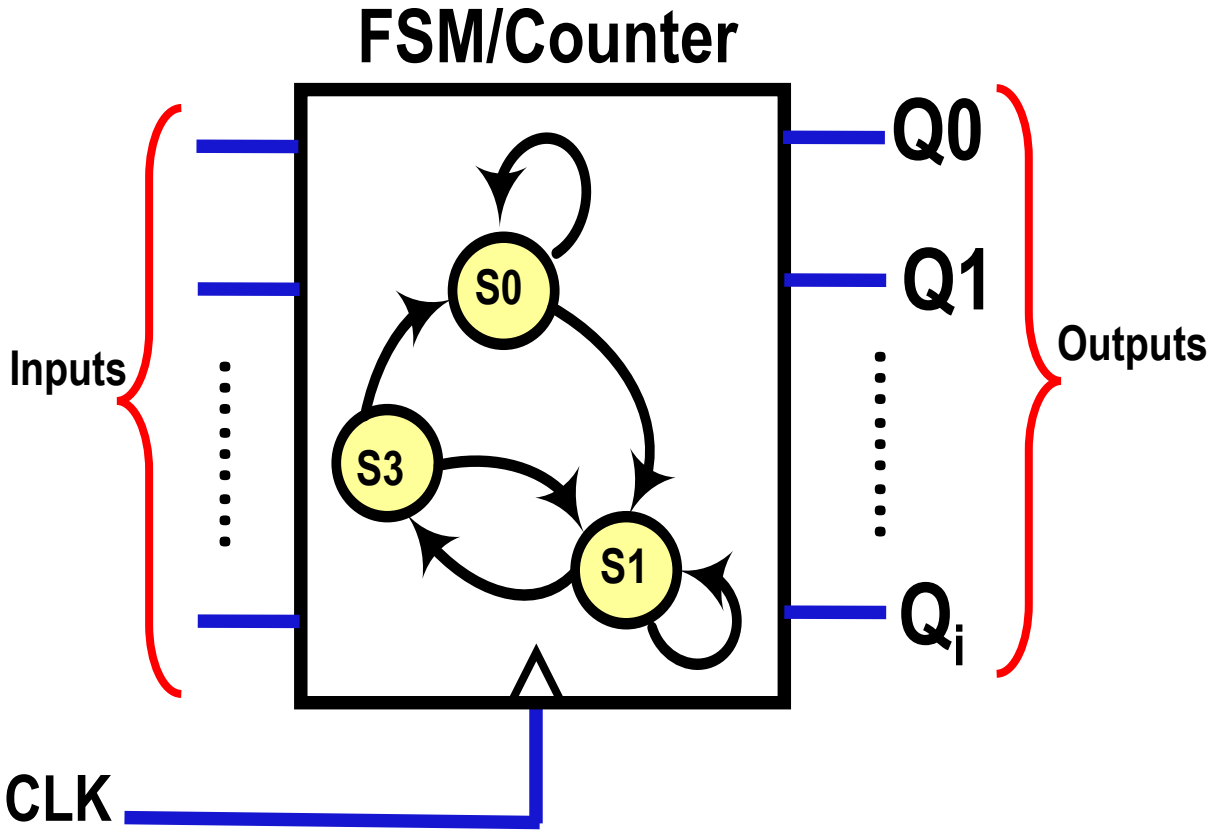
Design of Synchronous Counters

- You have to execute **Five** steps to design a **counter** Or even any finite state machine (**FSM**).

- **Step 1:** State Diagram
- **Step 2:** Next-State Table
- **Step 3:** Flip-Flop Transition Table
- **Step 4:** K-Maps
- **Step 5:** Counter Implementation



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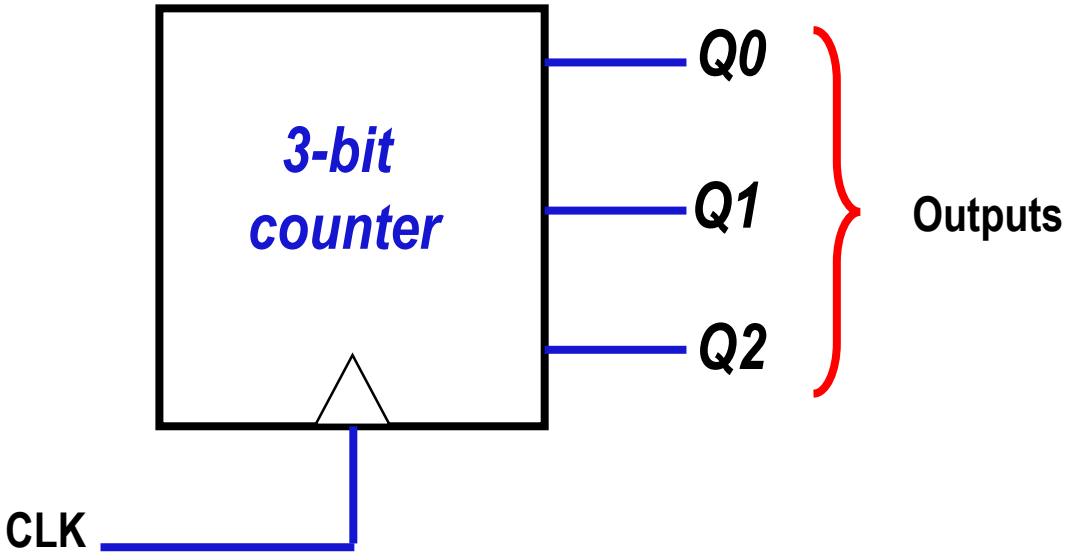
Exersice_01

- Design a 3-bit **synchronous up counter** using **JK Flip-Flop.**

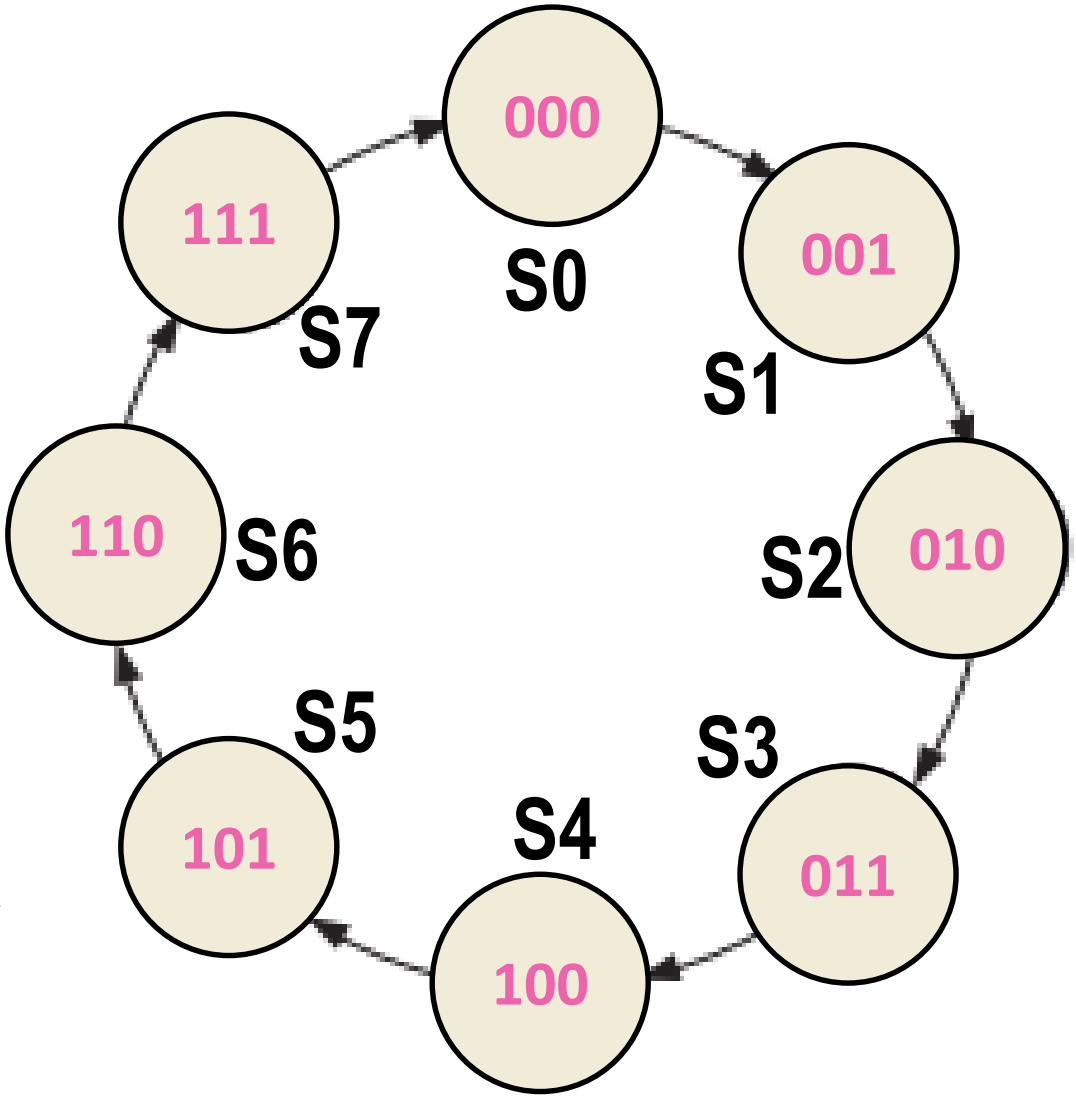
Ans.



Exersice_01

❑Step 1: State Diagram

3-bit synchronous→ 2^3 =8 states
Up counter→ {0,1,2,3,4,5,6,7}



State Diagram
3-bit counter

Exersice_01

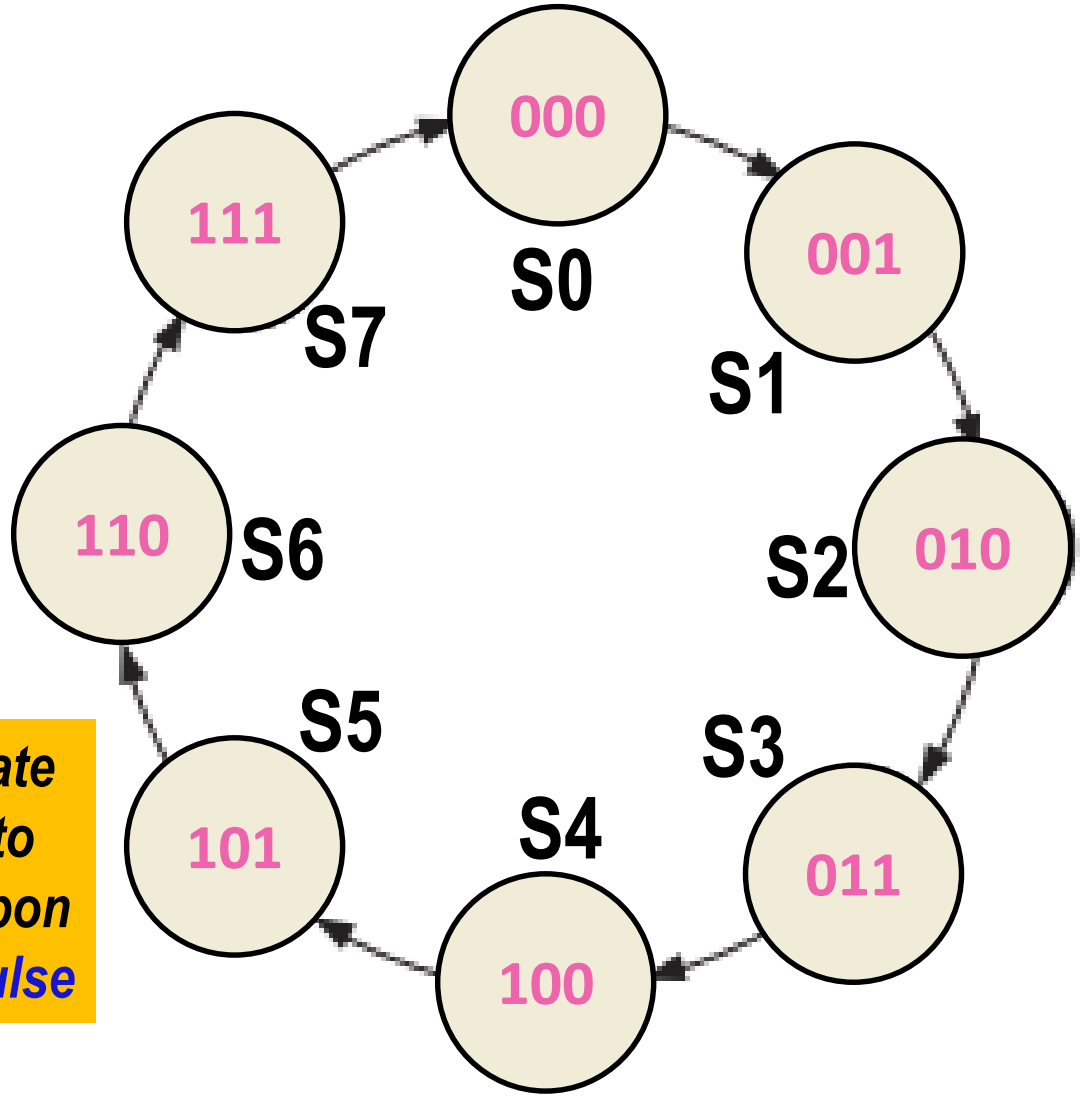
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table for 3-bit counter

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0

The next state is the state that the counter goes to from its present state upon application of a clock pulse



Exersice_01

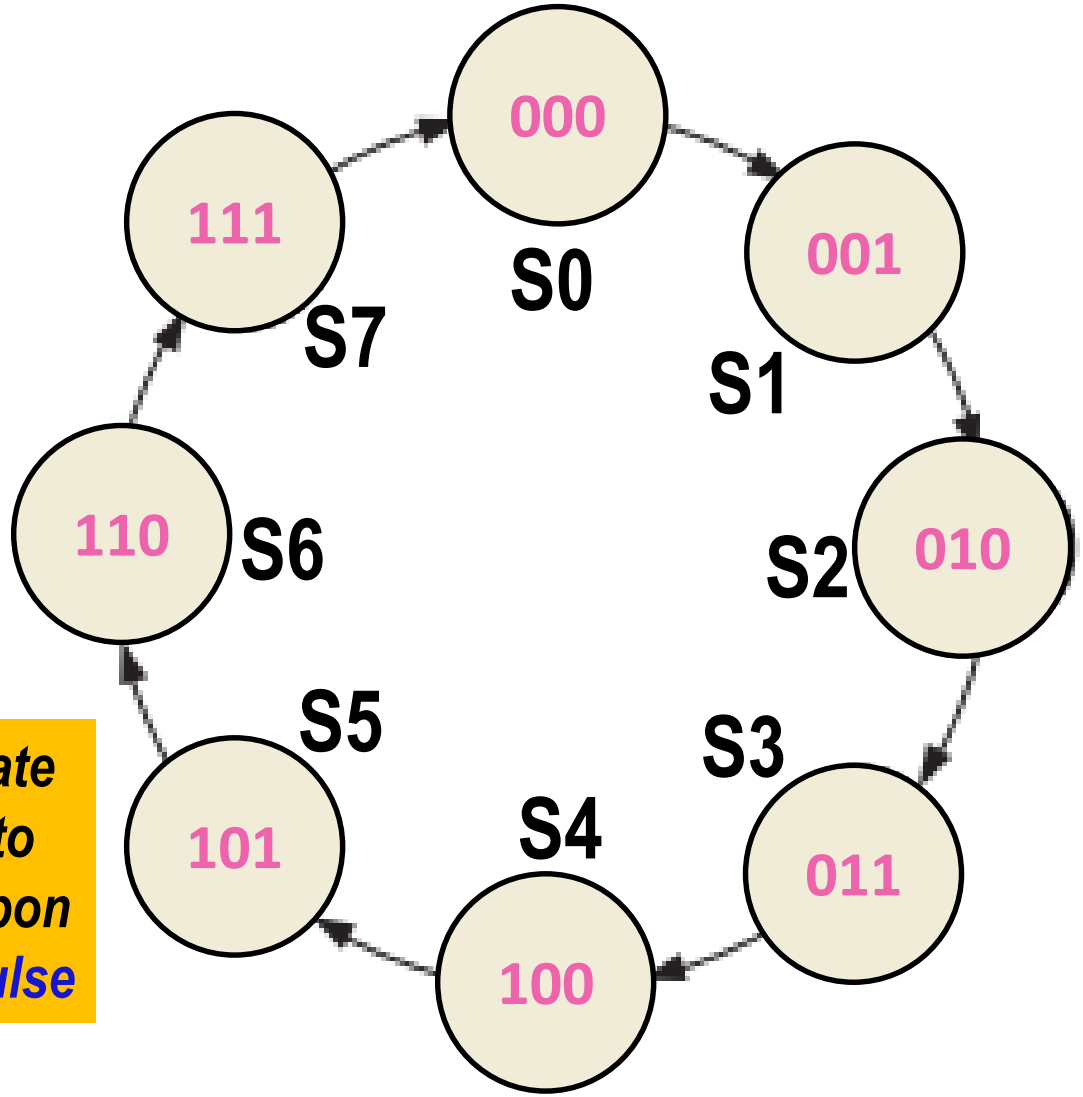
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table for 3-bit counter

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

The next state is the state that the counter goes to from its present state upon application of a clock pulse



Exersice_01

❑Step 3: Flip-Flop Transition Table

❑For each output transition, the J and K inputs that will cause the output transition to occur are always the same and defined in table.

Next-state table for 3-bit counter

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_01

❑Step 3: Flip-Flop Transition Table

❑# of JK Flip-Flop = # of output of the counter. Here, # of JK Flip-Flop=3.

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1						
0	0	1	0	1	0						
0	1	0	0	1	1						
0	1	1	1	0	0						
1	0	0	1	0	1						
1	0	1	1	1	0						
1	1	0	1	1	1						
1	1	1	0	0	0						

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_01

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for 3-bit counter

Present State		Next State		Inputs of the JK-Flip Flop		
[redacted]	Q0	[redacted]	Q0	[redacted]	J0	K0
	0		1			
	1		0			
	0		1			
	1		0			
	0		1			
	1		0			
	0		1			
	1		0			

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
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❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for 3-bit counter

Present State		Next State		Inputs of the JK-Flip Flop	
[redacted]	Q0	[redacted]	Q0	J0	K0
	0		1	1	X
	1		0	X	1
	0		1	1	X
	1		0	X	1
	0		1	1	X
	1		0	X	1
	0		1	1	X
	1		0	X	1

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_01

❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table for 3-bit counter

Present State		Next State		Inputs of the JK-Flip Flop	
	Q1		Q1	J1	K1
	0		0		
	0		1		
	1		1		
	1		0		
	0		0		
	0		1		
	1		1		
	1		0		

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_01

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for 3-bit counter

Present State	Next State	Inputs of the JK-Flip Flop	
Q1	Q1	J1	K1
0	0	0	X
0	1	1	X
1	1	X	0
1	0	X	1
0	0	0	X
0	1	1	X
1	1	X	0
1	0	X	1

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_01

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for 3-bit counter

Present State		Next State		Inputs of the JK-Flip Flop		
Q2		Q2		J2	K2	
0		0				
0		0				
0		0				
0		1				
1		1				
1		1				
1		1				
1		0				

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_01

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for 3-bit counter

Present State		Next State		Inputs of the JK-Flip Flop		
Q2	[redacted]	Q2	[redacted]	J2	K2	[redacted]
0		0		0	X	
0		0		0	X	
0		0		0	X	
0		1		1	X	
1		1		X	0	
1		1		X	0	
1		1		X	0	
1		0		X	1	

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_01

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

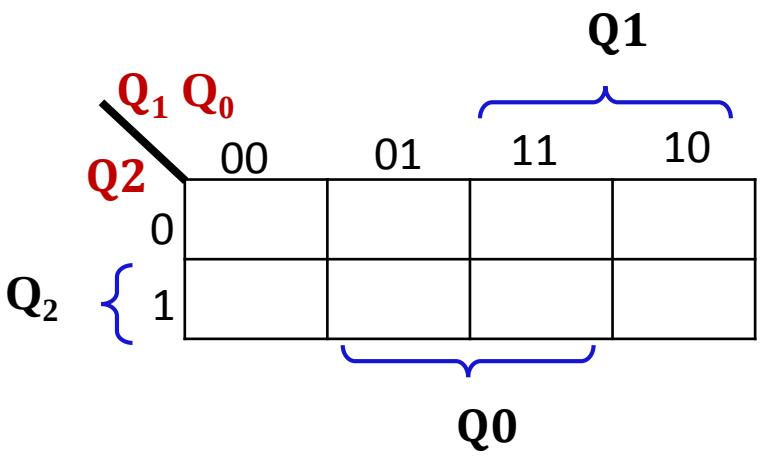
Exersice_01

❑Step 4: k-Maps

❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

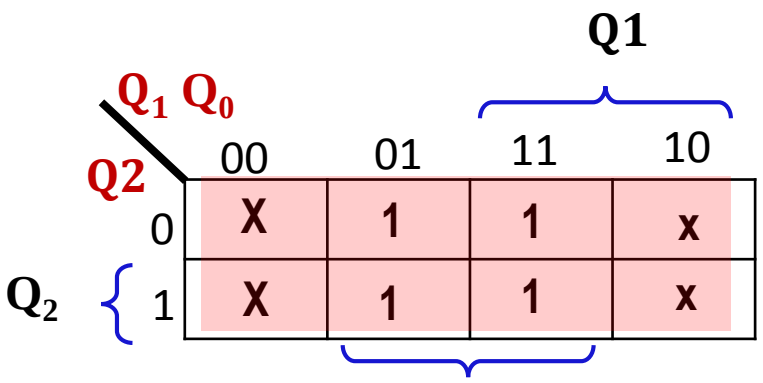


Exersice_01

- Step 4: k-Maps
  - K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1



$K_0=1$

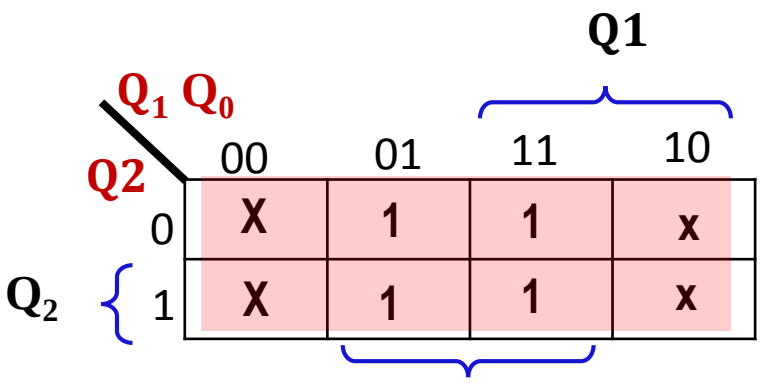
Exersice_01

❑Step 4: k-Maps

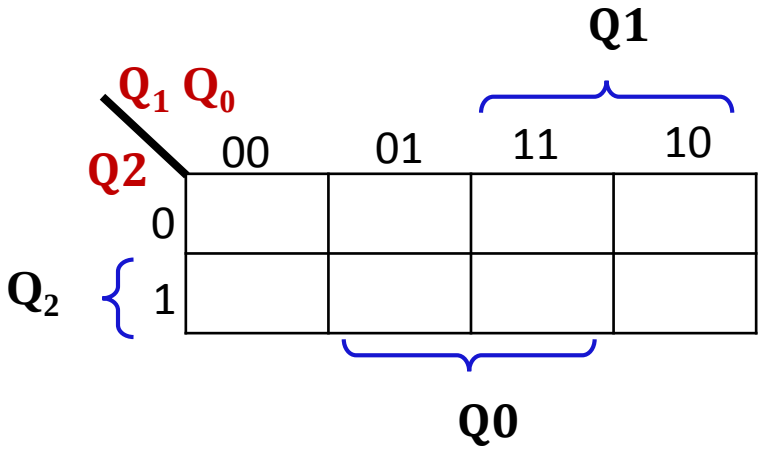
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1



$K_0=1$



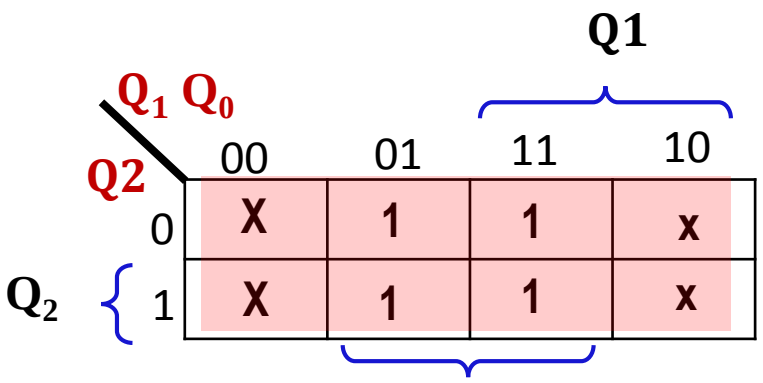
Exersice_01

❑Step 4: k-Maps

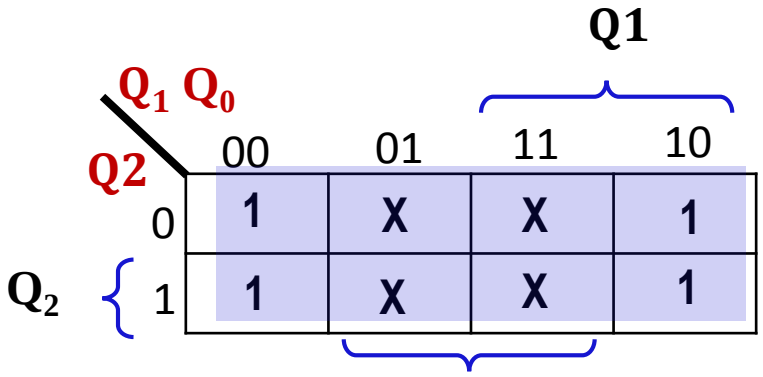
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1



$K_0=1$



$J_0=1$

Exersice_01

❑Step 4: k-Maps

❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

Q1

Q_2 \ $Q_1 Q_0$	00	01	11	10
0	X	X	1	0
1	X	X	1	0

Q0

$K_1=Q_0$

Q1

Q_2 \ $Q_1 Q_0$	00	01	11	10
0	0	1	X	X
1	0	1	X	X

Q0

$J_1=Q0$

Exersice_01

❑Step 4: k-Maps

❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for 3-bit counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

Q1

Q_2 \ $Q_1 Q_0$	00	01	11	10
0	X	X	X	X
1	0	0	1	0

Q0

$K_2 = Q_0.Q1$

Q1

Q_2 \ $Q_1 Q_0$	00	01	11	10
0	0	0	1	0
1	x	x	X	X

Q0

$J_2 = Q_0.Q1$

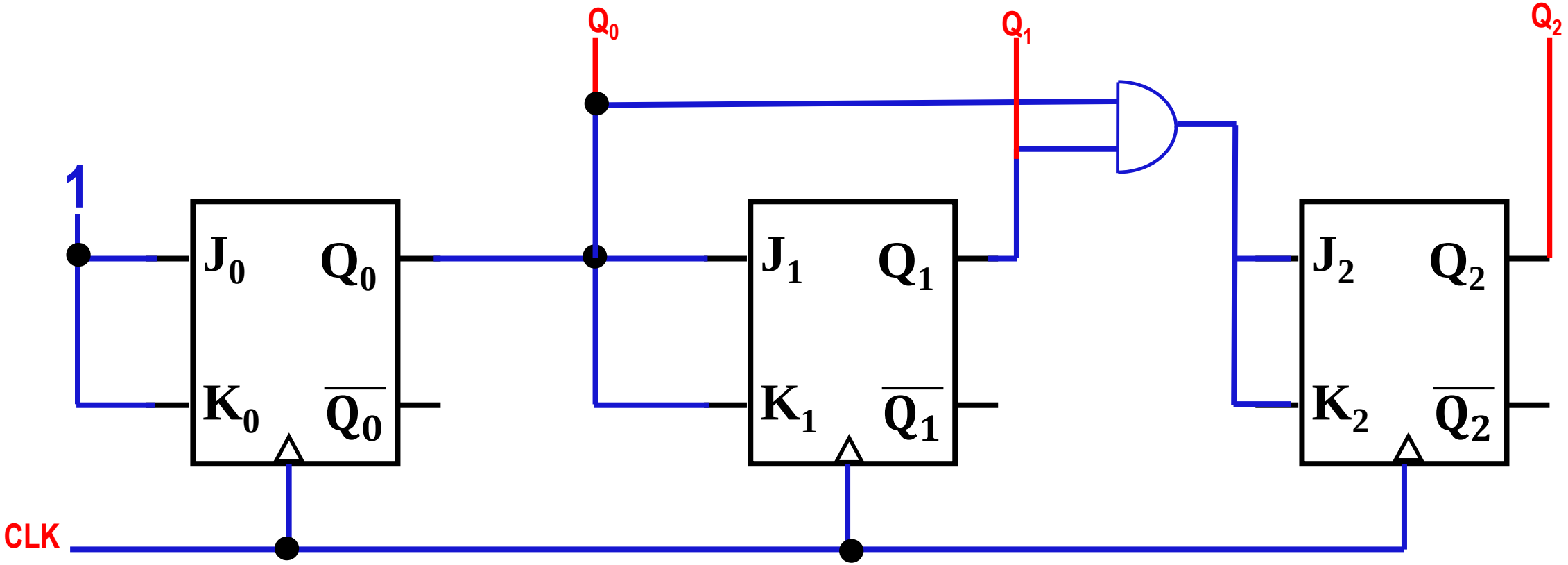
Exersice_01

❑Step 5: Counter implementation

❑The final step is to implement the combinational logic from the expressions for the *J* and *K* inputs

$J_0=1$ $J_1=Q_0$ $J_2=Q_0 . Q1$

$K_0=1$ $K_1=Q_0$ $K_2=Q_0 . Q1$



Outlines

- ❑ Finite State Machine
- ❑ Asynchronous Counter
- ❑ Synchronous Counter
- ❑ Design of Synchronous Counters
- ❑ Exersice_01
- ❑ Exersice_02
- ❑ Exersice_03
- ❑ Exersice_04

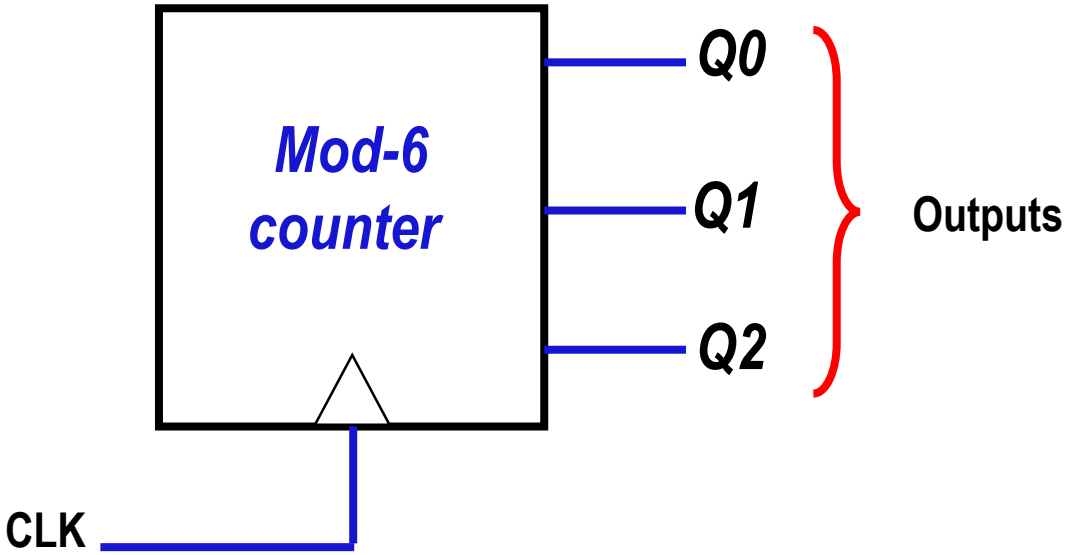
Exersice_02

❑Design a **Mod-6 synchronous up Counter** using JK flip flops.

Ans.

Mod-6 synchronous→ 6 states

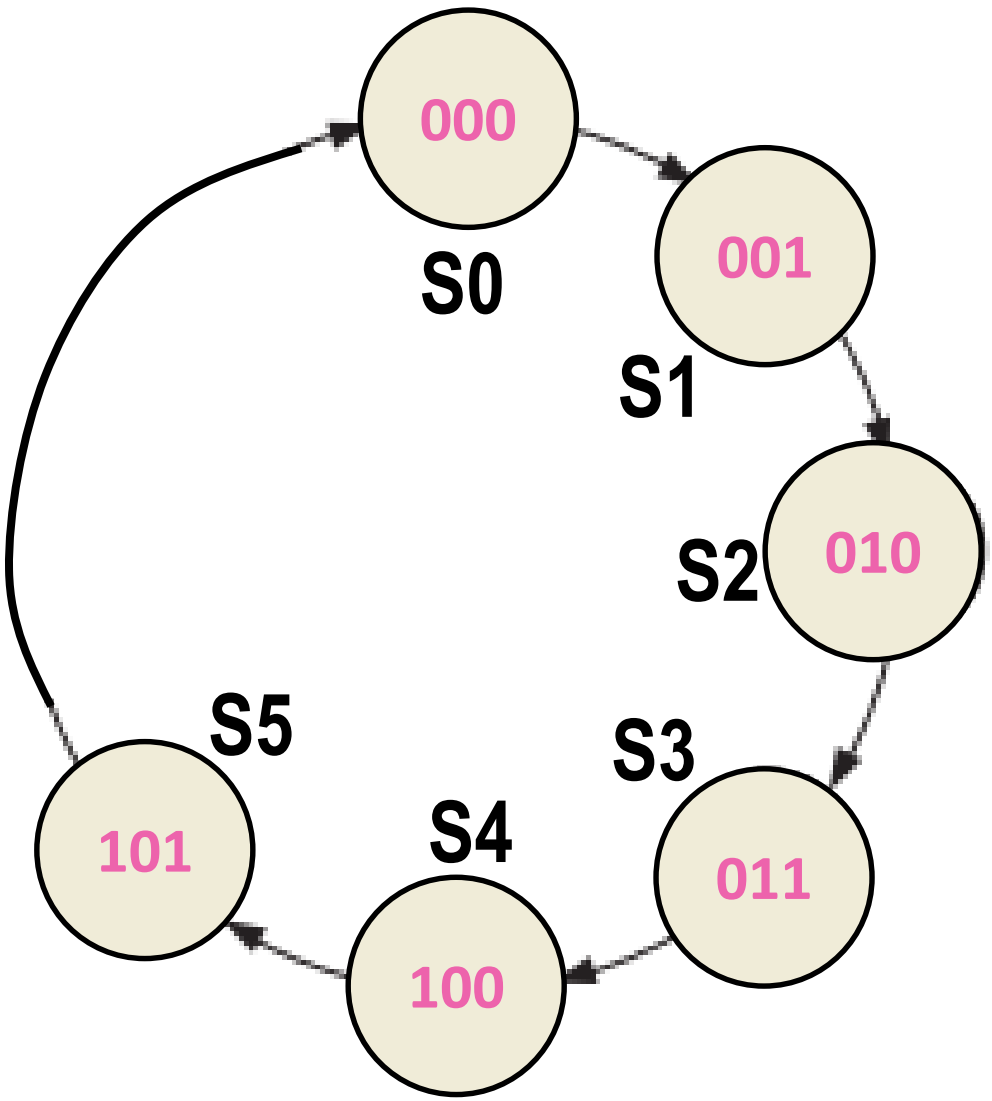
Mod-6 synchronous→ needs 3 outputs



Exersice_02

❑Step 1: State Diagram

Mod-6 synchronous → 6 states
Up counter→ {0,1,2,3,4,5}



State Diagram
Mod-6 counter

Exersice_02

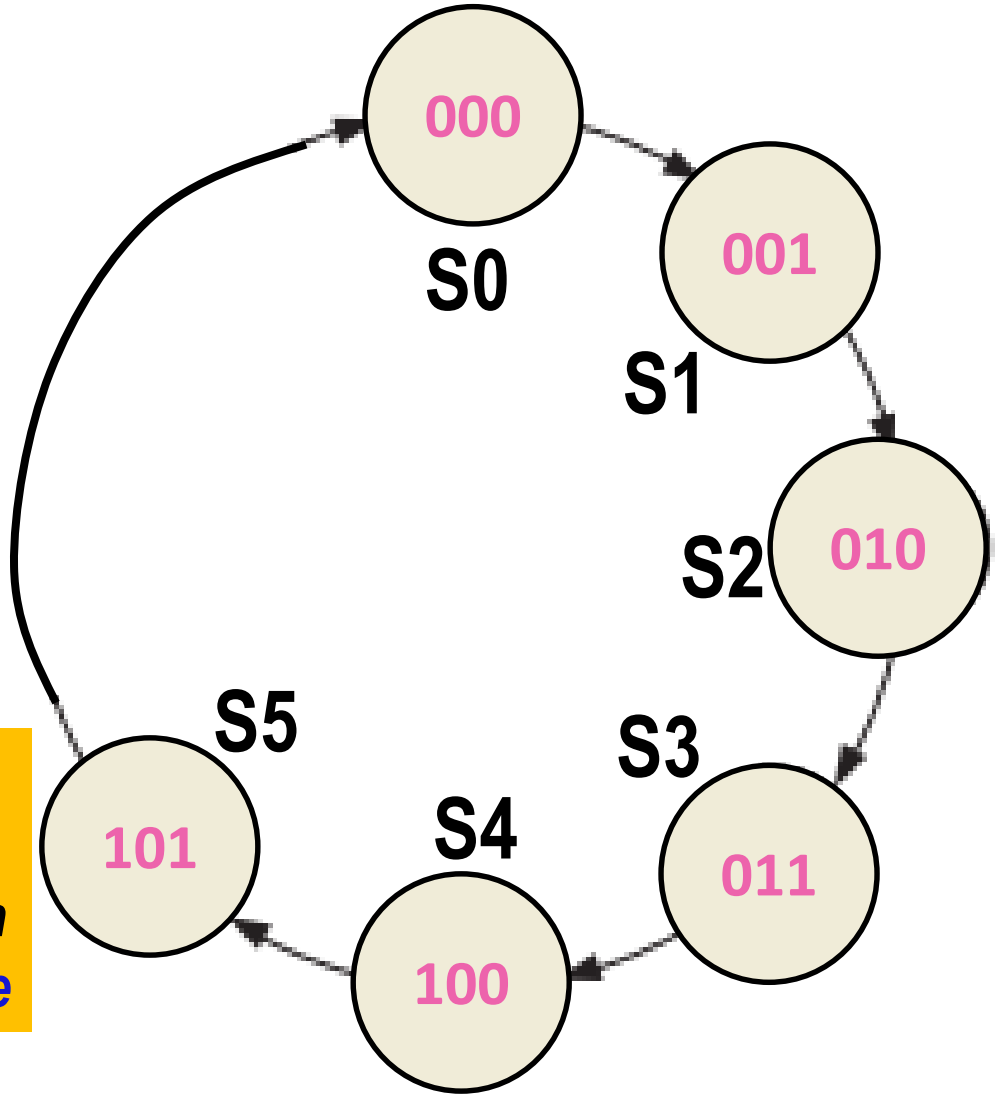
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table for Mod-6 counter

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0

The next state is the state that the counter goes to from its present state upon application of a clock pulse



Exersice_02

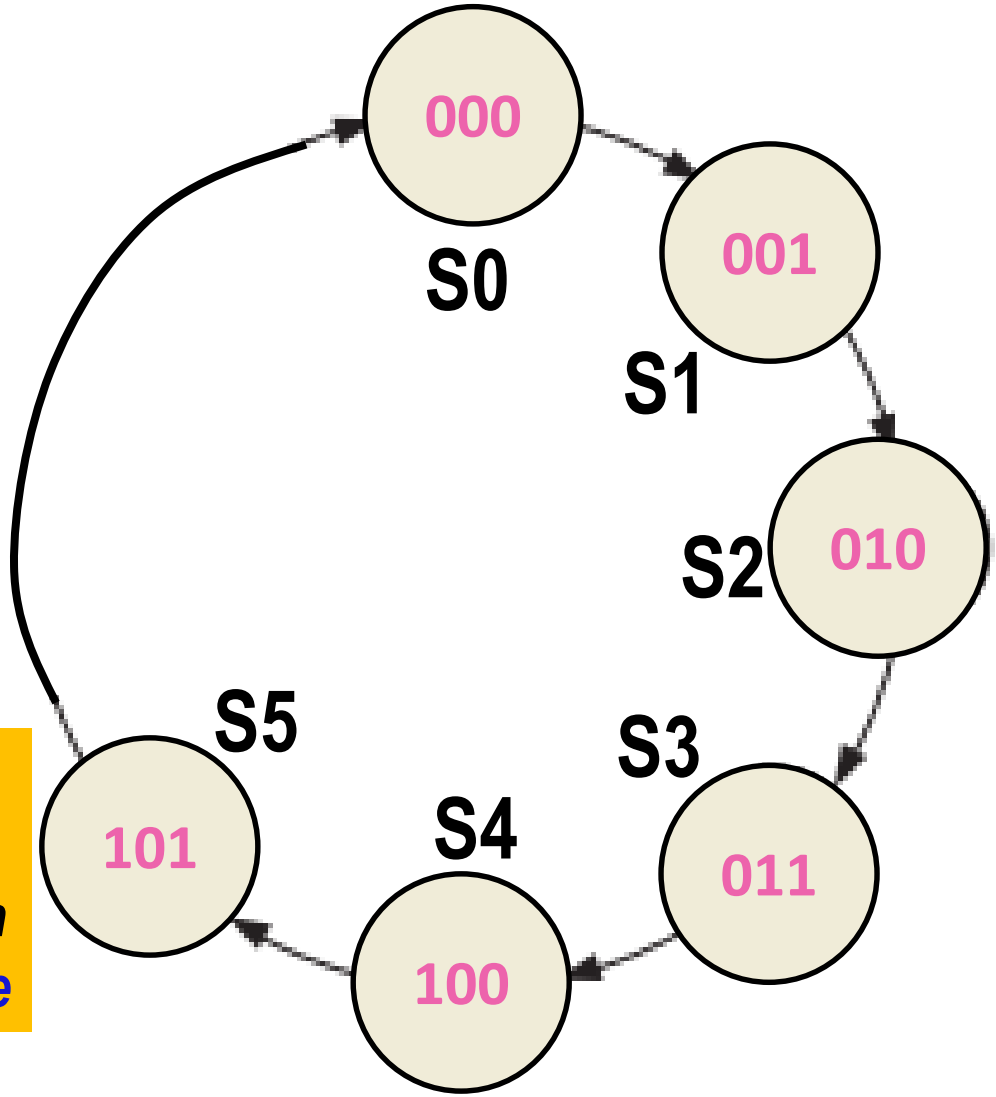
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table for Mod-6 counter

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	X	X	X
1	1	1	X	X	X

The next state is the state that the counter goes to from its present state upon application of a clock pulse



Exersice_02

❑Step 3: Flip-Flop Transition Table

❑For each output transition, the J and K inputs that will cause the output transition to occur are always the same and defined in table.

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	X	X	X
1	1	1	X	X	X

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑# of JK Flip-Flop = # of output of the counter. Here, # of JK Flip-Flop=3.

Next-state table for Mod-6 counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1						
0	0	1	0	1	0						
0	1	0	0	1	1						
0	1	1	1	0	0						
1	0	0	1	0	1						
1	0	1	0	0	0						
1	1	0	X	X	X						
1	1	1	X	X	X						

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for Mod-6 counter

Present State		Next State		Inputs of the JK-Flip Flop		
	Q0		Q0		J0	K0
	0		1			
	1		0			
	0		1			
	1		0			
	0		1			
	1		0			
	0		X			
	1		X			

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for Mod-6 counter

Present State		Next State		Inputs of the JK-Flip Flop	
	Q0		Q0	J0	K0
	0		1	1	X
	1		0	X	1
	0		1	1	X
	1		0	X	1
	0		1	1	X
	1		0	X	1
	0		X	X	X
	1		X	X	X

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for Mod-6 counter

Present State	Next State	Inputs of the JK-Flip Flop	
Q1	Q1	J1	K1
0	0		
0	1		
1	1		
1	0		
0	0		
0	0		
1	X		
1	X		

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table for Mod-6 counter

Present State	Next State	Inputs of the JK-Flip Flop	
Q1	Q1	J1	K1
0	0	0	X
0	1	1	X
1	1	X	0
1	0	X	1
0	0	0	X
0	0	0	X
1	X	X	X
1	X	X	X

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table for Mod-6 counter

Present State			Next State		Inputs of the JK-Flip Flop		
Q2			Q2		J2	K2	
0			0				
0			0				
0			0				
0			1				
1			1				
1			0				
1			X				
1			X				

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table for Mod-6 counter

Present State			Next State		Inputs of the JK-Flip Flop		
Q2			Q2		J2	K2	
0			0		0	X	
0			0		0	X	
0			0		0	X	
0			1		1	X	
1			1		X	0	
1			0		X	1	
1			X		X	X	
1			X		X	X	

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_02

❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table for Mod-6 counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

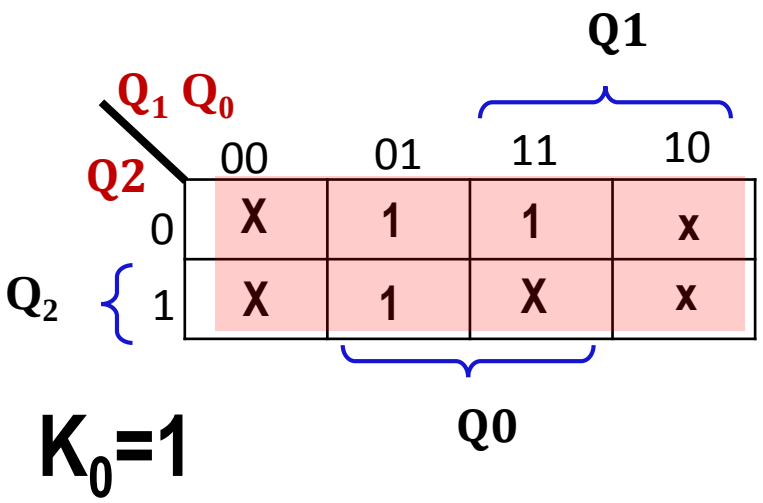
Exersice_02

❑Step 4: k-Maps

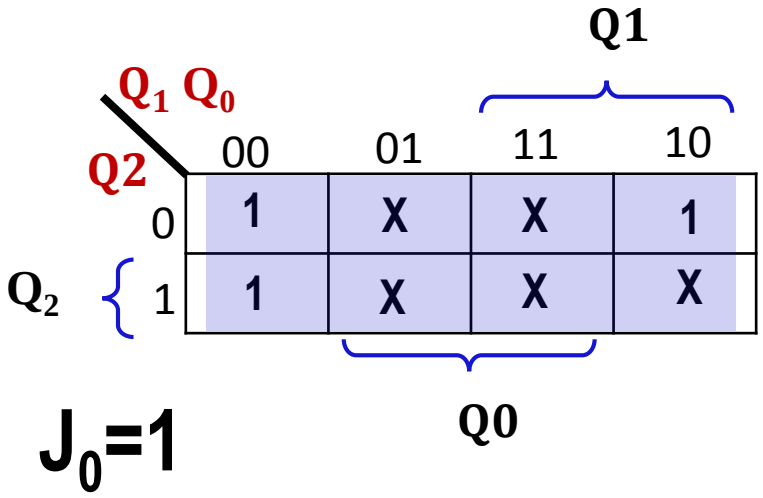
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for Mod-6 counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X



$K_0=1$



$J_0=1$

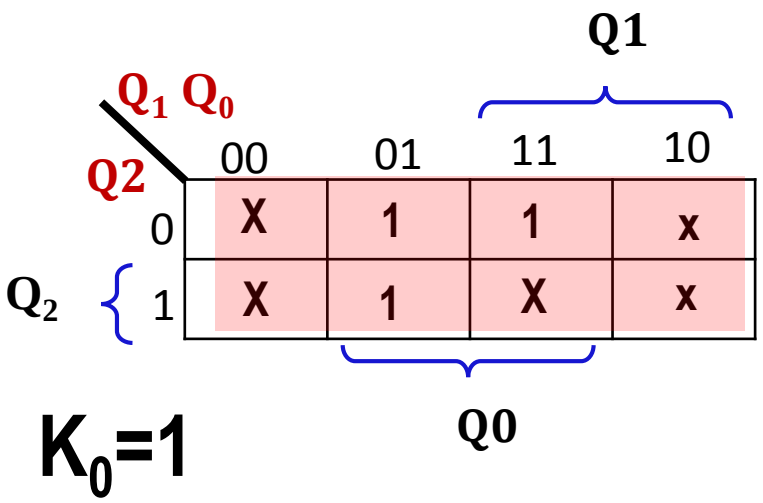
Exersice_02

❑Step 4: k-Maps

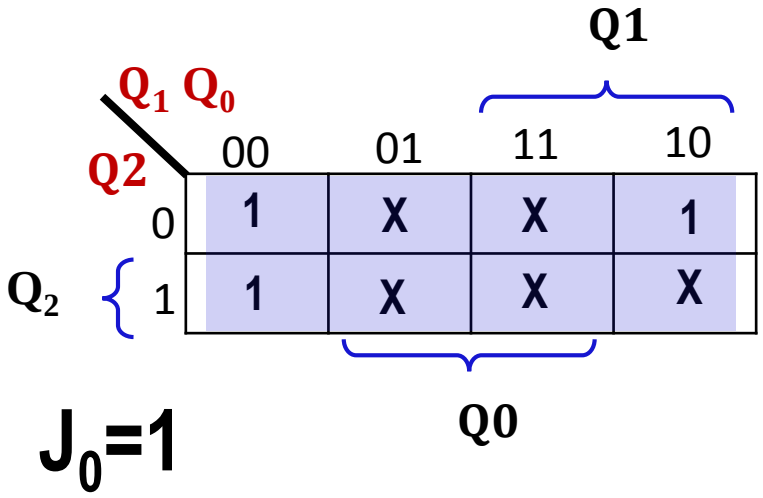
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for Mod-6 counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X



$K_0=1$



$J_0=1$

Exersice_02

❑Step 4: k-Maps

❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for Mod-6 counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Q1

Q_2 \ $Q_1 Q_0$	00	01	11	10
0	X	X	1	0
1	X	X	X	0

Q0

$K_1=Q_0$

Q1

Q_2 \ $Q_1 Q_0$	00	01	11	10
0	0	1	X	X
1	0	0	X	X

Q0

$J_1=Q_0.\overline{Q_2}$

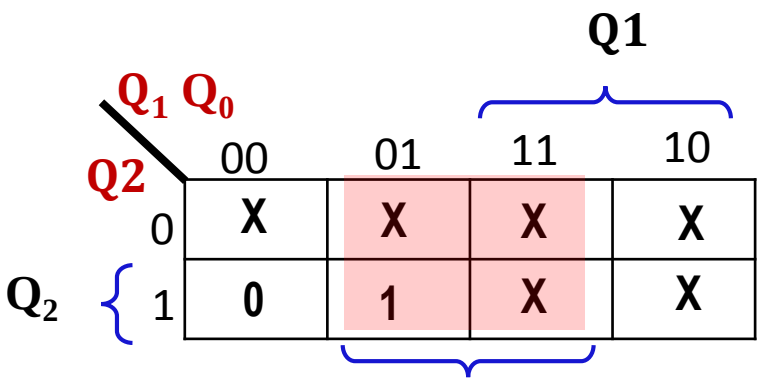
Exersice_02

❑Step 4: k-Maps

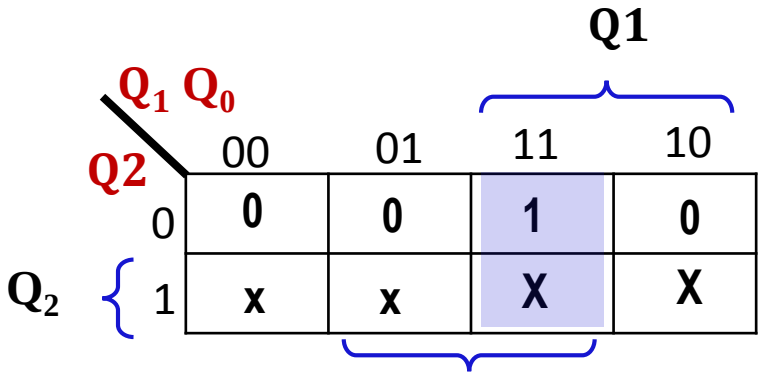
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table for Mod-6 counter

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X



$K_2=Q_0.$



$J_2=Q_0.\ Q1$

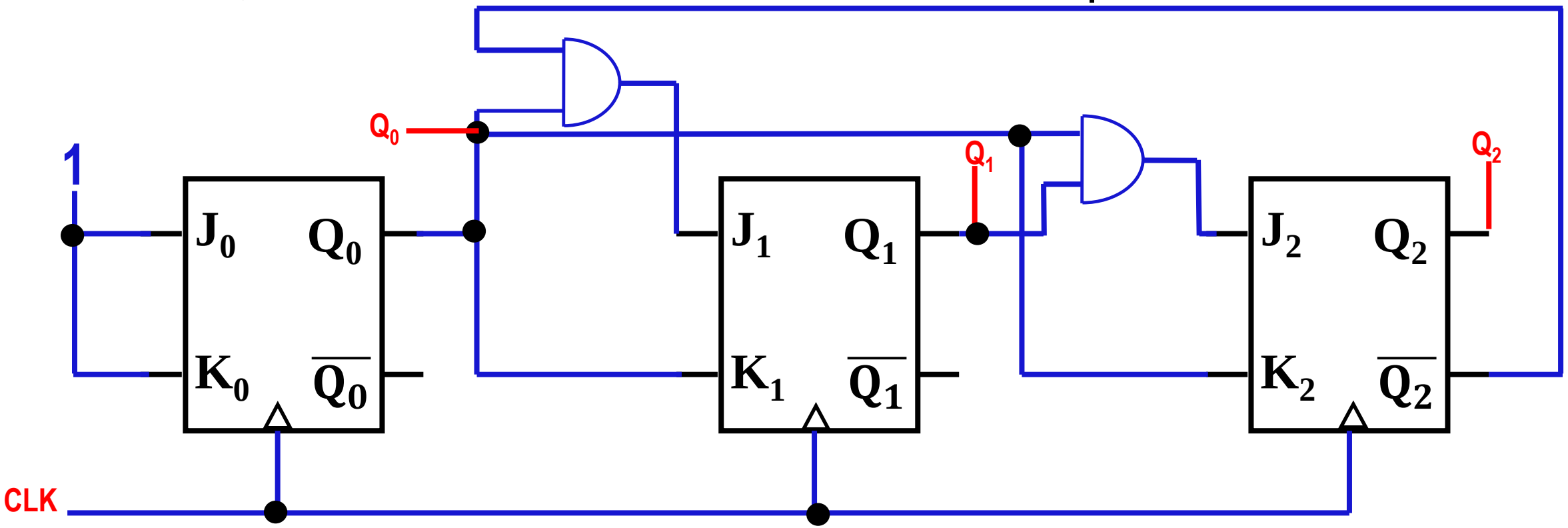
Exersice_02

❑Step 5: Counter implementation

❑The final step is to implement the combinational logic from the expressions for the *J* and *K* inputs

$J_0=1$ $\quad$ $J_1=Q_0.\overline{Q_2}$ $\quad$ $J_2=Q_0.\ Q1$

$K_0=1$ $\quad$ $K_1=Q_0$ $\quad$ $K_2=Q_0$



Outlines

- Finite State Machine
- Asynchronous Counter
- Synchronous Counter
- Design of Synchronous Counters
- Exersice_01
- Exersice_02
- Exersice_03
- Exersice_04

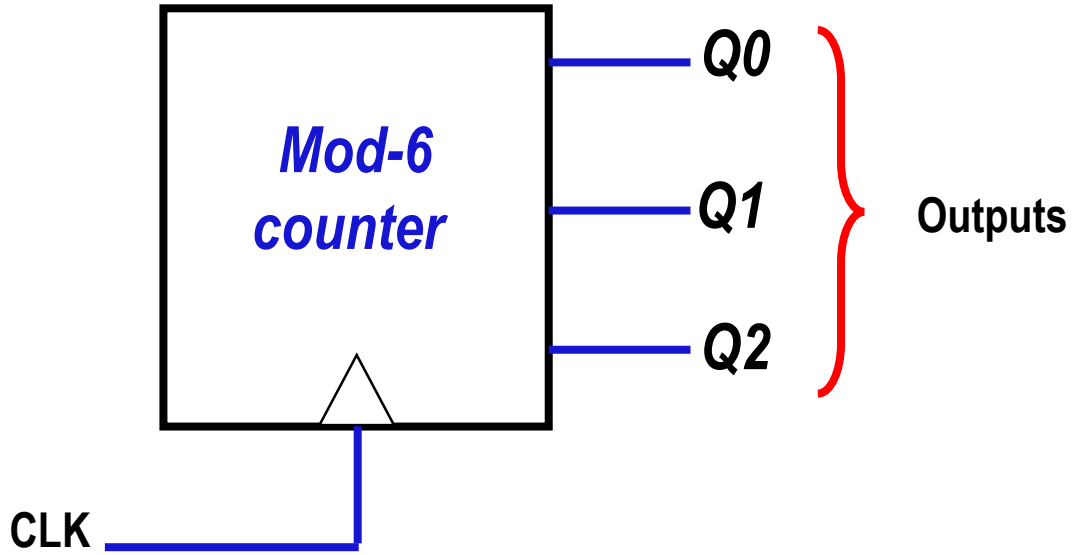
Exersice_03

- Design a synchronous counter with counting sequence: 000, 001, 011, 111, 110, 100, 000,…using JK flip flops.

Ans.

Mod-6 synchronous→ 6 states

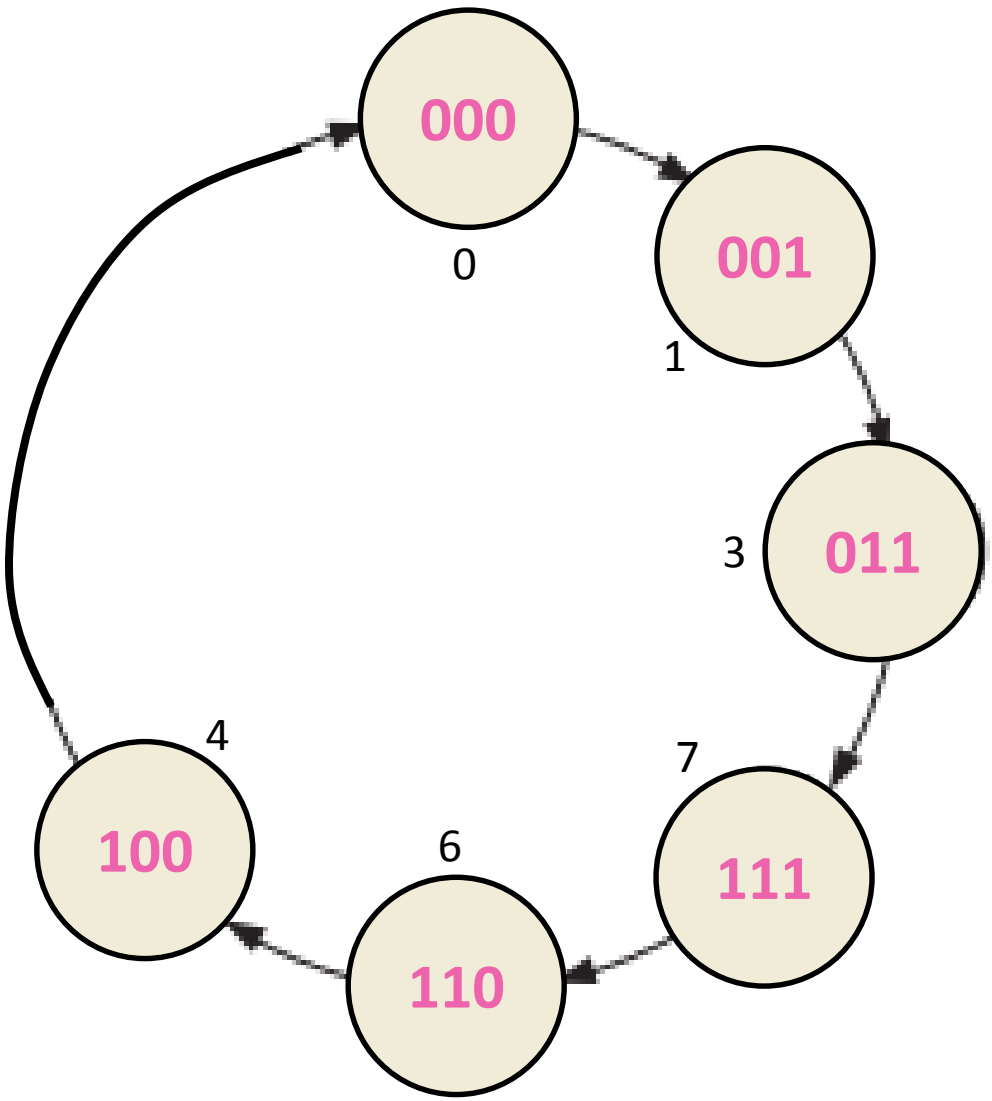
Mod-6 synchronous→ needs 3 outputs



Exersice_03

❑Step 1: State Diagram

Mod-6 synchronous → 6 states
Up counter→ {0,1,3,7,6,4}



State Diagram
Mod-6 counter

Exersice_03

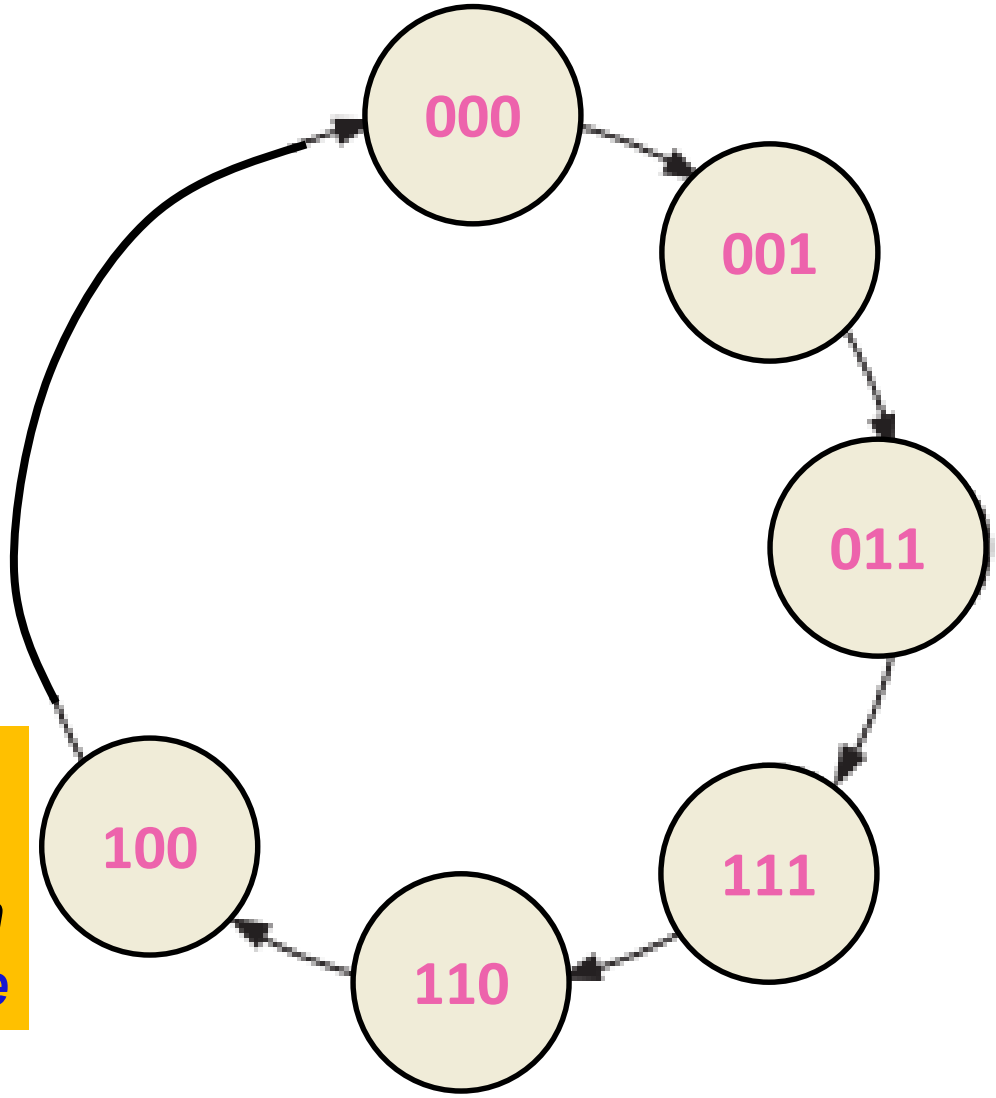
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0

The next state is the state that the counter goes to from its present state upon application of a clock pulse



Exersice_03

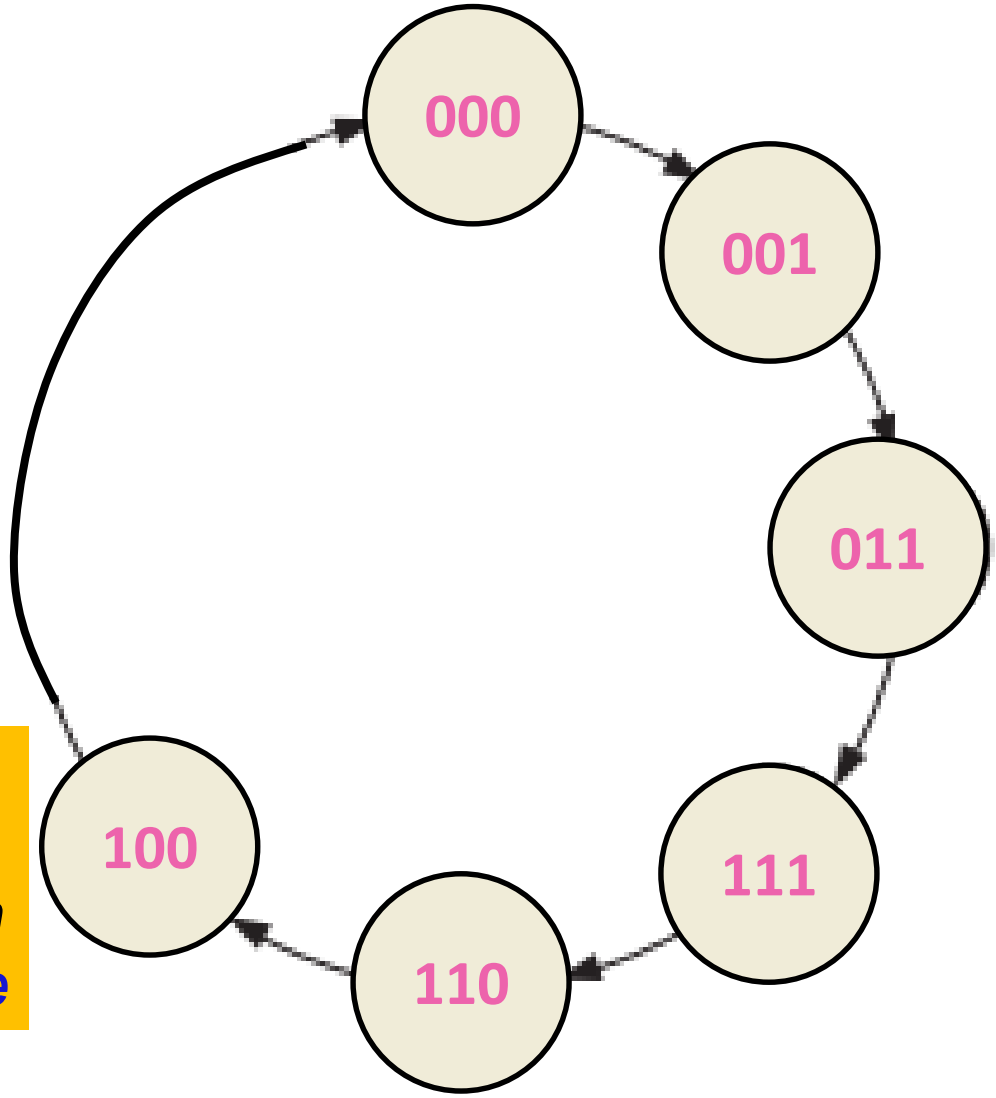
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	X	X	X
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	X	X	X
1	1	0	0	0	0
1	1	1	1	1	0

The next state is the state that the counter goes to from its present state upon application of a clock pulse



Exersice_03

❑Step 3: Flip-Flop Transition Table

- ❑For each output transition, the J and K inputs that will cause the output transition to occur are always the same and defined in table.

Next-state table

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	X	X	X
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	X	X	X
1	1	0	0	0	0
1	1	1	1	1	0

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑# of JK Flip-Flop = # of output of the counter. Here, # of JK Flip-Flop=3.

Next-state table

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1						
0	0	1	0	1	1						
0	1	0	X	X	X						
0	1	1	1	1	1						
1	0	0	0	0	0						
1	0	1	X	X	X						
1	1	0	0	0	0						
1	1	1	1	1	0						

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

Present State		Next State		Inputs of the JK-Flip Flop		
	Q0		Q0		J0	K0
	0		1			
	1		1			
	0		X			
	1		1			
	0		0			
	1		X			
	0		0			
	1		0			

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

Present State		Next State		Inputs of the JK-Flip Flop	
[redacted]	Q0	[redacted]	Q0	J0	K0
	0		1	1	X
	1		1	X	0
	0		X	X	X
	1		1	X	0
	0		0	0	X
	1		X	X	X
	0		0	0	X
	1		0	X	1

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

Present State		Next State		Inputs of the JK-Flip Flop		
	Q1		Q1		J1	K1
	0		0			
	0		1			
	1		X			
	1		1			
	0		0			
	0		X			
	1		0			
	1		1			

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

Present State	Next State	Inputs of the JK-Flip Flop	
Q1	Q1	J1	K1
0	0	0	X
0	1	1	X
1	X	X	X
1	1	X	0
0	0	0	X
0	X	X	X
1	0	X	1
1	1	X	0

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

Present State		Next State			Inputs of the JK-Flip Flop		
Q2	[redacted]	Q2	[redacted]	[redacted]	J2	K2	[redacted]
0	[redacted]	0	[redacted]	[redacted]			[redacted]
0	[redacted]	0	[redacted]	[redacted]			[redacted]
0	[redacted]	X	[redacted]	[redacted]			[redacted]
0	[redacted]	1	[redacted]	[redacted]			[redacted]
1	[redacted]	0	[redacted]	[redacted]			[redacted]
1	[redacted]	X	[redacted]	[redacted]			[redacted]
1	[redacted]	0	[redacted]	[redacted]			[redacted]
1	[redacted]	1	[redacted]	[redacted]			[redacted]

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

Present State		Next State			Inputs of the JK-Flip Flop		
Q2	[redacted]	Q2	[redacted]	[redacted]	J2	K2	[redacted]
0	[redacted]	0	[redacted]	[redacted]	0	X	[redacted]
0	[redacted]	0	[redacted]	[redacted]	0	X	[redacted]
0	[redacted]	X	[redacted]	[redacted]	X	X	[redacted]
0	[redacted]	1	[redacted]	[redacted]	1	X	[redacted]
1	[redacted]	0	[redacted]	[redacted]	X	1	[redacted]
1	[redacted]	X	[redacted]	[redacted]	X	X	[redacted]
1	[redacted]	0	[redacted]	[redacted]	X	0	[redacted]
1	[redacted]	1	[redacted]	[redacted]	X	0	[redacted]

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_03

❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	X	X	X	X	X	X	X	X	X
0	1	1	1	1	1	1	X	X	0	X	0
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	0	X	1	0	X
1	1	1	1	1	0	X	0	X	0	X	1

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

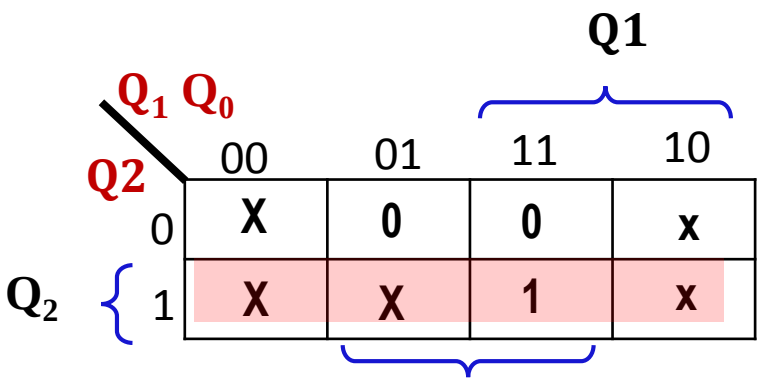
Exersice_03

❑Step 4: k-Maps

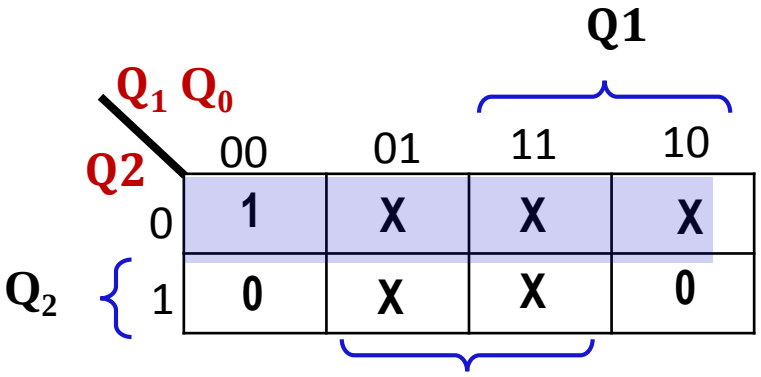
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	X	X	X	X	X	X	X	X	X
0	1	1	1	1	1	1	X	X	0	X	0
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	0	X	1	0	X
1	1	1	1	1	0	X	0	X	0	X	1



$K_0=Q_2$



$J_0=\overline{Q_2}$

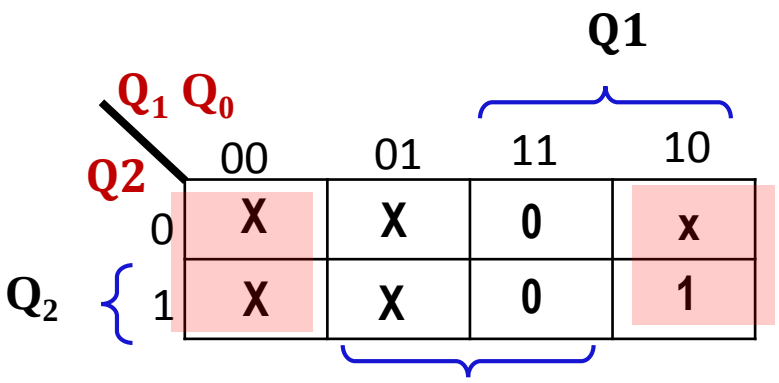
Exersice_03

❑Step 4: k-Maps

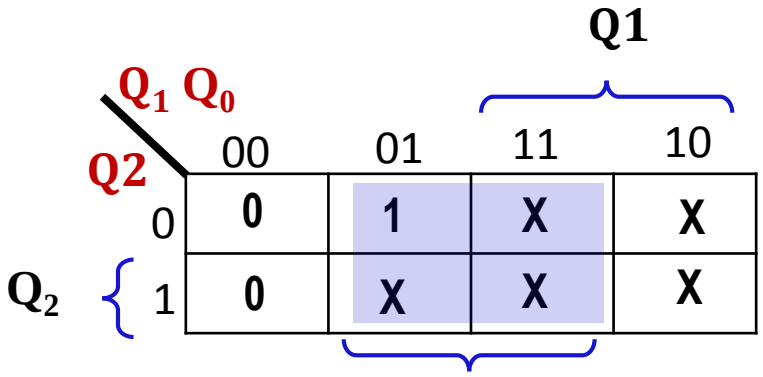
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	X	X	X	X	X	X	X	X	X
0	1	1	1	1	1	1	X	X	0	X	0
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	0	X	1	0	X
1	1	1	1	1	0	X	0	X	0	X	1



$K_1=\overline{Q_0}$



$J_1=Q_0$

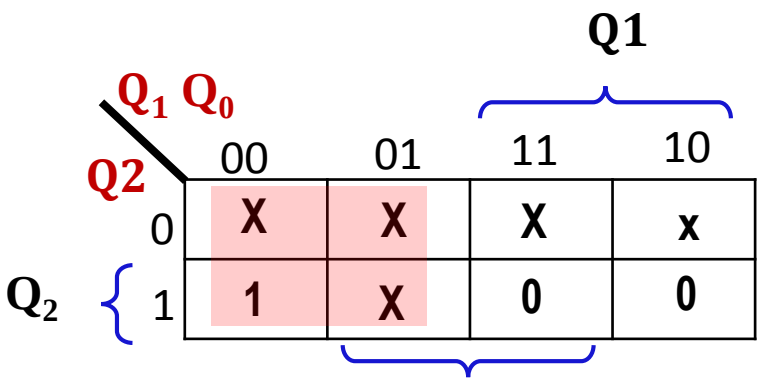
Exersice_03

❑Step 4: k-Maps

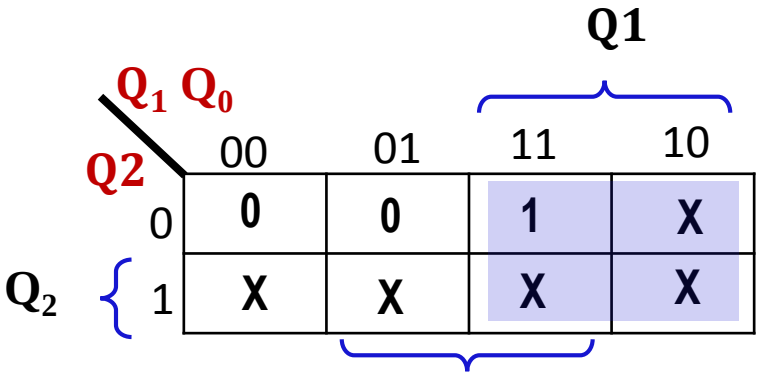
❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table

Present State			Next State			Inputs of the JK-Flip Flop					
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	X	X	X	X	X	X	X	X	X
0	1	1	1	1	1	1	X	X	0	X	0
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	0	0	0	X	0	X	1	0	X
1	1	1	1	1	0	X	0	X	0	X	1



$K_2=\overline{Q_1}$



$J_2=Q_1$

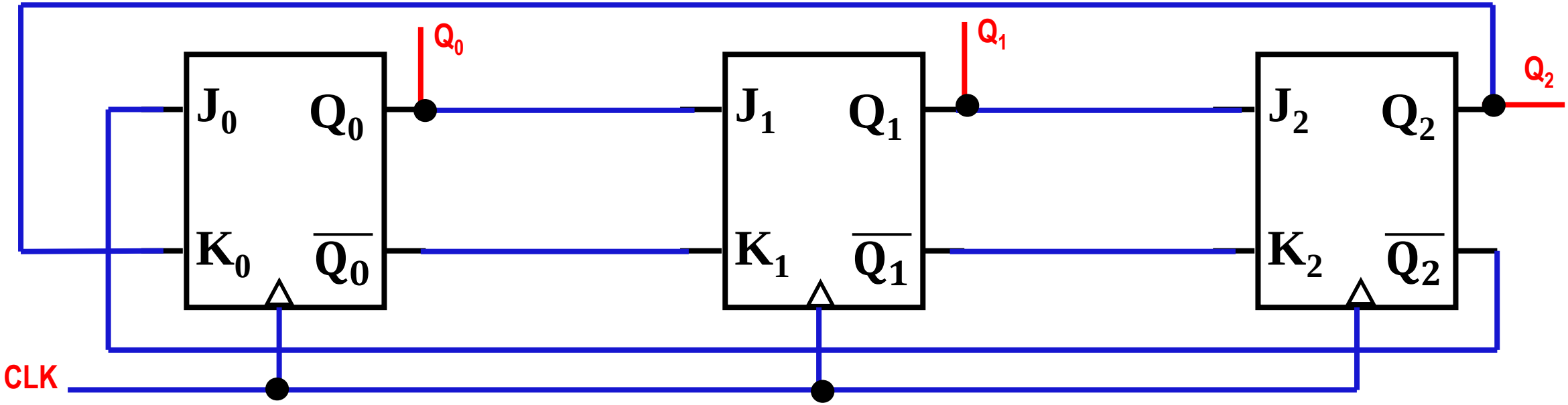
Exersice_03

❑Step 5: Counter implementation

❑The final step is to implement the combinational logic from the expressions for the *J* and *K* inputs

$J_0=\overline{Q_2}$ $J_1=Q_0.$ $J_2= Q1$

$K_0=Q_2$ $K_1=\overline{Q_0}$ $K_2=\overline{Q_1}$



Outlines

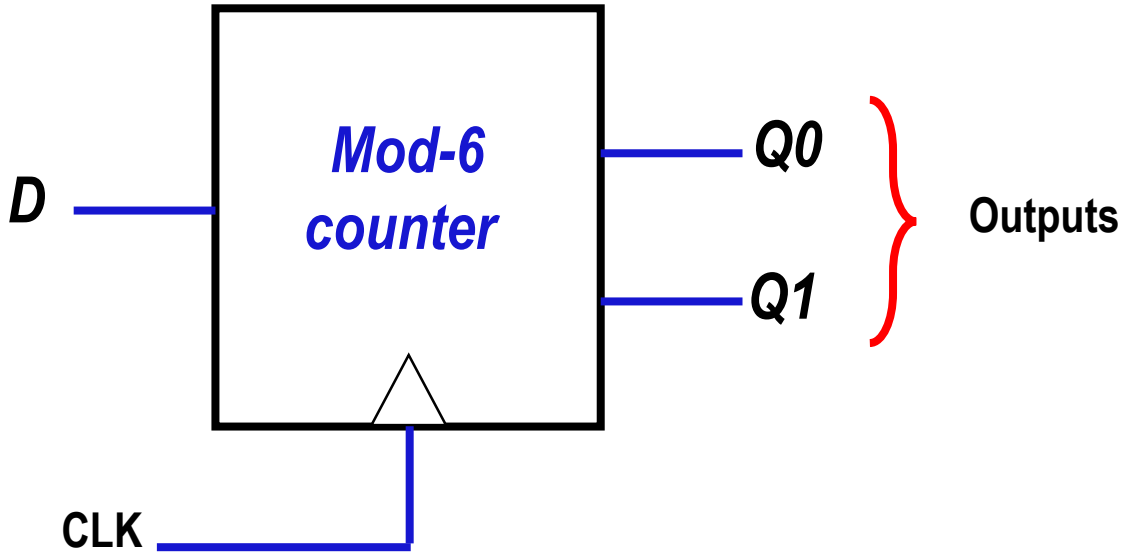
- Finite State Machine
- Asynchronous Counter
- Synchronous Counter
- Design of Synchronous Counters
- Exersice_01
- Exersice_02
- Exersice_03
- Exersice_04

Exersice_04

- Design a 2 bit up/down counter with an input D which determines the up/down function. Thus when D=0, the count sequence is 00,01,10,11,00 ... when D=1, the count sequence is 00,11,10,01,00 ...

Ans.

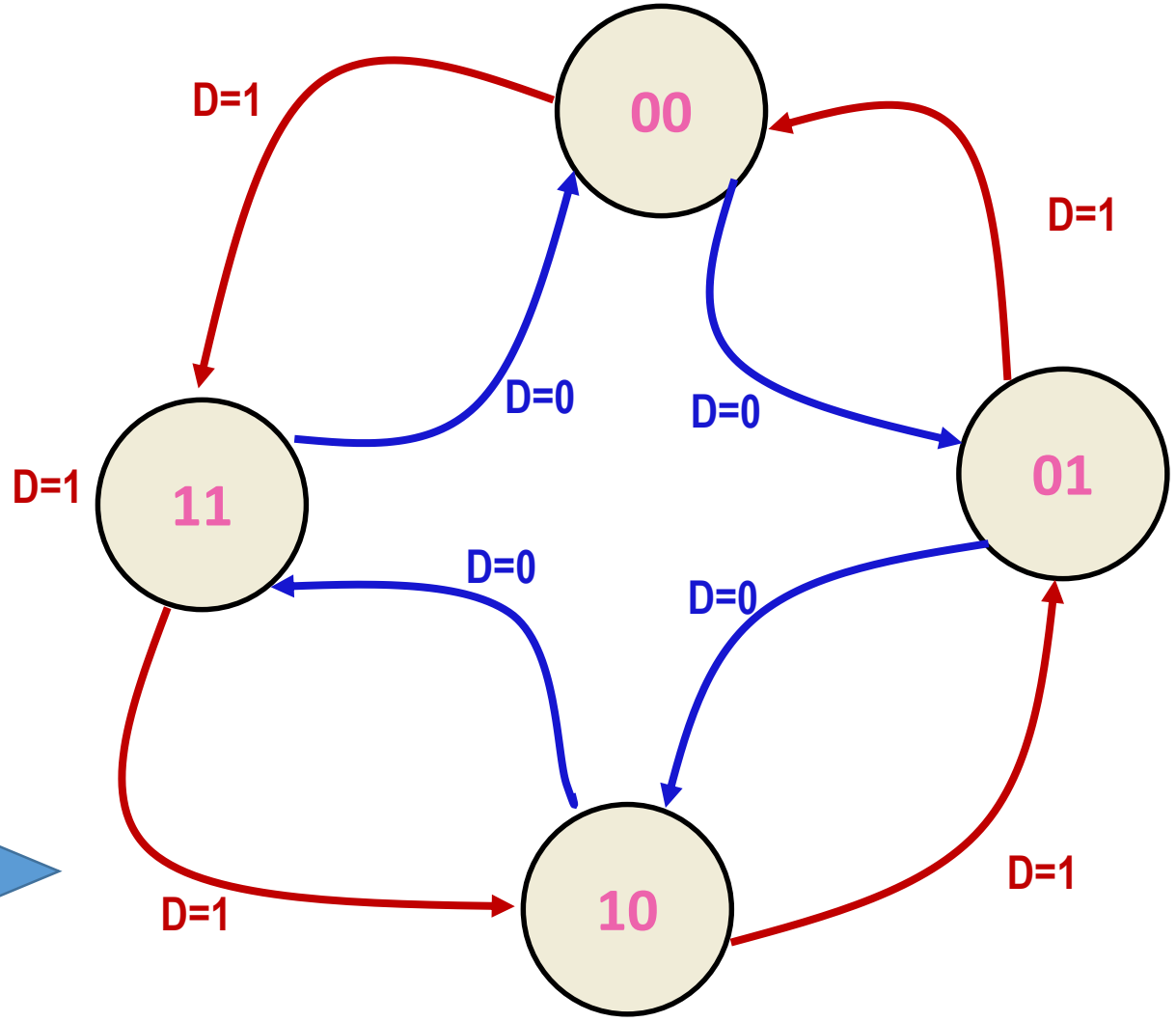
2 bit up/down counter → 2^2=4 states



Exersice_04

❑Step 1: State Diagram

2-bit synchronous→ 2^2 =4 states
Up counter → {0,1,2,3} @ D=0
Down counter→ {0,3,2,1} @ D=1



State Diagram

Exersice_04

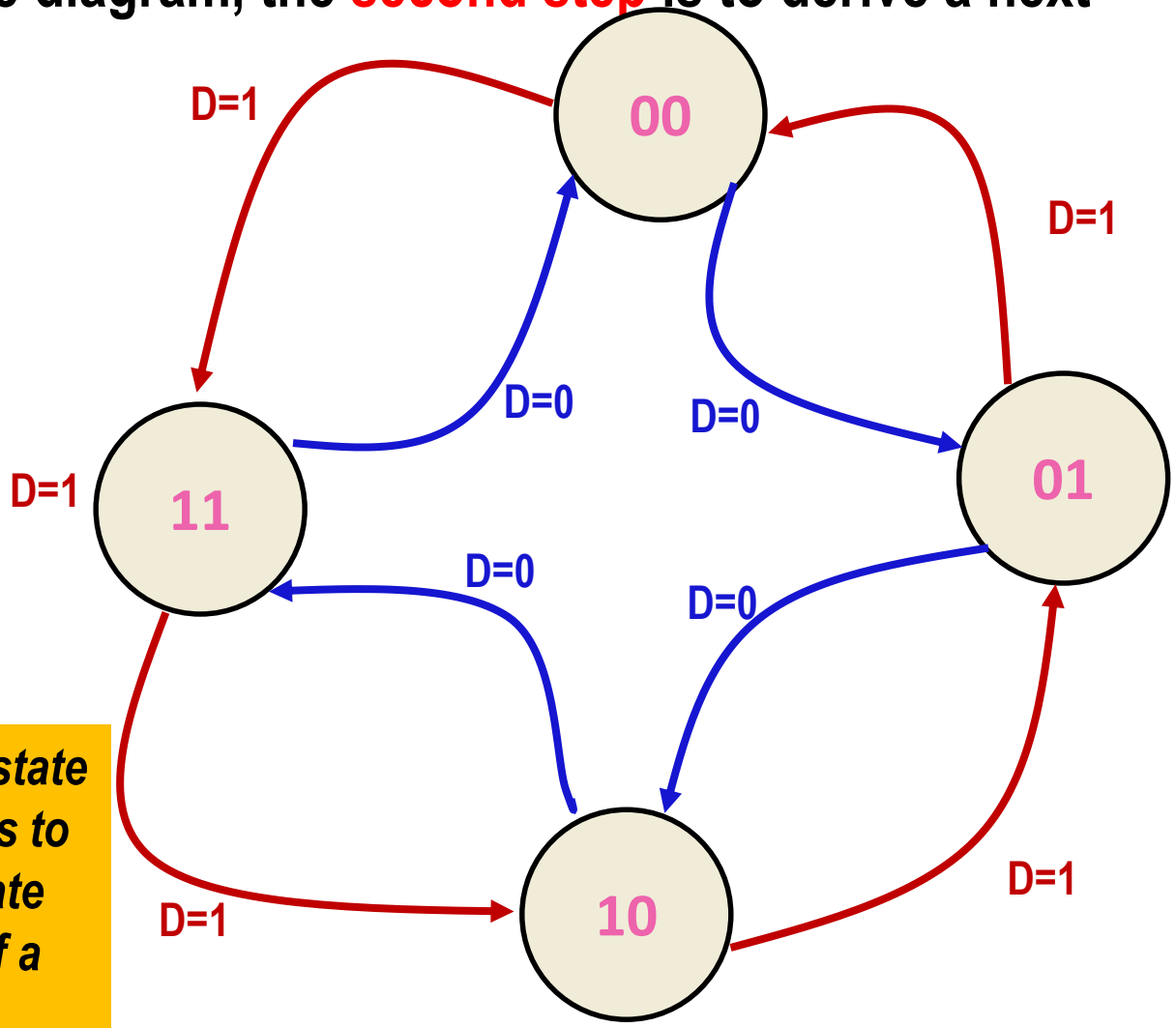
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table

I/P	Present State		Next State	
D	Q1	Q0	Q1	Q0

The next state is the state that the counter goes to from its present state upon application of a clock pulse



State Diagram

Exersice_04

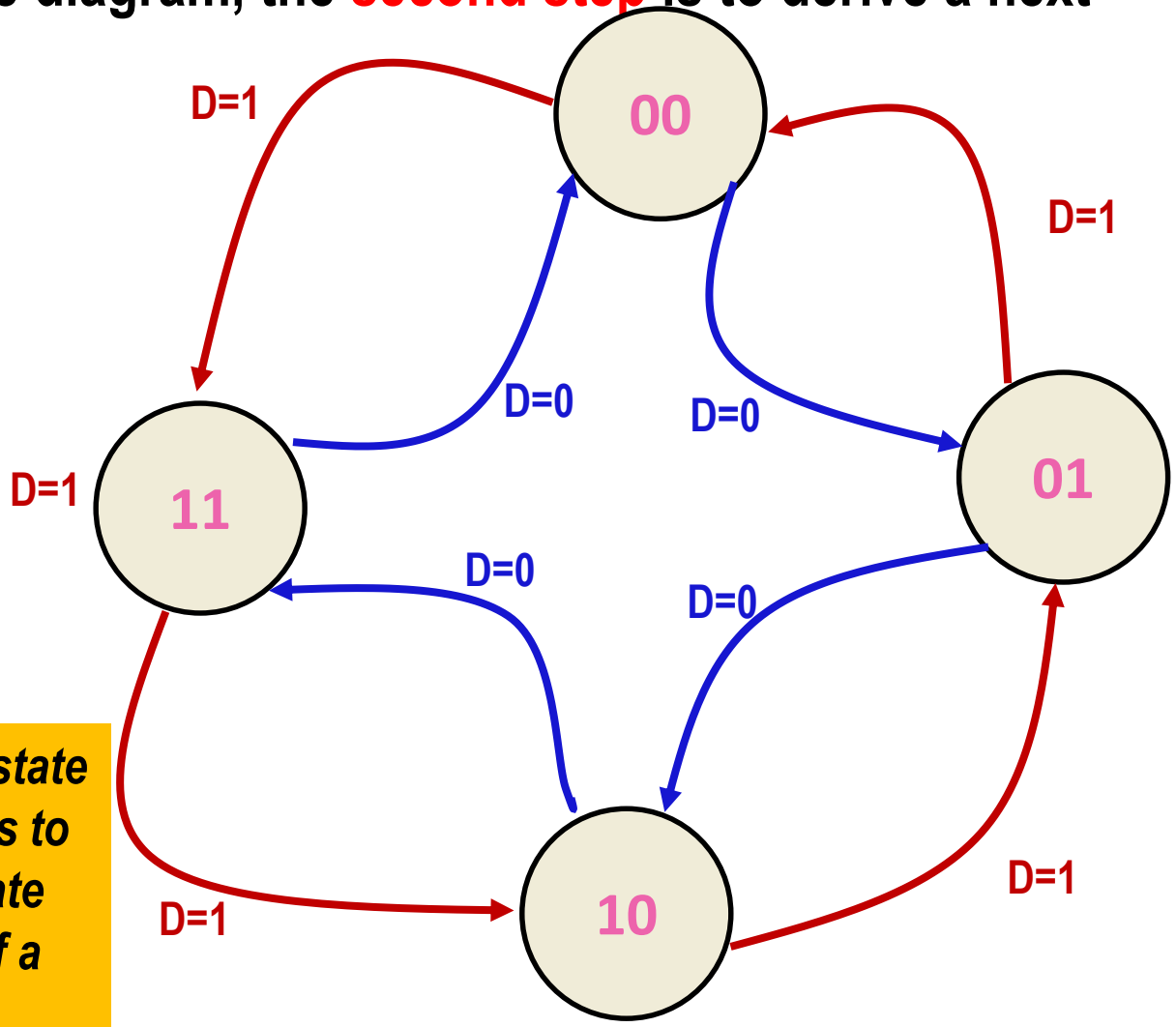
❑Step 2: Next-State Table

❑Once the sequential circuit is defined by a state diagram, the second step is to derive a next-state table

Next-state table

I/P	Present State		Next State	
D	Q1	Q0	Q1	Q0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

The next state is the state that the counter goes to from its present state upon application of a clock pulse



State Diagram

Exersice_04

❑Step 3: Flip-Flop Transition Table

❑For each output transition, the J and K inputs that will cause the output transition to occur are always the same and defined in table.

Next-state table

I/P	Present State		Next State	
D	Q1	Q0	Q1	Q0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_04

❑Step 3: Flip-Flop Transition Table

❑# of JK Flip-Flop = # of output of the counter. Here, # of JK Flip-Flop=2.

Next-state table

I/P	Present State		Next State		Inputs of the JK-Flip Flop			
D	Q1	Q0	Q1	Q0	J1	K1	J0	K0
0	0	0	0	1				
0	0	1	1	0				
0	1	0	1	1				
0	1	1	0	0				
1	0	0	1	1				
1	0	1	0	0				
1	1	0	0	1				
1	1	1	1	0				

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

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❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

I/P	Present State		Next State		Inputs of the JK-Flip Flop		
D		Q0		Q0		J0	K0
0		0		1			
0		1		0			
0		0		1			
0		1		0			
1		0		1			
1		1		0			
1		0		1			
1		1		0			

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_04

❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table

I/P	Present State		Next State		Inputs of the JK-Flip Flop	
D		Q0		Q0	J0	K0
0		0		1	1	X
0		1		0	X	1
0		0		1	1	X
0		1		0	X	1
1		0		1	1	X
1		1		0	X	1
1		0		1	1	X
1		1		0	X	1

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_04

❑Step 3: Flip-Flop Transition Table

❑**Map** between the each output transition and the inputs of JK Flip-Flop

Next-state table

I/P	Present State		Next State		Inputs of the JK-Flip Flop		
D	Q1		Q1		J1	K1	
0	0		0				
0	0		1				
0	1		1				
0	1		0				
1	0		1				
1	0		0				
1	1		0				
1	1		1				

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

Exersice_04

❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table

I/P	Present State		Next State		Inputs of the JK-Flip Flop		
D	Q1		Q1		J1	K1	
0	0		0		0	X	
0	0		1		1	X	
0	1		1		X	0	
0	1		0		X	1	
1	0		1		1	X	
1	0		0		0	X	
1	1		0		X	1	
1	1		1		X	0	

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

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❑Step 3: Flip-Flop Transition Table

❑Map between the each output transition and the inputs of JK Flip-Flop

Next-state table

I/P	Present State		Next State		Inputs of the JK-Flip Flop			
D	Q1	Q0	Q1	Q0	J1	K1	J0	K0
0	0	0	0	1	0	X	1	X
0	0	1	1	0	1	X	X	1
0	1	0	1	1	X	0	1	X
0	1	1	0	0	X	1	X	1
1	0	0	1	1	1	X	1	X
1	0	1	0	0	0	X	X	1
1	1	0	0	1	X	1	1	X
1	1	1	1	0	X	0	X	1

Transition table for a J-K flip-flop

Output Transistors			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0

Q_N : Present State
Q_{N+1} : Next State
X: Don't Care

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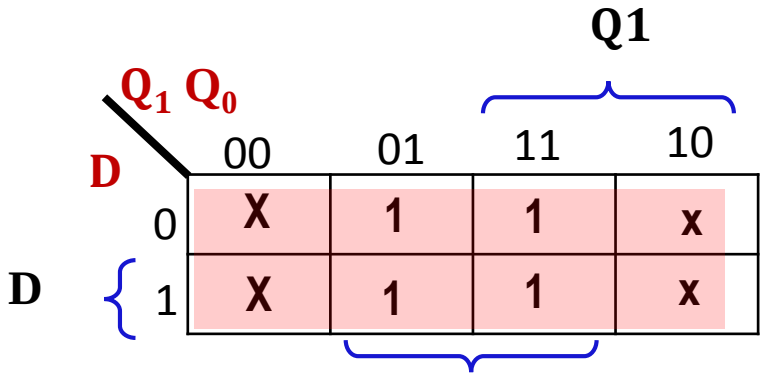
❑Step 4: k-Maps

❑K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

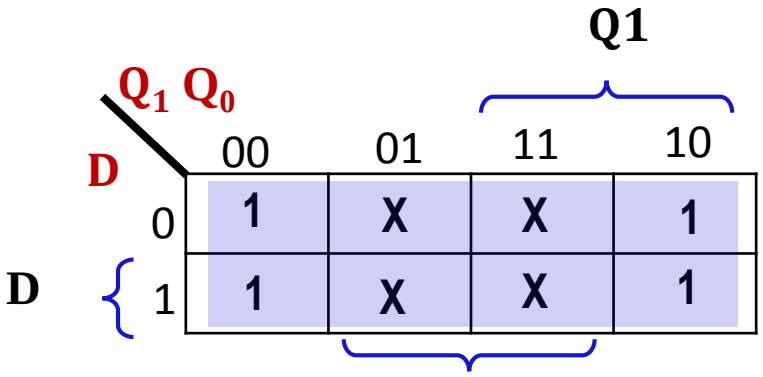
Next-state table

I/P	Present State		Next State	
D	Q1	Q0	Q1	Q0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Inputs of the JK-Flip Flop			
J1	K1	J0	K0
0	X	1	X
1	X	X	1
X	0	1	X
X	1	X	1
1	X	1	X
0	X	X	1
X	1	1	X
X	0	X	1



$K_0=1$



$J_0=1$

Exersice_04

- Step 4: k-Maps
  - K-maps can be used to determine the logic required for the J and K inputs of each flip-flop in the counter

Next-state table

I/P	Present State		Next State	
D	Q1	Q0	Q1	Q0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Inputs of the JK-Flip Flop			
J1	K1	J0	K0
0	X	1	X
1	X	X	1
X	0	1	X
X	1	X	1
1	X	1	X
0	X	X	1
X	1	1	X
X	0	X	1

Q1

D \ $Q_1 Q_0$	00	01	11	10
0	X	X	1	0
1	X	X	0	1

Q0

$$K_0 = \overline{D}.Q_0 + D.\overline{Q_0}$$
$$= Q_0 \oplus D$$

Q1

D \ $Q_1 Q_0$	00	01	11	10
0	0	1	X	X
1	1	0	X	X

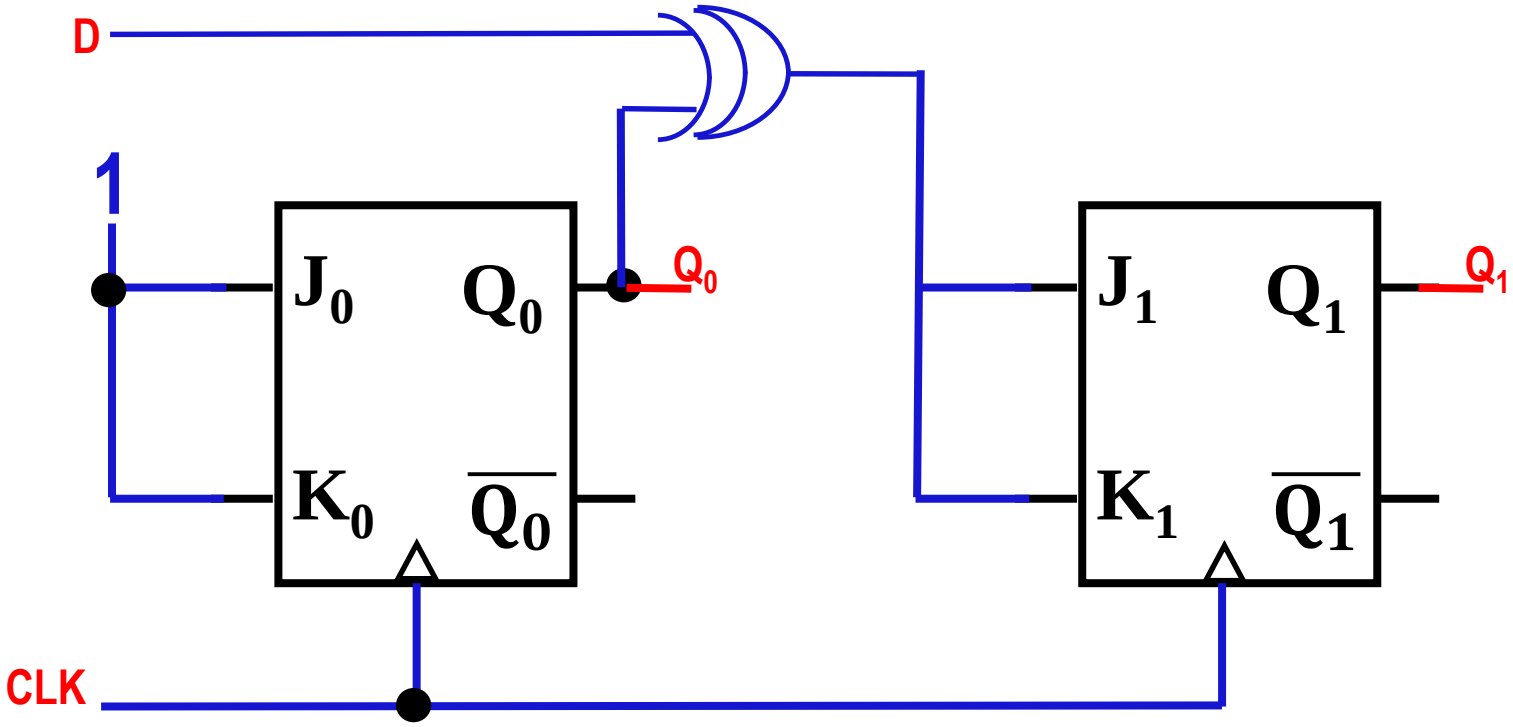
Q0

$$J_0 = \overline{D}.Q_0 + D.\overline{Q_0}$$
$$= Q_0 \oplus D$$

Exersice_04

❑Step 5: Counter implementation

❑The final step is to implement the combinational logic from the expressions for the *J* and *K* inputs

$J_0=1$ $\qquad$ $J_1= Q_0 \oplus D$

$K_0=1$ $\qquad$ $K_1=Q_0 \oplus D$