TRI-STATE® Hex Buffers

General Description

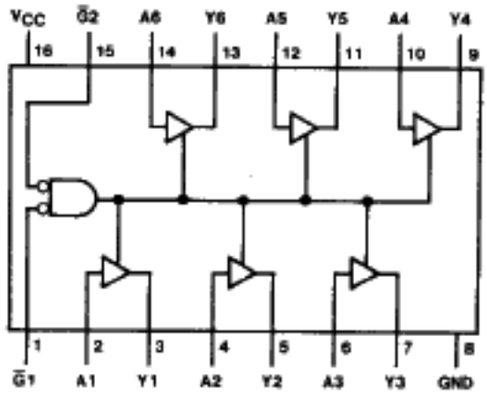
These devices provide six, two-input buffers in each package. Both the standard (7400 compatible) TTL technology, and the "true tenth-power" (74L compatible) low power versions are available for each of the four types. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The 95 and 97 present the true data at the outputs, while the 96 and 98 are inverting. On the 95 and 96 versions, all six control lines for TRI-STATE enable are common in a single line. On the 97 and 98 versions, four buffers are enabled from a common line, and the other two buffers from a separate common line. In all cases, the outputs are placed in the TRI-STATE condition by applying a high logic level to the control pins. With either the standard TTL or the low power versions of these circuits, it is possible to connect over 100 like devices to a common bus line and still have adequate drive capability.

Features

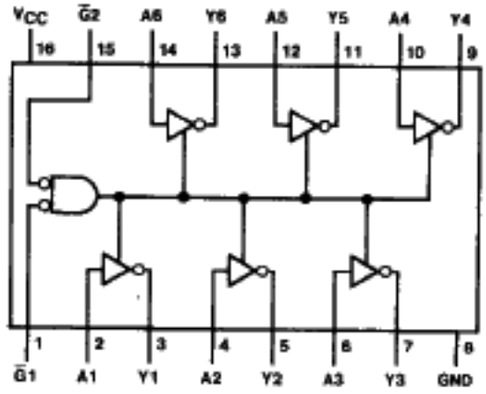
Type	Typical Power Dissipation	Typical Propagation Delay
95, 97	325 mW	12 ns
L95, L97	20 mW	34 ns
96, 98	295 mW	11 ns
L96, L98	15 mW	31 ns

- Pin equivalent to DM54365 (95), DM54366 (96), DM54367 (97), DM54368 (98)

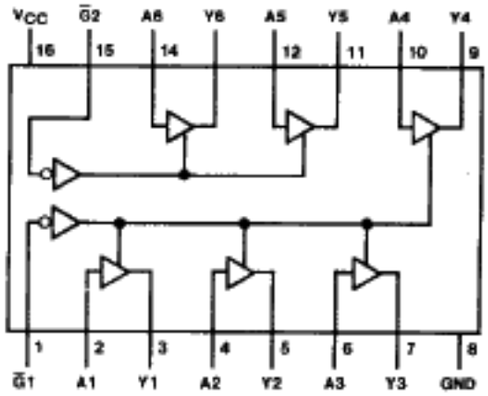
Connection Diagrams



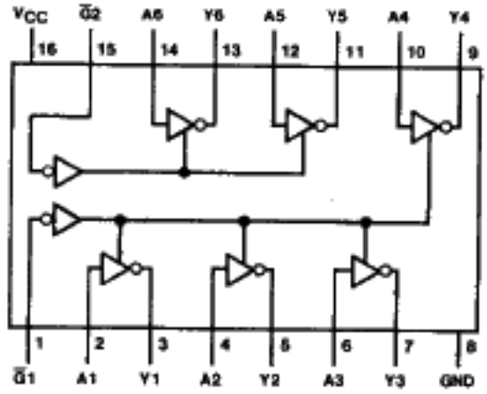
7095 (J,W)
70L95 (J,W)
8095 (N)
80L95 (N)



7096 (J,W)
70L96 (J,W)
8096 (N)
80L96 (N)



7097 (J,W)
70L97 (J,W)
8097 (N)
80L97 (N)



7098 (J,W)
70L98 (J,W)
8098 (N)
80L98 (N)

Truth Table (Each Driver)

95, L95

Inputs			Outputs
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

96, L96

Inputs			Outputs
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	L
L	L	L	H

97, L97

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	H
L	L	L

98, L98

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM70/80 95, 96, 97, 98 Min	Typ (1)	Max	DM70/80 L95, L96, L97, L98 Min	Typ (1)	Max	Units
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.8			0.7	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5			N/A	V
I_{OH}	High Level Output Current		DM70			−2.0			−1.0	mA
			DM80			−5.2			−1.0	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OH} = Max		2.4	3.1		2.4			V
I_{OL}	Low Level Output Current		DM70			32			2.0	mA
			DM80			32			3.6	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = Max, I_{OL} = Max	DM70			0.4			0.3	V
			DM80			0.4			0.4	
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2 V, V_{IL} = Max	V_O = 0.3 V						−10	μA
			V_O = 0.4 V			−40				
			V_O = 2.4 V			40			10	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V				40			10	μA
I_{IL}	Level Input Current, A Input	V_{CC} = Max	Both $\overline{G}$ Inputs at 2 V, V_I = 0.3 V						−10	μA
			Both $\overline{G}$ Inputs at 2 V, V_I = 0.5 V			−40				
			Both $\overline{G}$ Inputs at 0.4 V, V_I = 0.3 V						−0.18	mA
			Both $\overline{G}$ Inputs at 0.4 V, V_I = 0.4 V			−1.6				
	$\overline{G}$ Input		V_I = 0.3 V						−0.18	
			V_I = 0.4 V			−1.6				
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		−40		−115	−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max	95, 97		65	85		4.0	5.8	mA
			96, 98		59	77		3.0	4.5	

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time, and for the DM70/DM8095, 96, 97, 98 duration of short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions: Both	Std.	Low Power	DM70/80 95, 97 Typ	Max	96, 98 Typ	Max	DM70/80 L95, L97 Typ	Max	L96, L98 Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF	R_L = 400 Ω	R_L = 4 kΩ	10	16	11	17	30	60	26	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				14	22	10	16	37	75	35	53	ns
t_{ZH}	Output Enable Time to High Level				21	35	21	35	47	96	42	90	ns
t_{ZL}	Output Enable Time to Low Level				24	37	24	37	21	45	42	75	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF			6	11	6	11	47	90	25	43	ns
t_{LZ}	Output Disable Time from Low Level				16	27	16	27	30	63	34	63	ns

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