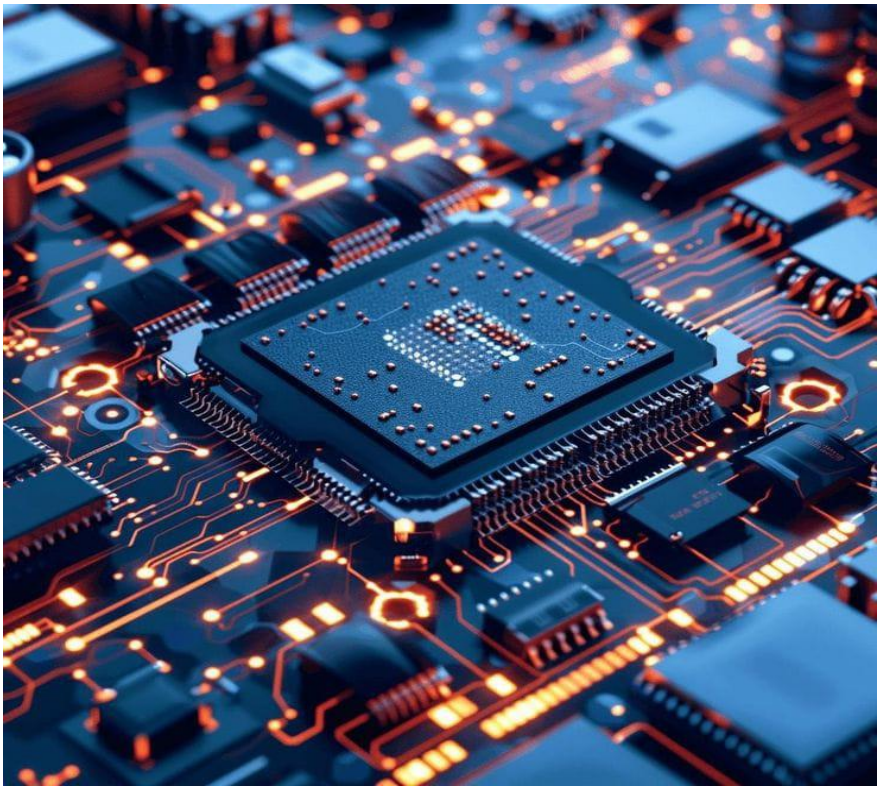

TUNNELING FIELD EFFECT TRANSISTORS

Course: ECE 222: Solid State Electronic Devices
Project: Simulation of advanced Solid-State Devices (TFET) using Silvaco TCAD

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Abstract

This report presents the design, simulation, and characterization of a Double-Gate (DG) Tunneling Field-Effect Transistor (TFET) using the Silvaco ATLAS TCAD tool. The project aims to investigate the fundamental operating principles and performance characteristics of TFETs, which are promising candidates for low-power electronics due to their potential for a sub-60 mV/decade subthreshold swing. A Intrinsic channel silicon DG-TFET with a p-i-n structure was simulated. The report details the device structure, simulation methodology, and physical models employed. Key results, including the Id-Vg and Id-Vd characteristics, energy band diagrams, and internal physical properties, are analyzed. The simulation confirms the TFET's operation via band-to-band tunneling (BTBT), demonstrating steep-slope switching behavior. However, it also highlights the challenge of ambipolar conduction, a characteristic issue in TFET design.

1. Introduction

As conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) approach their physical scaling limits, their power consumption has become a major bottleneck. The subthreshold swing (SS) of a MOSFET is fundamentally limited to 60 mV/decade at room temperature, which restricts the reduction of the threshold voltage and leads to significant leakage currents.

The Tunneling Field-Effect Transistor (TFET) is an alternative device architecture that overcomes this limitation. Instead of relying on thermionic emission over a potential barrier, the TFET operates based on the quantum mechanical principle of band-to-band tunneling (BTBT). By modulating the tunneling barrier width with the gate voltage, a TFET can achieve a subthreshold swing below 60 mV/decade, enabling ultra-low power operation.

The objective of this project is to use the Silvaco TCAD framework to:

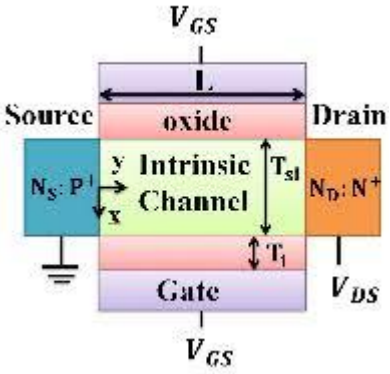
1. Construct a Double-Gate (DG) Intrinsic channel TFET structure.
2. Simulate its electrical characteristics (Id-Vg, Id-Vd).
3. Analyze the internal device physics, including energy bands and tunneling rates, to understand its operation.

2. Device Structure and Simulation Code and Methodology

2.1 Device Structure

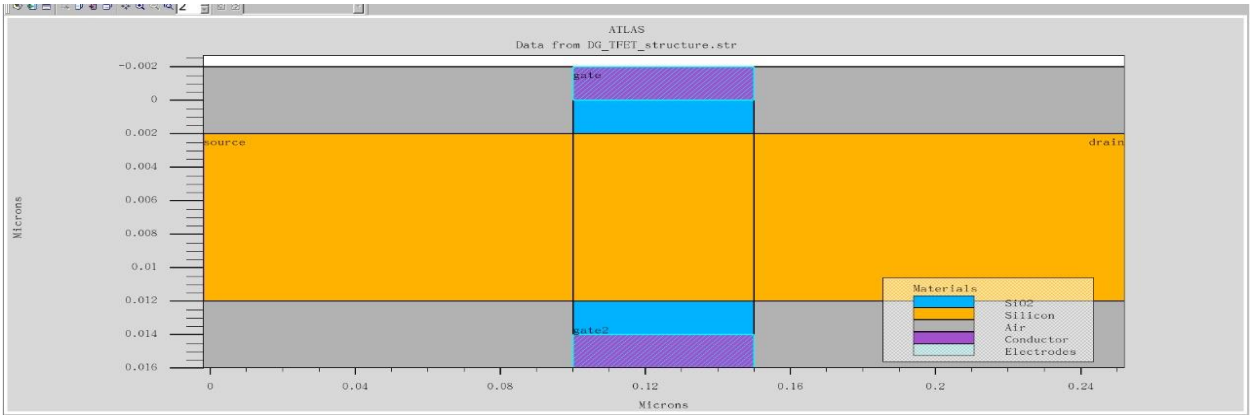
The device features a p-i-n doping profile, essential for a p-channel TFET:

Source: p-type doped region (Boron), concentration $1x10^{18}$ cm^{-3}.
Channel: Intrinsic region.
Drain: n-type doped region (Arsenic), concentration $1x10^{20}$ cm^{-3}.

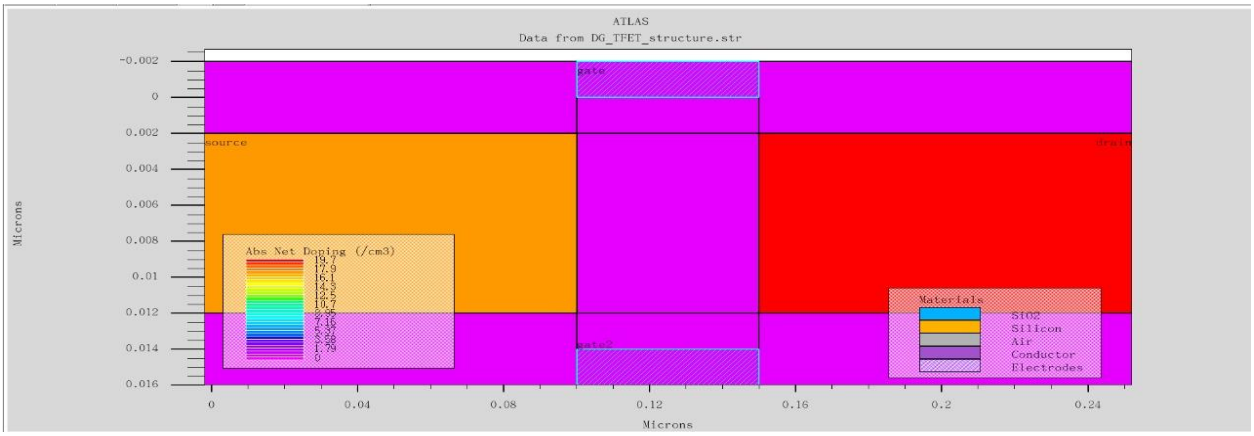


The simulated device is a Double-Gate (DG) TFET, as shown in the material and doping profile figures below. The double-gate structure provides superior electrostatic control over the channel, which is crucial for enhancing TFET performance.

(Device structure with materials)



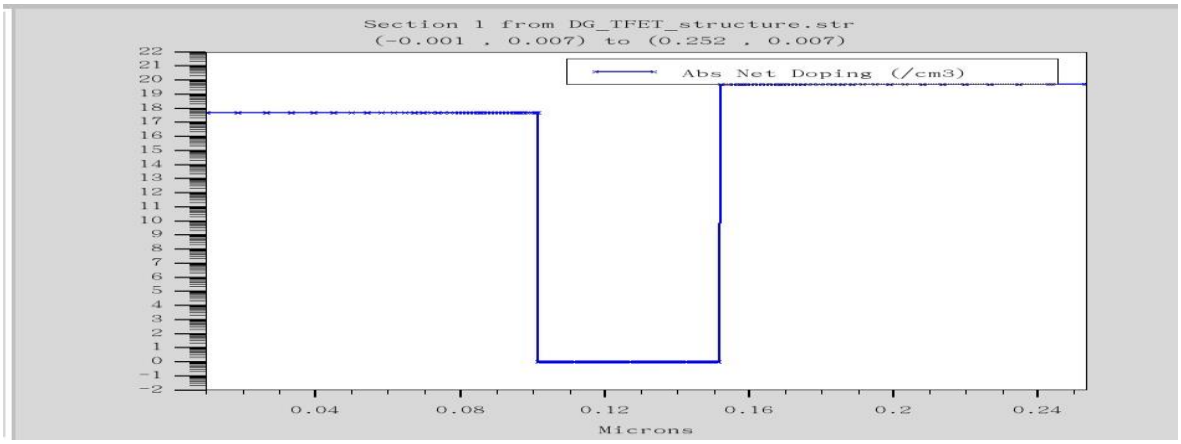
(Device structure with doping overlay)



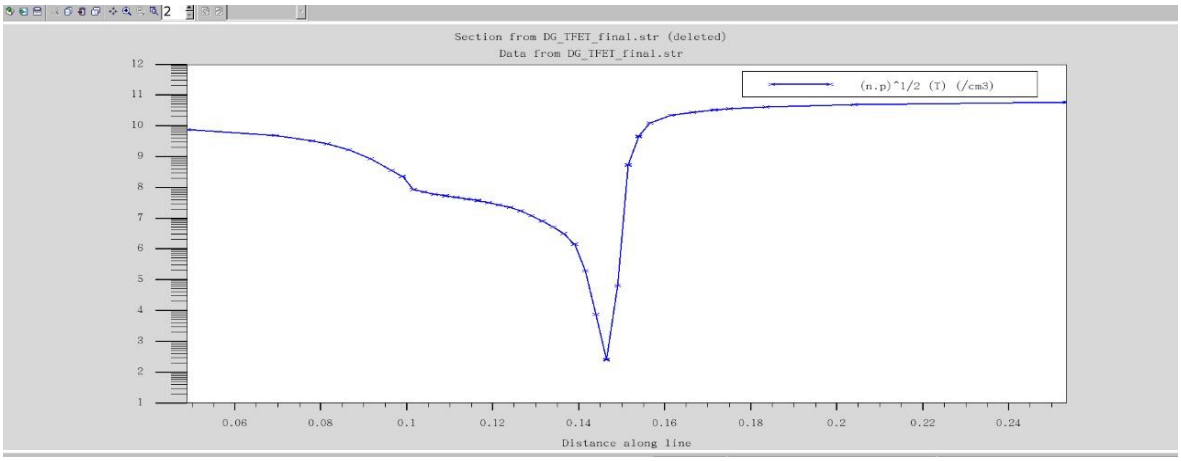
The key structural parameters and materials are:

- **Channel Material:** Silicon (Si)
- **Gate Dielectric:** Silicon Dioxide (SiO_2)
- **Gate Electrodes:** Conductor (Top and Bottom Gates)
- **Gate Length (Lg):** 50 nm (from x=0.1 µm to x=0.15 µm)
- **Silicon Body Thickness (Tsi):** 10 nm (from y=0.002 µm to y=0.012 µm)
- **Source Length:** 100 nm (from x=0 to x=0.1 µm)
- **Drain Length:** 100 nm (from x=0.15 µm to x=0.25 µm)

The detailed doping profile along the channel is confirmed by the 1D cutline plot below.



(1D cutline of Abs Net Doping)



(Ni plotting)

2.2 Silvaco code

```
go atlas
mesh space.mult= 1

# Define Meshes
x.mesh loc=-0.002 spac=0.01
x.mesh loc=0.080 spac=0.001
x.mesh loc=0.095 spac=0.001
x.mesh loc=0.100 spac=0.0005
x.mesh loc=0.105 spac=0.0005
x.mesh loc=0.145 spac=0.0005
x.mesh loc=0.150 spac=0.0005
x.mesh loc=0.155 spac=0.001
```

```
x.mesh loc=0.170 spac=0.001
x.mesh loc=0.252 spac=0.01

y.mesh loc=-0.002 spac=0.001
y.mesh loc=0.002 spac=0.0005
y.mesh loc=0.0025 spac=0.001
y.mesh loc=0.012 spac=0.0005
y.mesh loc=0.014 spac=0.0005
y.mesh loc=0.016 spac=0.001

# Define regions
region num=1 y.min=0.000 y.max=0.002 x.min=0.10  x.max=0.150 material=Oxide
region num=2 y.min=0.002 y.max=0.012 x.min=0.00  x.max=0.100 material=Silicon
region num=3 y.min=0.002 y.max=0.012 x.min=0.10  x.max=0.150 material=Silicon
region num=4 y.min=0.002 y.max=0.012 x.min=0.15  x.max=0.250 material=Silicon
region num=5 y.min=0.012 y.max=0.014 x.min=0.10  x.max=0.150 material=Oxide

# Air regions
region num=6 y.min=-0.002 y.max=0.002 x.min=0.00  x.max=0.100 material=Air
region num=7 y.min=-0.002 y.max=0.002 x.min=0.150 x.max=0.252 material=Air
region num=8 y.min=0.014 y.max=0.016 x.min=0.00  x.max=0.100 material=Air
region num=9 y.min=0.014 y.max=0.016 x.min=0.150 x.max=0.252 material=Air

# Gate metal region
region num=10 y.min=-0.002 y.max=0.000 x.min=0.10 x.max=0.150 material=aluminum
region num=11 y.min=0.014 y.max=0.016 x.min=0.10 x.max=0.150 material=aluminum

# Source and drain region
region num=12 y.min=0.002 y.max=0.012 x.min=-0.002 x.max=0.000 material=aluminum
region num=13 y.min=0.002 y.max=0.012 x.min=0.250 x.max=0.252 material=aluminum

# air region
region num=14 y.min=-0.002 y.max=0.002 x.min=-0.002 x.max=0.10 material=Air
region num=15 y.min=0.0120 y.max=0.016 x.min=-0.002 x.max=0.10 material=Air
region num=16 y.min=-0.002 y.max=0.002 x.min=0.150  x.max=0.252 material=Air
region num=17 y.min=0.0120 y.max=0.016 x.min=0.150  x.max=0.252 material=Air

# Define electrodes
electrode name=gate x.min=0.100 x.max=0.150  y.min=-0.002 y.max=0.000
electrode name=gate2 x.min=0.100 x.max=0.150 y.min=0.014 y.max=0.016
electrode name=source x.min=-0.002 x.max=0.000 y.min=0.002 y.max=0.012
electrode name=drain x.min=0.250 x.max=0.252 y.min=0.002 y.max=0.012

# Define quantum mesh
qtx.mesh loc=0.00 spac=0.01
qtx.mesh loc=0.090 spac=0.001
qtx.mesh loc=0.098 spac=0.001
qtx.mesh loc=0.100 spac=0.0001
qtx.mesh loc=0.125 spac=0.0001
qtx.mesh loc=0.150 spac=0.0001
qtx.mesh loc=0.152 spac=0.001
qtx.mesh loc=0.160 spac=0.001
qtx.mesh loc=0.250 spac=0.01

qty.mesh loc=0.000 spac=0.001
qty.mesh loc=0.002 spac=0.0002
qty.mesh loc=0.007 spac=0.0002
qty.mesh loc=0.012 spac=0.0002
```

```
qty.mesh loc=0.014 spac=0.001

material material=silicon me.tunnel=0.19 mh.tunnel=0.16 EG300=1.12 \
         TAUN0=1e-8 TAUP0=1e-8 PERMITTIVITY=11.8 NC300=2.8e19 NV300=1.04e19 MUN=1400
MUP=450

material material=oxide PERMITTIVITY=3.9 EG300=9.0

# Define doping profile
doping uniform n.type conc=5e17 region=2
doping uniform p.type conc=5e19 region=4

# Contact work functions
contact name=gate workfunction=4.5
contact name=gate2 workfunction=4.5 common=gate

# physical models
models bbt.nonlocal bbt.forward qtunn.dir=1 bgn consrh conmob

# Save structure
save outf=DG_TFET_structure.str
tonyplot DG_TFET_structure.str

method gummel carriers=2 itlim=100
solve init

method newton carriers=2 itlim=50 autonr nrcriterion=0.1

# ========================================
# ENERGY BAND DIAGRAM VISUALIZATION SECTION
# ========================================

# Subthreshold - Below Threshold (Vg=-0.3V, Vd=-0.5V)
# Gate voltage below threshold, minimal tunneling
solve vsource=0 vgate=-0.3 vdrain=-0.5
save outf=Subthreshold_state.str
output con.band val.band band.temp band.param traps u.srh j.electron j.hole j.total
qfn qfp

# ON State - Above Threshold (Vg=0.5V, Vd=-1.0V)
# Gate voltage enables band-to-band tunneling, device is ON
solve vsource=0 vgate=0.5 vdrain=-1.0
save outf=ON_state_tunneling.str
output con.band val.band band.temp band.param traps u.srh j.electron j.hole j.total
qfn qfp


# Plot each case individually first to verify they exist
tonyplot Subthreshold_state.str
tonyplot ON_state_tunneling.str

# Create one comprehensive overlay showing OFF, Subthreshold, and ON states
tonyplot -overlay Subthreshold_state.str ON_state_tunneling.str

# ========================================
# ORIGINAL CHARACTERISTIC CURVES SECTION
# ========================================
```

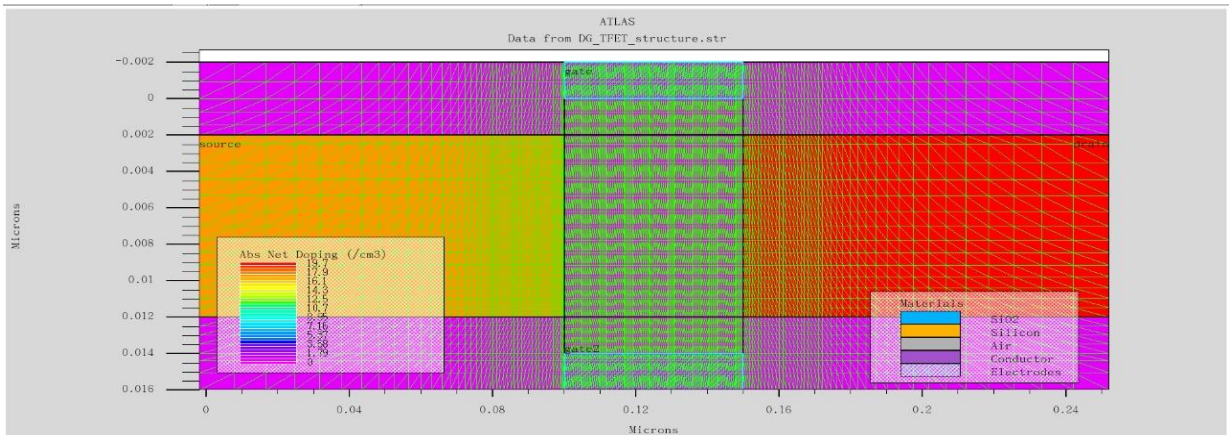
```
# Vgate sweep at different drain voltages
log outf=Vd_neg_0_5.log
solve vsource=0 vgate=-1.2 vdrain=-0.5
solve vgate=-1.0 vstep=0.01 vfinal=-0.8 name=gate electrode=gate
solve vgate=-0.8 vstep=0.01 vfinal=-0.6 name=gate electrode=gate
solve vgate=-0.6 vstep=0.005 vfinal=2.0 name=gate electrode=gate
solve vgate=2 vstep=0.1 vfinal=5.0 name=gate electrode=gate

log outf=Vd_neg_1.log
solve vsource=0 vgate=-1.2 vdrain=-1.0

solve vgate=-1.0 vstep=0.01 vfinal=-0.8 name=gate electrode=gate
solve vgate=-0.8 vstep=0.01 vfinal=-0.6 name=gate electrode=gate
solve vgate=-0.6 vstep=0.005 vfinal=2.0 name=gate electrode=gate
solve vgate=2 vstep=0.1 vfinal=5.0 name=gate electrode=gate

log outf=Vd_neg_1_5.log
solve vsource=0 vgate=-1.2 vdrain=-1.5

solve vgate=-1.0 vstep=0.01 vfinal=-0.8 name=gate electrode=gate
solve vgate=-0.8 vstep=0.01 vfinal=-0.6 name=gate electrode=gate
solve vgate=-0.6 vstep=0.005 vfinal=2.0 name=gate electrode=gate
solve vgate=2 vstep=0.1 vfinal=5.0 name=gate electrode=gate

log outf=Vd_neg_2.log
solve vsource=0 vgate=-1.2 vdrain=-2

solve vgate=-1.0 vstep=0.01 vfinal=-0.8 name=gate electrode=gate
solve vgate=-0.8 vstep=0.01 vfinal=-0.6 name=gate electrode=gate
solve vgate=-0.6 vstep=0.005 vfinal=2.0 name=gate electrode=gate
solve vgate=2 vstep=0.1 vfinal=5.0 name=gate electrode=gate

# Id vs Vg characteristic curves
tonyplot -overlay Vd_neg_0_5.log Vd_neg_1.log Vd_neg_1_5.log Vd_neg_2.log

# Vd sweep at different gate voltages
log outf=Vg_neg_0_6.log
solve vsource=0 vgate=-0.6 vdrain=0.0
solve vdrain=0.0 vstep=-0.02 vfinal=-3.0 name=drain electrode=drain
solve vdrain=-3.0 vstep=-0.1 vfinal=-5.0 name=drain electrode=drain

log outf=Vg_neg_0_4.log
solve vsource=0 vgate=-0.4 vdrain=0.0
solve vdrain=0.0 vstep=-0.02 vfinal=-3.0 name=drain electrode=drain
solve vdrain=-3.0 vstep=-0.1 vfinal=-5.0 name=drain electrode=drain

log outf=Vg_neg_0_2.log
solve vsource=0 vgate=-0.2 vdrain=0.0
solve vdrain=0.0 vstep=-0.02 vfinal=-3.0 name=drain electrode=drain
solve vdrain=-3.0 vstep=-0.1 vfinal=-5.0 name=drain electrode=drain

log outf=Vg_0_0.log
solve vsource=0 vgate=0.0 vdrain=0.0
solve vdrain=0.0 vstep=-0.02 vfinal=-3.0 name=drain electrode=drain
solve vdrain=-3.0 vstep=-0.1 vfinal=-5.0 name=drain electrode=drain

log outf=Vg_pos_0.2.log
solve vsource=0 vgate=0.2 vdrain=0.0
```

```
solve vdrain=0.0 vstep=-0.02 vfinal=-3.0 name=drain electrode=drain
solve vdrain=-3.0 vstep=-0.1 vfinal=-5.0 name=drain electrode=drain

log outf=Vg_pos_0.4.log
solve vsource=0 vgate=0.4 vdrain=0.0
solve vdrain=0.0 vstep=-0.02 vfinal=-3.0 name=drain electrode=drain
solve vdrain=-3.0 vstep=-0.1 vfinal=-5.0 name=drain electrode=drain

save outf=DG_TFET_final.str
tonyplot DG_TFET_final.str

# Id vs Vd characteristic curves
tonyplot -overlay Vg_neg_0_6.log Vg_neg_0_4.log Vg_neg_0_2.log Vg_0_0.log
Vg_pos_0.2.log Vg_pos_0.4.log

quit
```

2.3 Simulation Methodology

The simulations were performed using the **Silvaco ATLAS** device simulator. A fine mesh was defined, particularly at the source-channel and channel-drain junctions, to accurately capture the high electric fields and tunneling phenomena.

(Device structure with mesh overlay)



The following physical models were activated in the simulation to accurately model the TFET's behavior:

Carrier Transport: Drift-Diffusion model was used to solve for carrier transport.

Band-to-Band Tunneling (BTBT): A **Nonlocal BTBT model** was employed. This is critical for TFETs, as tunneling is a nonlocal phenomenon where an electron's transition depends on the band structure over a finite distance.

Recombination: The Shockley-Read-Hall (SRH) recombination model was included to account for trap-assisted recombination.

Mobility: Standard concentration-dependent and field-dependent mobility models were used.

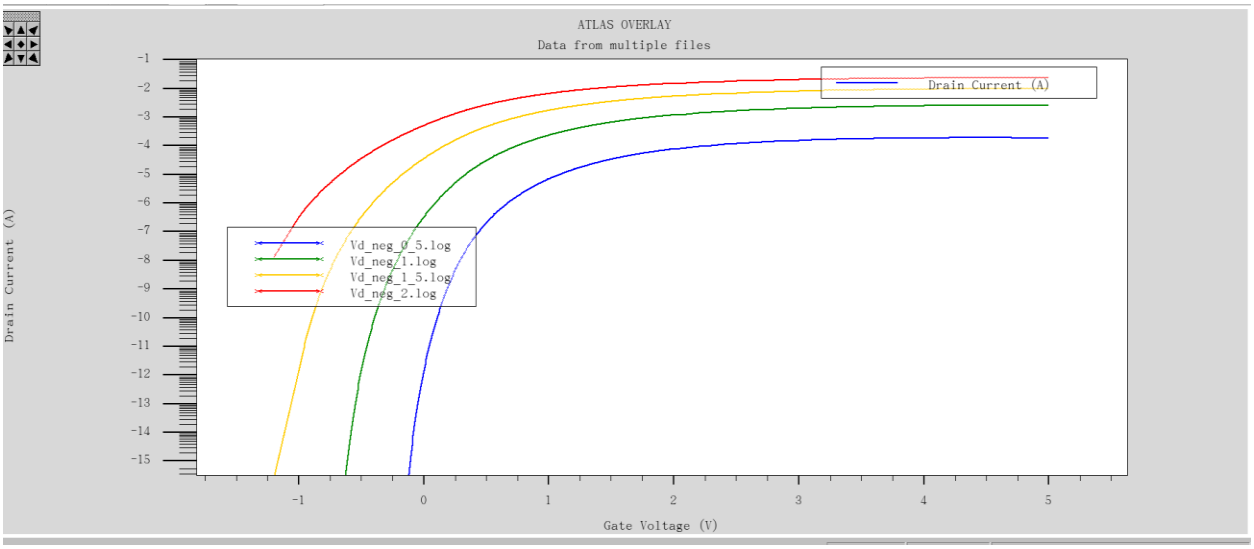
The simulation procedure involved ramping the gate and drain voltages to obtain the transfer (Id-Vg) and output (Id-Vd) characteristics.

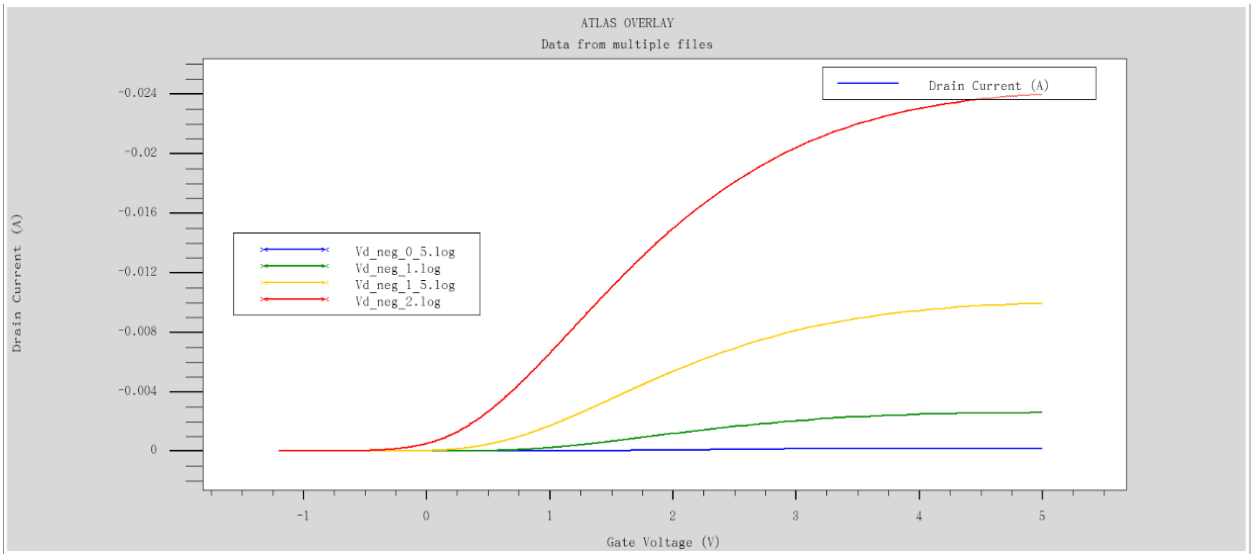
3. Results

3.1 Transfer Characteristics (Id-Vg)

The transfer characteristic curve plots the drain current (Id) on a logarithmic scale against the gate voltage (Vg) for different drain voltages (Vd).

(InsId-Vg transfer characteristics)





Key Observations:

P-channel Operation: The device turns on for negative gate voltages (Vg < 0 V), confirming its Intrinsic-channel behavior. In this mode, a negative Vg pulls the energy bands in the channel up, enabling electrons from the valence band in the p+ source to tunnel into the conduction band of the intrinsic channel, leaving holes that drift to the drain.

Steep Subthreshold Swing: The plot shows a very sharp transition from the OFF-state (low current) to the ON-state. This indicates a subthreshold swing (SS) that is significantly steeper than the 60 mV/decade limit of MOSFETs, which is the primary advantage of a TFET.

Ambipolar Conduction: For positive gate voltages (Vg > 0 V), the drain current begins to rise again. This is known as ambipolar conduction. It occurs because a large positive Vg pulls the channel bands down, enabling tunneling at the channel-drain junction. This is a significant leakage path and a major drawback of simple TFET designs.

Maximum separation: occurs at 0V gate voltage (transition region)

Minimum separation: occurs at -1V gate voltage (subthreshold region)

Systematic pattern: Outer curve pairs (Red-Orange) show largest separation, inner pairs (Green-Blue) show smallest

Fan-out ratio: Curves spread 6-7x wider in transition region compared to subthreshold region

Physical significance: Greatest drain voltage sensitivity occurs in the transition region where transistor switches between off and on states

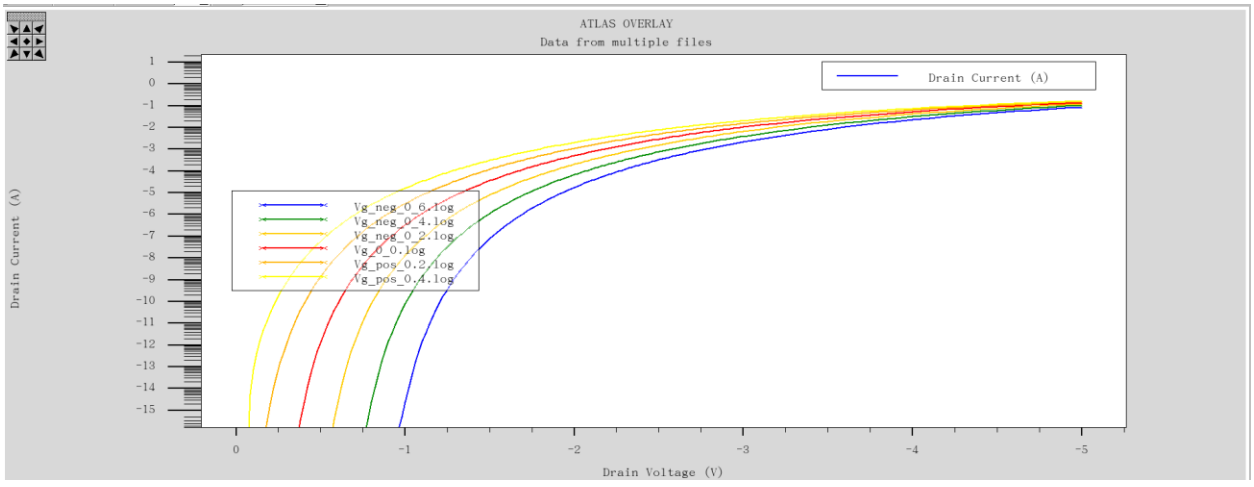
Effect of Vd: As the drain voltage (Vd) increases from 0.5V to 1.5V, the ON-current increases due to the larger energy window available for tunneling.

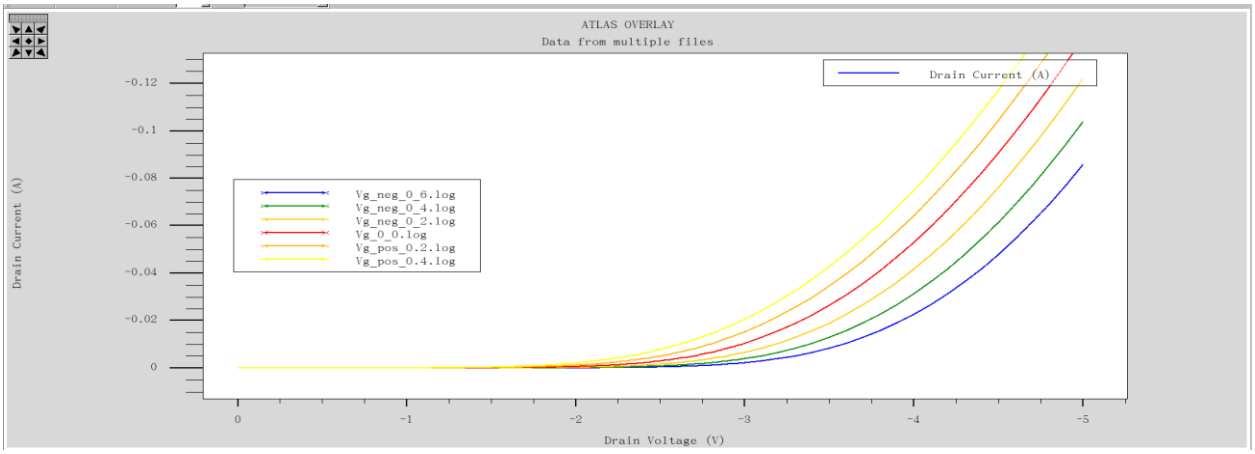
Curve Spacing Analysis: Distance Between Adjacent Lines				
Gate Voltage (V)	**Red-Orange Separation**	**Orange-Green Separation**	**Green-Blue Separation**	**Operating Region**
-1.0	0.3 units	0.2 units	0.1 units	Subthreshold
0.0	2.0 units	2.0 units	1.5 units	Transition
+2.0	0.5 units	0.4 units	0.3 units	Saturation

3.2 Output Characteristics (Id-Vd)

The output characteristics plot the drain current (Id) against the drain voltage (Vd) for various fixed gate voltages (Vg).

(Id-Vd output characteristics)





Key Observations:

Gate Control: As the gate voltage becomes more negative (e.g., from Vg = -0.2 V to Vg = -0.6 V), the drain current increases significantly, demonstrating strong gate control over the tunneling current.

Saturation Behavior: The device shows a weak current saturation compared to a MOSFET. The current continues to increase with Vd, which is characteristic of TFETs where the drain bias influences the tunneling junction until all curves reach the same saturation level because this represents the maximum tunneling current the device can sustain, determined by the tunnel junction design and energy band engineering, not by the applied drain voltage beyond the saturation point.

This behavior demonstrates the fundamental current-driving limitation of tunneling-based transistors.

TFET vs MOSFET: Saturation Current Mechanism Comparison

Aspect	TFET	MOSFET
Saturation Cause	Band-to-band tunneling rate reaches maximum	Charge carrier velocity saturation
Physical Limitation	Quantum tunneling probability limit	Drift velocity limit in semiconductor
Current Transport	Tunneling through energy barrier	Drift/diffusion of charge carriers
Saturation Dependence	Energy band alignment optimization	Electric field strength in channel
Beyond Saturation	Additional voltage cannot enhance tunneling	Additional voltage cannot increase carrier velocity

Key Difference:

- **TFET**: Saturation occurs when the tunneling process reaches its quantum mechanical efficiency limit
- **MOSFET**: Saturation occurs when charge carriers reach their maximum drift velocity in the material

Common Result: Both devices show current saturation at high drain voltages, but the underlying physics is fundamentally different - quantum tunneling versus classical carrier transport.

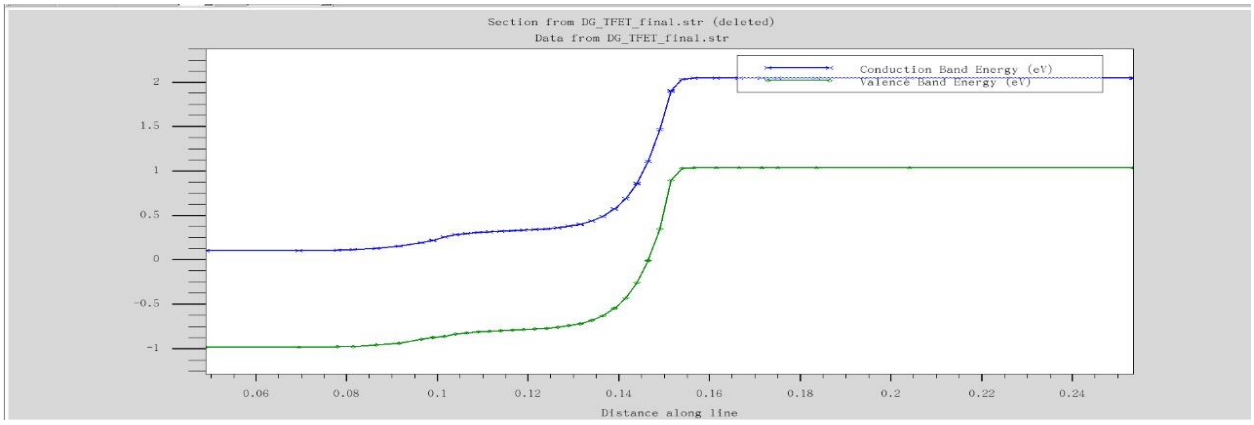
3.3 Internal Device Physics

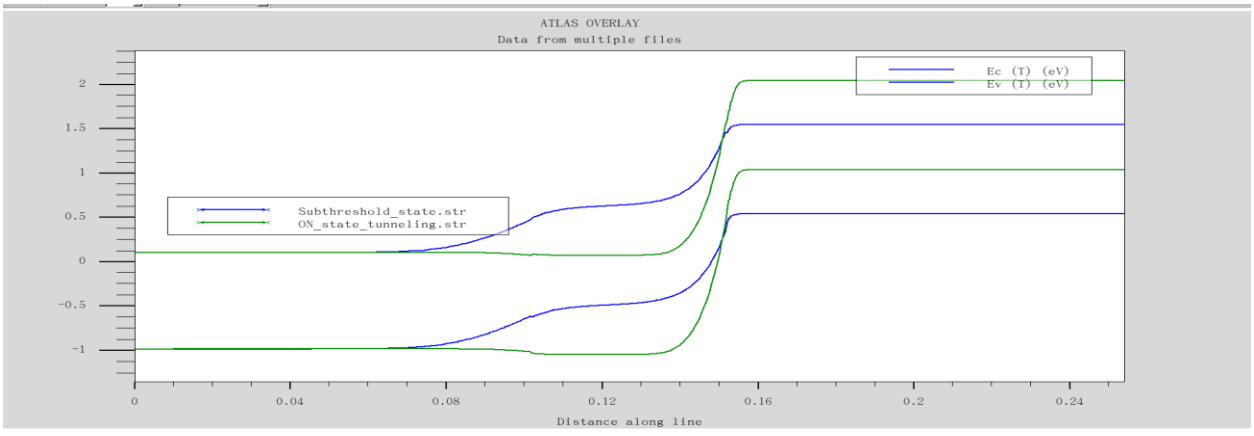
To understand the underlying mechanism, we analyze the internal physics through 1D cutlines across the device.

A. Energy Band Diagram

The energy band diagram is the most direct way to visualize the TFET's operation.

(Insert Image 6: Energy band diagram)



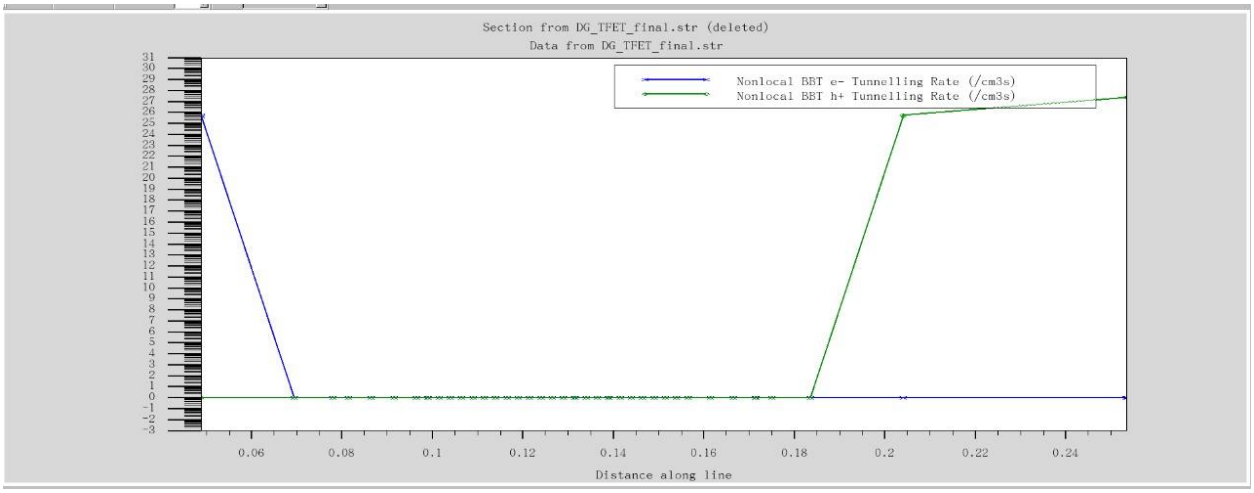


The plot shows the conduction band (Ec) and valence band (Ev) along the channel. In the ON state (negative Vg), the gate voltage pulls the bands in the channel upwards. This aligns the valence band of the p+ source with (or above) the conduction band of the channel, creating a very narrow tunneling barrier at the source-channel junction (around x = 0.1 µm). This alignment allows for efficient BTBT, turning the device ON.

B. Nonlocal Tunneling Rate

This plot directly confirms the location and magnitude of the BTBT generation.

(Nonlocal BTBT Tunneling Rate)

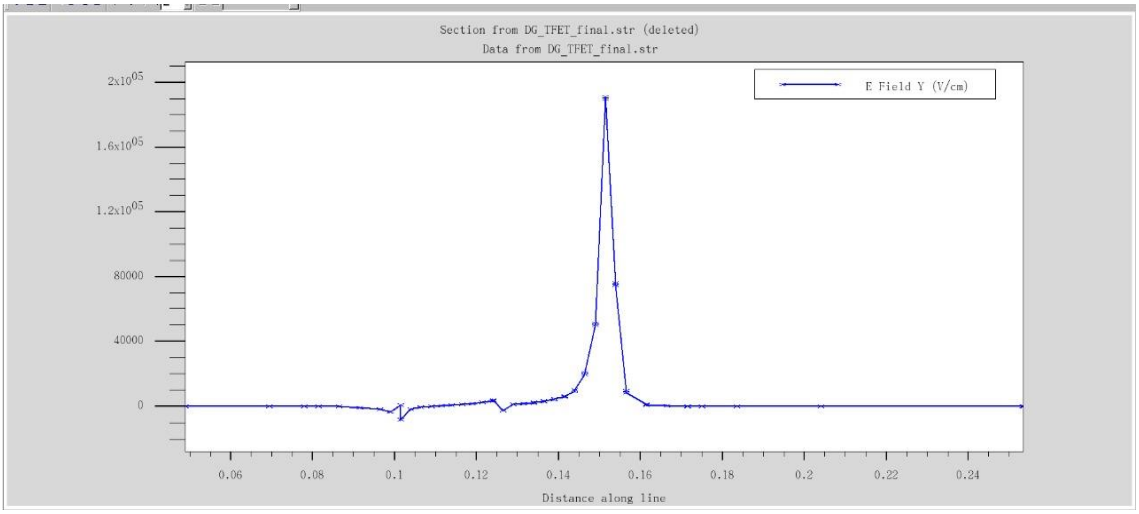


The plot shows a sharp peak in the electron (e-) and hole (h+) tunneling rates precisely at the source-channel junction. This confirms that the device current is indeed generated by band-to-band tunneling at this specific location, as controlled by the gate. The rate is negligible elsewhere in the device.

C. Electric Field

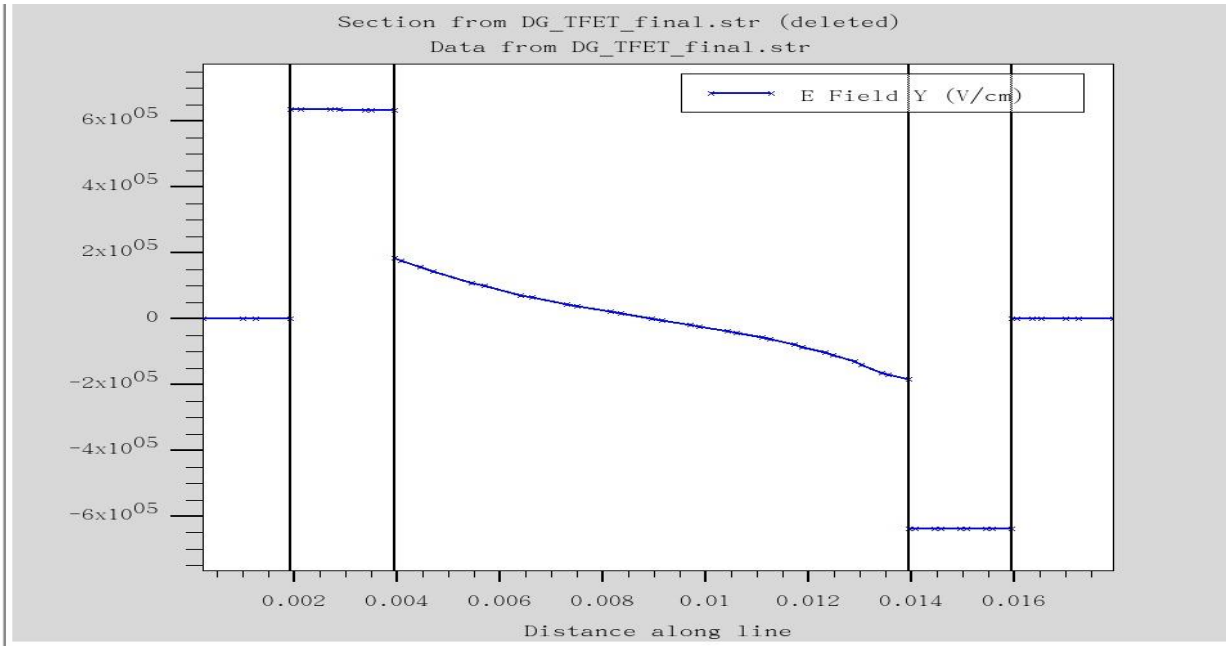
The electric field profile is critical to band bending and carrier transport.

(E Field Y plot)

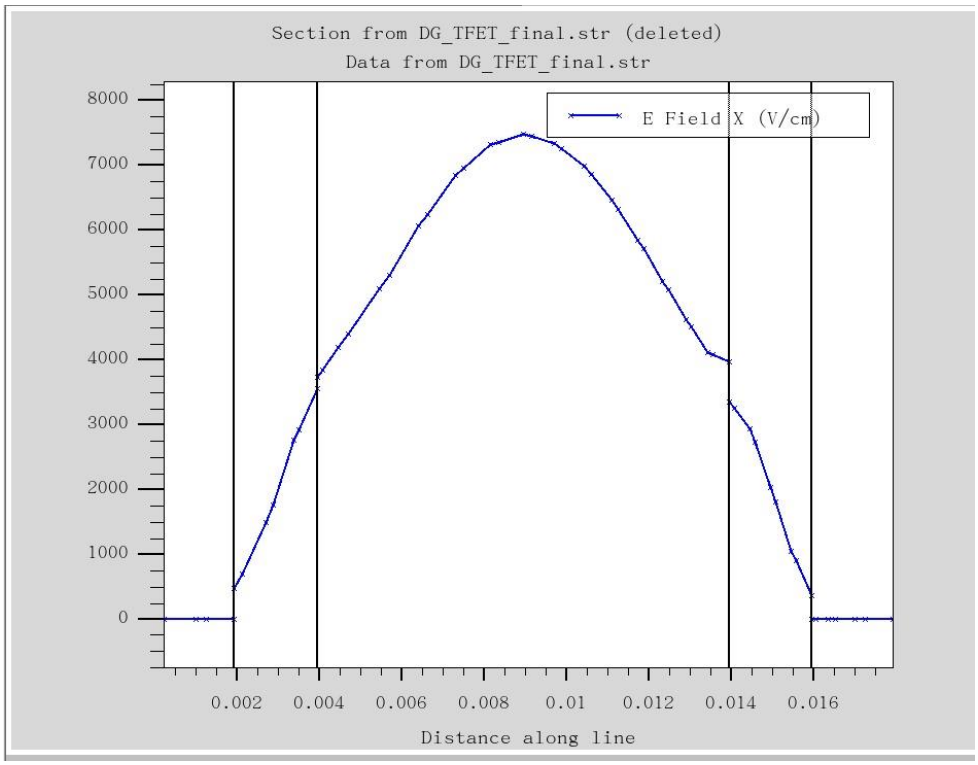


The vertical electric field (E Field Y) is highest near the gate, peaking at the source-channel junction. This high vertical field is responsible for bending the energy bands to enable tunneling. This highlights the excellent electrostatic control provided by the double-gate structure.

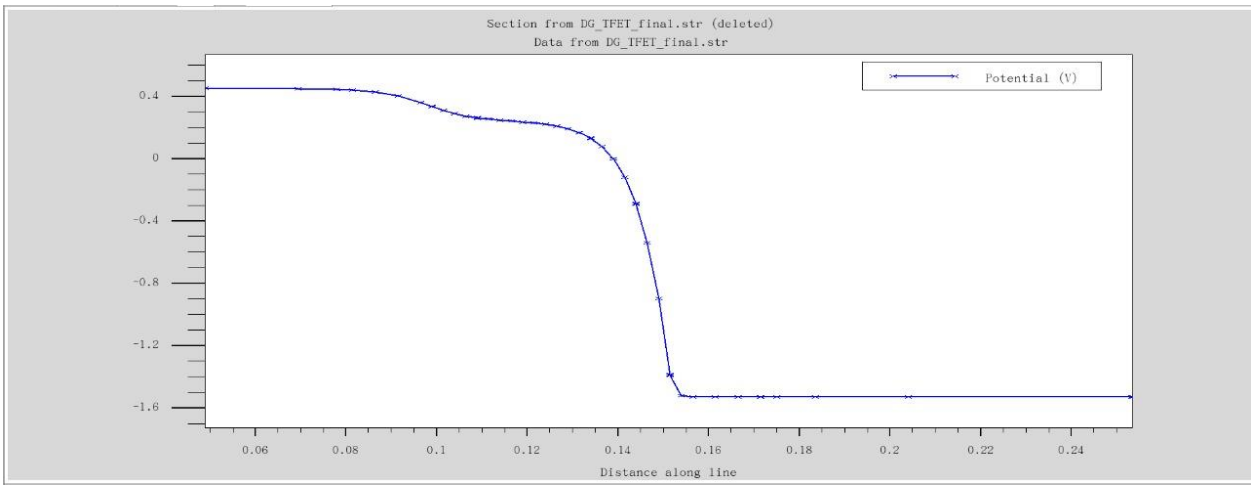
(Electric Field Y vertical cutline)



(Electric Field X vertical cutline)

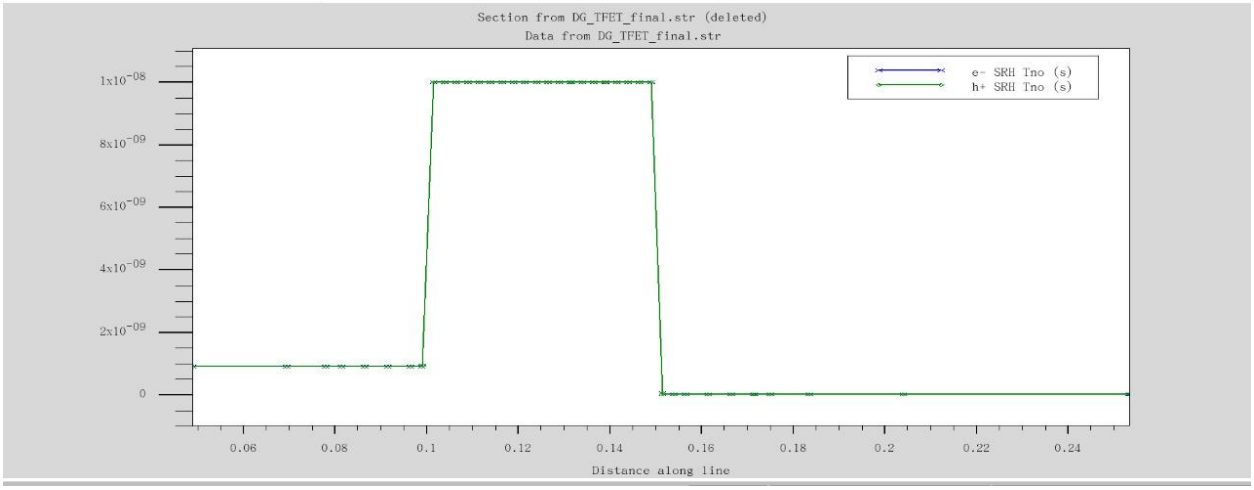


D.Electrostatic Potential Profile in DG-TFET



This figure shows the variation of electrostatic potential along the device length in a Double-Gate TFET. A sharp potential drop is observed near the source-channel junction (around 0.14 μm), indicating the tunneling region. The potential is relatively constant in the source and drain, highlighting strong gate control and effective junction formation essential for tunneling operation.

E.SRH Carrier Lifetime Distribution in DG-TFET



The plot displays the Shockley-Read-Hall (SRH) recombination lifetimes for electrons and holes across the TFET structure. A sharp increase in both lifetimes is observed between 0.1 µm and 0.14 µm, corresponding to the intrinsic or lightly doped channel region. The lower values in the source and drain regions indicate higher doping concentrations, which reduce carrier lifetimes due to increased recombination. This profile confirms proper doping design, with longer lifetimes in the tunneling region enhancing carrier availability for efficient tunneling.

4. Conclusion

This project successfully demonstrated the simulation of a p-channel Double-Gate TFET using Silvaco ATLAS. The analysis of the simulation results provided key insights into the device's operation and performance.

5.References

- **Kam, H., Liu, T. J. K., Markovic, D., Alon, E., & King, T. J.** (2007). *Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec*. IEEE Electron Device Letters, 28(7), 583-585. [First experimental demonstration of sub-60 mV/decade SS in silicon-based TFETs]
- **Vandenberghe, W. G., Verhulst, A. S., Groeseneken, G., Soree, B., & Magnus, W.** (2014). *Subthreshold-swing physics of tunnel field-effect transistors*. AIP Advances, 4(6), 067141. [Comprehensive study of subthreshold swing physics in TFETs]