RISCV32IM Single Cycle Processor, Verilog Implementation

Computer Architecture Fall 2023: MS1

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1 Overview

RISC-V is an open and extensible instruction set architecture (ISA) that has gained popularity in recent years due to its simplicity and flexibility. The RV32I and RV32M specifications provide the foundation for a basic 32-bit RISC-V processor with integer and multiply/divide instructions. We planned on implementing RV32IM spec for MS1.

2 Methodology

We started A top-down approach for our design, we figured the lab code required a lot of refactoring, so we rewrote most modules with proper best practices.

Most modules pass linting tests for Xilinix chips specifically virtex2 rule sets.

The Design is implemented as is in blockdiagram.pdf.

3 Implementation

Implementation was done in Verilog, and tested by either using Vivado or Gtkwave and Iverilog.

Appending the datapath for more instructions was a matter of adding multiplexer, adders or functionality to CU/ALU as outlined in the block diagram pdf.

4 Testing Methodology

Testing was done in increments, tests are put in tests folder along with gtkwave files if possible. We have tests for basic seven instruction done in lab, tests for loops, and R-format.

More tests where planned each having a specific purpose, but due to time constraints we opted to make one test encompassing all/other instructions (generaltest.txt). It however lacked testing for M-Spec instructions.

We were not able to test the processor on the FPGA due to time constraints, but we are confident that it will work as intended as it passed liniting tests.

4.1 Future testing objectives

Using Verilog's file interface we think we could make a more robust testing methodology, either a golden randomized self checking test-bench (which was in plan but was left blank due to time constraints), or a implement riscv un-official testing suite programs.

5 Results

All simulation results in repo as waveforms.

5.1 tested instructions

All instructions tested passed, except for M-Spec instructions which were not tested.