

# Combinational Circuit Design

Design the following circuits using Verilog **and create a testbench (directed or randomized)** for each design to check its functionality.

1)

Design a Verilog module that takes a 3-bit binary input (A[2:0]) and produces a corresponding encoded output (B[6:0]). The encoding method can be selected using a parameter called USE\_GRAY, which can be set to either 1 or 0. If USE\_GRAY is set to 1, the module should perform Gray encoding on the input. If USE\_GRAY is set to 0, the module should perform one-hot encoding on the input. Default value for USE\_GRAY = 1.

One-hot encoding is a way of representing data in a binary string in which only a single bit can be 1, while all others are 0.

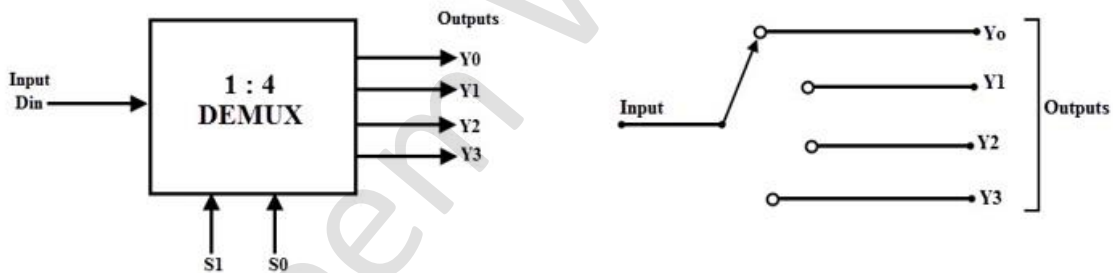
Gray encoding, also known as Gray code, is a binary numeral system where consecutive values differ by only one bit. In Gray encoding, each binary number is represented such that only one bit changes from one value to the next, reducing the possibility of errors during transitions.

Decimal	Binary	Gray code	One-hot
0	000	000	0000000
1	001	001	0000001
2	010	011	0000010
3	011	010	0000100
4	100	110	0001000
5	101	111	0010000
6	110	101	0100000
7	111	100	1000000

Write the Verilog code for this module and demonstrate its functionality using a testbench. Include the waveform diagram and simulation results in your submission.

2) Design a 1-to-4 demultiplexer (Demux) using Verilog. The demultiplexer should have a single input (D) and two select inputs (S[1:0]). The output should consist of four signals (Y[3:0]), where the input signal (D) is routed to one of the four outputs based on the select inputs. Write the Verilog code for this demultiplexer and simulate its functionality using a testbench.

Data Input	Select Inputs		Outputs			
D	S <sub>1</sub>	S <sub>0</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0



Deliverables: The assignment should be submitted as a PDF file with this format <your\_name>\_Assignment2 for example Kareem\_Waseem\_Assignment2\_Extended

Note that your document should be organized as 2 sections corresponding to each design above, and in each section, I am expecting the Verilog code for the design, testbench and the waveforms snippets