MIPS 16 (ASIC Project)

➢ Project Requirements

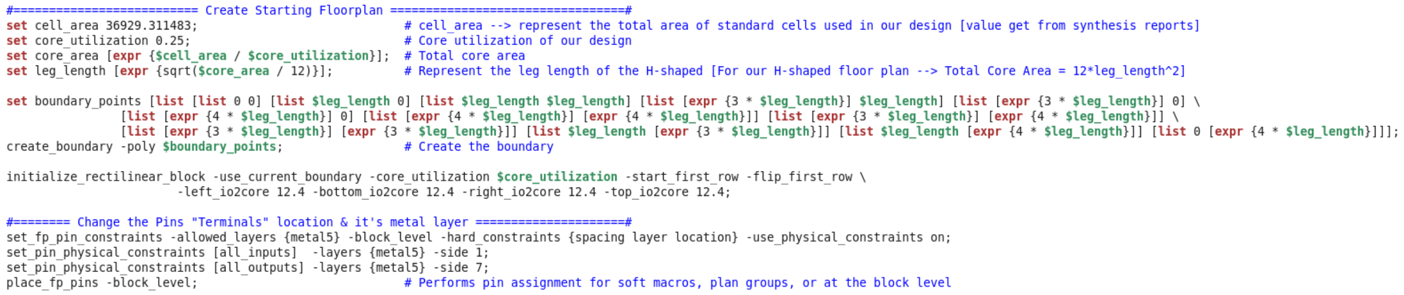
- ❖ Starting point should be clock period of **4ns** and core utilization equal to **0.25**
- ❖ Input delay and output delay are factors **(30%) from Clock Period**
- ❖ Clock uncertainties depend on the technology node, put it **0.35 ns**
- ❖ Core Area is **H-shaped**. Where the middle part of the H width is always as thick as left and right side combined
- ❖ Input pins placed on the **left side** & output pins placed on the **right side** (Pins locate at **metal5**)
- ❖ Maximum IR drop not to exceed **2%** (In our case supply voltage = 1.1 v, so **Max. IR drop = 22 mv**)
- ❖ **Formality is passing** (RTL vs pre-layout netlist and RTL vs post-layout netlist)
- ❖ Our Challenge & target is to run the design at the **fastest frequency** and the **smallest core area**

➢ First Trial (Clock period = 4 ns & Core utilization = 0.25)

- We know that $Core\ utilization\ = \frac{Total\ Standard\ cell\ Area}{Core\ Area} = \frac{36929.311483\ \mu m^2}{Core\ Area}$ where the total cell area is determined from the synthesis step. Therefore, we can determine the core Area easily as follow:

$$\boxed{Core\ Area = \frac{Total\ Standard\ cell\ Area}{core\ utilization} = \frac{36929.311483}{0.25} = 147717.2459\ \mu m^2}$$

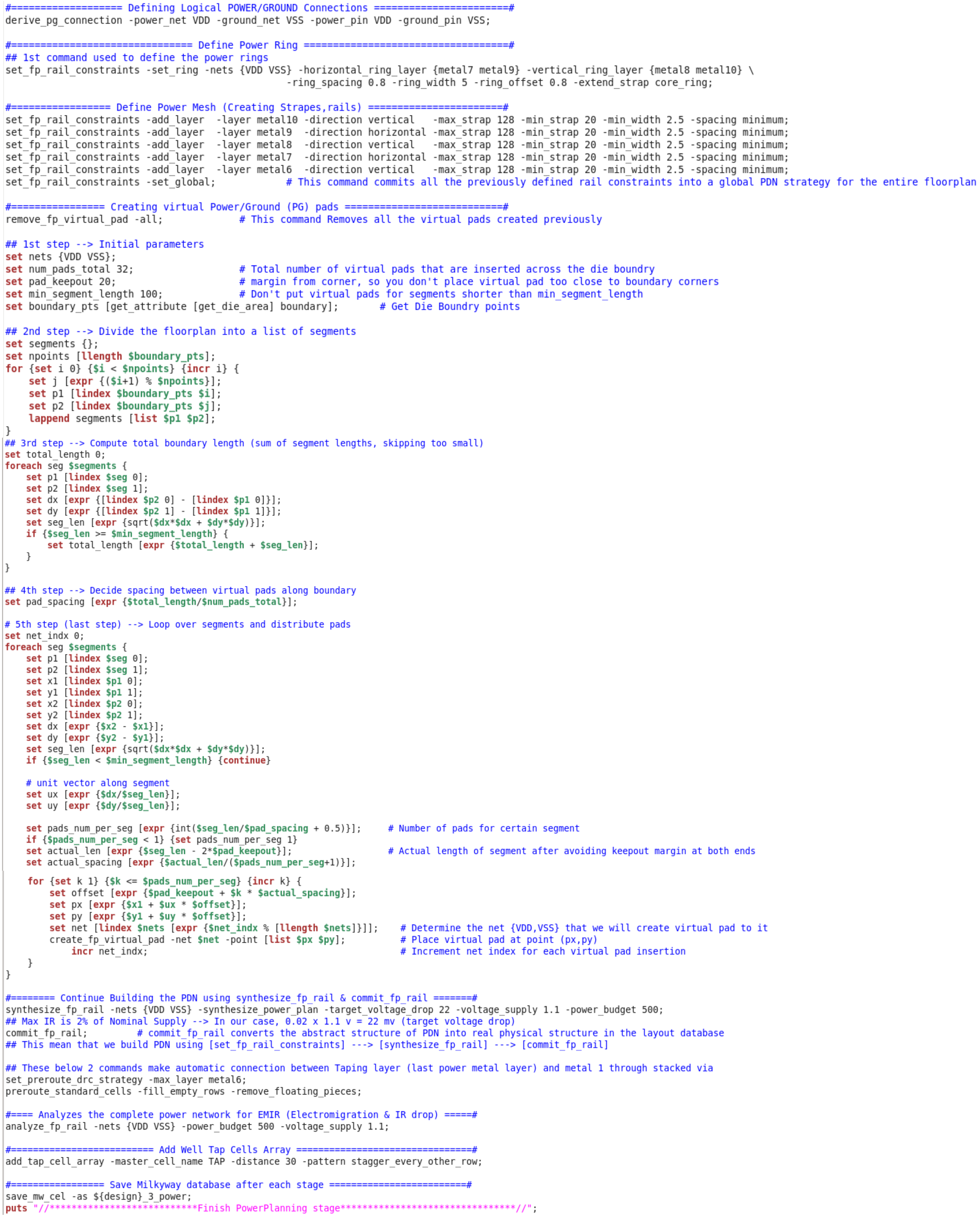
- Initially we define a generic H-shaped core region whose dimensions depend on the targeted core utilization. Input pins are arranged along the left side of this region, while output pins are placed along the right side, as shown in Figure (1)



```
#========================= Create Starting Floorplan ===============================#
set cell_area 36929.311483;                         # cell_area --> represent the total area of standard cells used in our design [value get from synthesis reports]
set core_utilization 0.25;                          # Core utilization of our design
set core_area [expr {$cell_area / $core_utilization}];  # Total core area
set leg_length [expr {sqrt($core_area / 12)}];      # Represent the leg length of the H-shaped [For our H-shaped floor plan --> Total Core Area = 12*leg_length^2]

set boundary_points [list [list 0 0] [list $leg_length 0] [list $leg_length $leg_length] [list [expr {3 * $leg_length}] $leg_length] [list [expr {3 * $leg_length}] 0] \
               [list [expr {4 * $leg_length}] 0] [list [expr {4 * $leg_length}] [expr {4 * $leg_length}]] [list [expr {3 * $leg_length}] [expr {4 * $leg_length}]] \
               [list [expr {3 * $leg_length}] [expr {3 * $leg_length}]] [list $leg_length [expr {3 * $leg_length}]] [list $leg_length [expr {4 * $leg_length}]] [list 0 [expr {4 * $leg_length}]]]];
create_boundary -poly $boundary_points;             # Create the boundary

initialize_rectilinear_block -use_current_boundary -core_utilization $core_utilization -start_first_row -flip_first_row \
                      -left_io2core 12.4 -bottom_io2core 12.4 -right_io2core 12.4 -top_io2core 12.4;

#======== Change the Pins "Terminals" location & it's metal layer ====================#
set_fp_pin_constraints -allowed_layers {metal5} -block_level -hard_constraints {spacing layer location} -use_physical_constraints on;
set_pin_physical_constraints [all_inputs]  -layers {metal5} -side 1;
set_pin_physical_constraints [all_outputs] -layers {metal5} -side 7;
place_fp_pins -block_level;                         # Performs pin assignment for soft macros, plan groups, or at the block level
```

Figure 1 : Create floorplan & place input/output pins

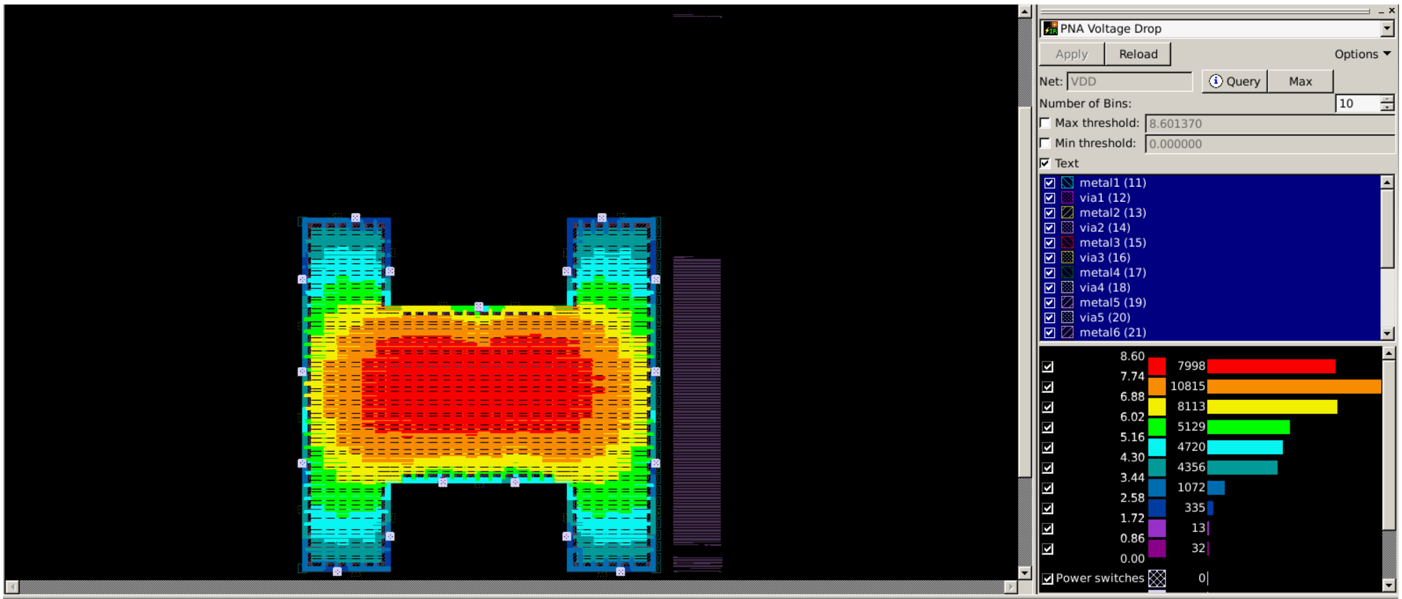
- After creating the floorplan, we directly create the power mesh on metal6 till metal10 & distribute the virtual pads along the core boundary as shown in figure (2)
  Total virtual pads = 32 → half of them is **VDD** & the other pads are **VSS**



```
#=================== Defining Logical POWER/GROUND Connections =======================#
derive_pg_connection -power_net VDD -ground_net VSS -power_pin VDD -ground_pin VSS;

#=============================== Define Power Ring ===================================#
## 1st command used to define the power rings
set_fp_rail_constraints -set_ring -nets {VDD VSS} -horizontal_ring_layer {metal7 metal9} -vertical_ring_layer {metal8 metal10} \
                                                 -ring_spacing 0.8 -ring_width 5 -ring_offset 0.8 -extend_strap core_ring;

#================= Define Power Mesh (Creating Strapes,rails) =======================#
set_fp_rail_constraints -add_layer  -layer metal10 -direction vertical   -max_strap 128 -min_strap 20 -min_width 2.5 -spacing minimum;
set_fp_rail_constraints -add_layer  -layer metal9  -direction horizontal -max_strap 128 -min_strap 20 -min_width 2.5 -spacing minimum;
set_fp_rail_constraints -add_layer  -layer metal8  -direction vertical   -max_strap 128 -min_strap 20 -min_width 2.5 -spacing minimum;
set_fp_rail_constraints -add_layer  -layer metal7  -direction horizontal -max_strap 128 -min_strap 20 -min_width 2.5 -spacing minimum;
set_fp_rail_constraints -add_layer  -layer metal6  -direction vertical   -max_strap 128 -min_strap 20 -min_width 2.5 -spacing minimum;
set_fp_rail_constraints -set_global;            # This command commits all the previously defined rail constraints into a global PDN strategy for the entire floorplan

#================ Creating virtual Power/Ground (PG) pads ===========================#
remove_fp_virtual_pad -all;             # This command Removes all the virtual pads created previously

## 1st step --> Initial parameters
set nets {VDD VSS};
set num_pads_total 32;                  # Total number of virtual pads that are inserted across the die boundry
set pad_keepout 20;                     # margin from corner, so you don't place virtual pad too close to boundary corners
set min_segment_length 100;             # Don't put virtual pads for segments shorter than min_segment_length
set boundary_pts [get_attribute [get_die_area] boundary];       # Get Die Boundry points

## 2nd step --> Divide the floorplan into a list of segments
set segments {};
set npoints [llength $boundary_pts];
for {set i 0} {$i < $npoints} {incr i} {
    set j [expr {($i+1) % $npoints}];
    set p1 [lindex $boundary_pts $i];
    set p2 [lindex $boundary_pts $j];
    lappend segments [list $p1 $p2];
}
## 3rd step --> Compute total boundary length (sum of segment lengths, skipping too small)
set total_length 0;
foreach seg $segments {
    set p1 [lindex $seg 0];
    set p2 [lindex $seg 1];
    set dx [expr {[lindex $p2 0] - [lindex $p1 0]}];
    set dy [expr {[lindex $p2 1] - [lindex $p1 1]}];
    set seg_len [expr {sqrt($dx*$dx + $dy*$dy)}];
    if {$seg_len >= $min_segment_length} {
        set total_length [expr {$total_length + $seg_len}];
    }
}

## 4th step --> Decide spacing between virtual pads along boundary
set pad_spacing [expr {$total_length/$num_pads_total}];

# 5th step (last step) --> Loop over segments and distribute pads
set net_indx 0;
foreach seg $segments {
    set p1 [lindex $seg 0];
    set p2 [lindex $seg 1];
    set x1 [lindex $p1 0];
    set y1 [lindex $p1 1];
    set x2 [lindex $p2 0];
    set y2 [lindex $p2 1];
    set dx [expr {$x2 - $x1}];
    set dy [expr {$y2 - $y1}];
    set seg_len [expr {sqrt($dx*$dx + $dy*$dy)}];
    if {$seg_len < $min_segment_length} {continue}

    # unit vector along segment
    set ux [expr {$dx/$seg_len}];
    set uy [expr {$dy/$seg_len}];

    set pads_num_per_seg [expr {int($seg_len/$pad_spacing + 0.5)}];     # Number of pads for certain segment
    if {$pads_num_per_seg < 1} {set pads_num_per_seg 1}
    set actual_len [expr {$seg_len - 2*$pad_keepout}];                  # Actual length of segment after avoiding keepout margin at both ends
    set actual_spacing [expr {$actual_len/($pads_num_per_seg+1)}];

    for {set k 1} {$k <= $pads_num_per_seg} {incr k} {
        set offset [expr {$pad_keepout + $k * $actual_spacing}];
        set px [expr {$x1 + $ux * $offset}];
        set py [expr {$y1 + $uy * $offset}];
        set net [lindex $nets [expr {$net_indx % [llength $nets]}]];    # Determine the net {VDD,VSS} that we will create virtual pad to it
        create_fp_virtual_pad -net $net -point [list $px $py];          # Place virtual pad at point (px,py)
            incr net_indx;                                              # Increment net index for each virtual pad insertion
    }
}

#======== Continue Building the PDN using synthesize_fp_rail & commit_fp_rail =======#
synthesize_fp_rail -nets {VDD VSS} -synthesize_power_plan -target_voltage_drop 22 -voltage_supply 1.1 -power_budget 500;
## Max IR is 2% of Nominal Supply --> In our case, 0.02 x 1.1 v = 22 mv (target voltage drop)
commit_fp_rail;         # commit_fp_rail converts the abstract structure of PDN into real physical structure in the layout database
## This mean that we build PDN using [set_fp_rail_constraints] ---> [synthesize_fp_rail] ---> [commit_fp_rail]

## These below 2 commands make automatic connection between Taping layer (last power metal layer) and metal 1 through stacked via
set_preroute_drc_strategy -max_layer metal6;
preroute_standard_cells -fill_empty_rows -remove_floating_pieces;

#==== Analyzes the complete power network for EMIR (Electromigration & IR drop) =====#
analyze_fp_rail -nets {VDD VSS} -power_budget 500 -voltage_supply 1.1;

#========================== Add Well Tap Cells Array ===============================#
add_tap_cell_array -master_cell_name TAP -distance 30 -pattern stagger_every_other_row;

#================= Save Milkyway database after each stage ========================#
save_mw_cel -as ${design}_3_power;
puts "//**************************Finish PowerPlanning stage********************************//";
```

Figure 2 : Creating power mesh & Automatic Virtual pads

- Here, we analyze the Maximum IR drop and the following figure "figure 3" ensure that we satisfy our target → $\boxed{\textit{maximum IR drop} \; = \; 8.6 \, mv \; (\leq 22 \, mv)}$



PNA Voltage Drop

Apply | Reload | Options ▾

Net: VDD | ⓘ Query | Max

Number of Bins: 10

☐ Max threshold: 8.601370

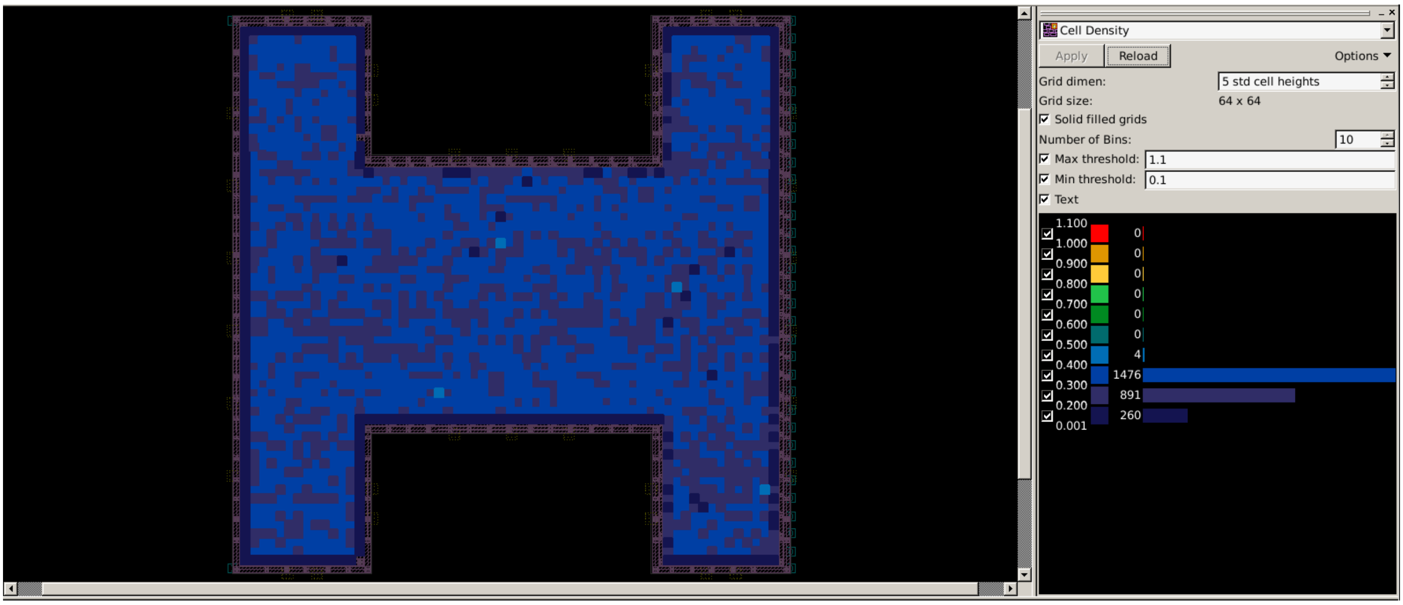
☐ Min threshold: 0.000000

☑ Text

☑ metal1 (11)
☑ via1 (12)
☑ metal2 (13)
☑ via2 (14)
☑ metal3 (15)
☑ via3 (16)
☑ metal4 (17)
☑ via4 (18)
☑ metal5 (19)
☑ via5 (20)
☑ metal6 (21)

Figure 3 : Voltage drop "IR drop"

- Once power planning is complete, we perform cell placement distributing all cells within the H-shaped core area. Then we inspect the resulting cell density (Figure 4) and pin density (Figure 5), to assess congestion and address any issues early, before proceeding to the routing



Cell Density

Apply | Reload | Options ▾

Grid dimen: 5 std cell heights

Grid size: 64 x 64

☑ Solid filled grids

Number of Bins: 10

☑ Max threshold: 1.1

☑ Min threshold: 0.1

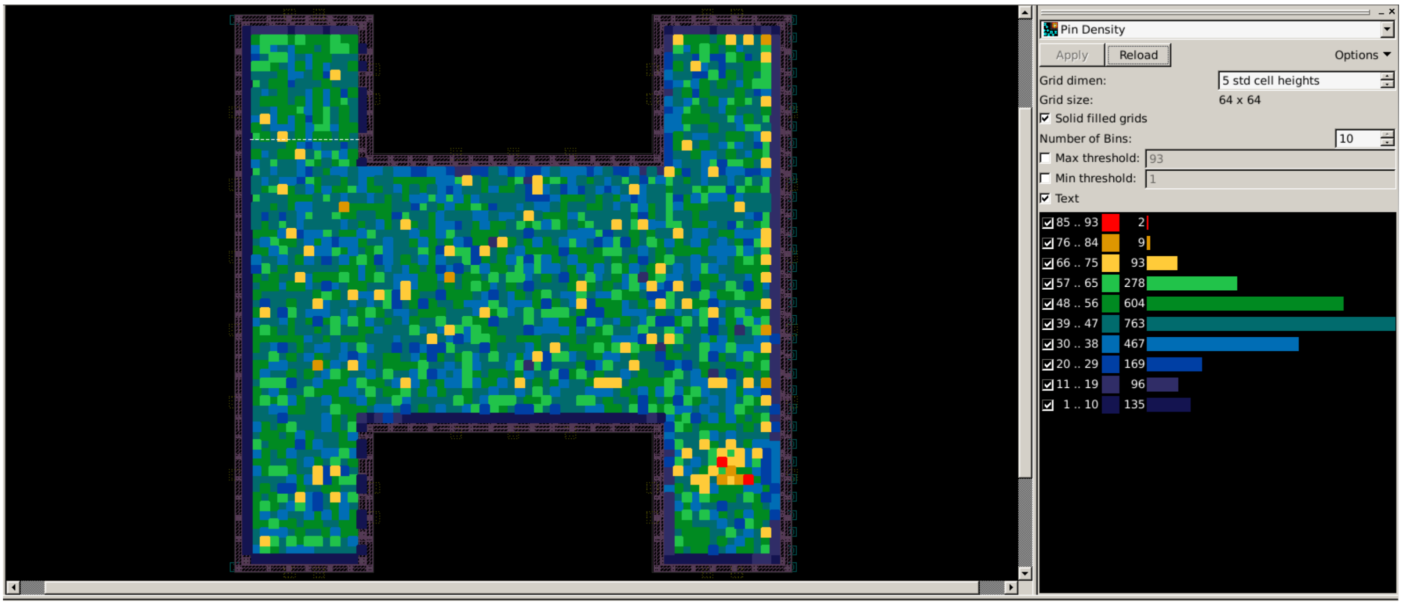
☑ Text

Figure 4 : Cell Density Map view

✓ In the above cell density map, the layout is divided into a grid of small windows, where for each window the cell density is computed as follows:

$$\boxed{\textbf{Cell density} = \frac{\textbf{Area of all standard cells that placed in certain window}}{\textbf{Window Area}}}$$

Therefore, our design is not congested as shown in the cell density view due to max. cell density ranges from **0.4 to 0.5** (Not congested design)



Grid dimen: 5 std cell heights
Grid size: 64 x 64
☑ Solid filled grids
Number of Bins: 10
□ Max threshold: 93
□ Min threshold: 1
☑ Text

☑ 85 .. 93 🟥 2
☑ 76 .. 84 🟧 9
☑ 66 .. 75 🟨 93
☑ 57 .. 65 🟩 278
☑ 48 .. 56 🟩 604
☑ 39 .. 47 🟦 763
☑ 30 .. 38 🟦 467
☑ 20 .. 29 🟦 169
☑ 11 .. 19 🟪 96
☑ 1 .. 10 🟪 135

Figure 5 : Pin Density Map view

- ✓ Form the pin density map view, we can notice that the **right region of the H-shaped** has **high pin density**. The reason behind that **is all the output pins are concentrated there** which can cause routing difficulty even if the cell density is good because many nets originate or terminate in that region increasing pin-to-pin routing demand

- After completing placement, we proceed with CTS and routing, which initially produced nine DRC violations caused by the high pin density on the right side of the H-shaped region, as expected. **These were resolved by repositioning the standard cells connected to the output pins closer to those pins**

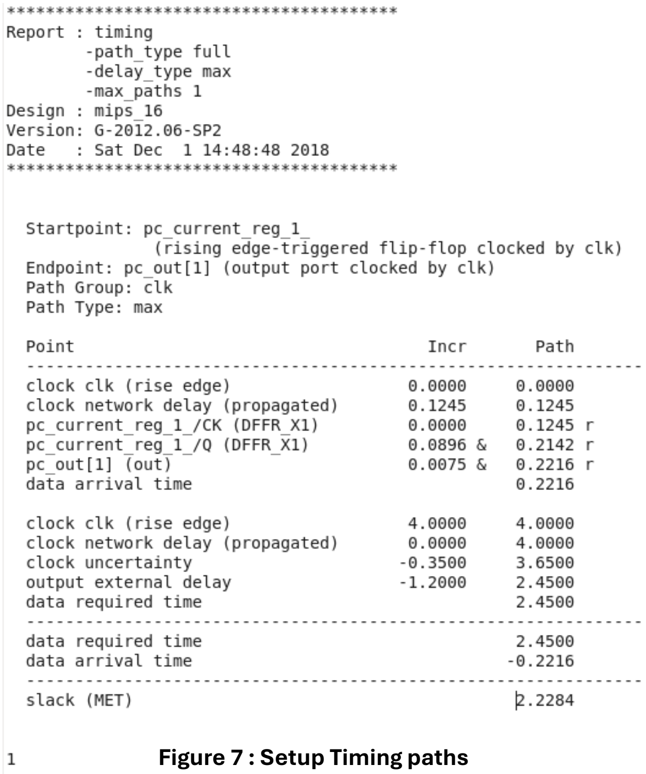
❖ Timing Sign-off Results

1. **Fast, Fast corner** → Initially, in this corner there are **no setup violations** exist but there are many hold violations (**16 paths are hold violated**). Therefore, we solve all these hold violations automatically by **resizing the cells** and **inserting buffers (BUF_X4, BUF_X8)**

- **Finally, we meet our timing constraints without any violations**

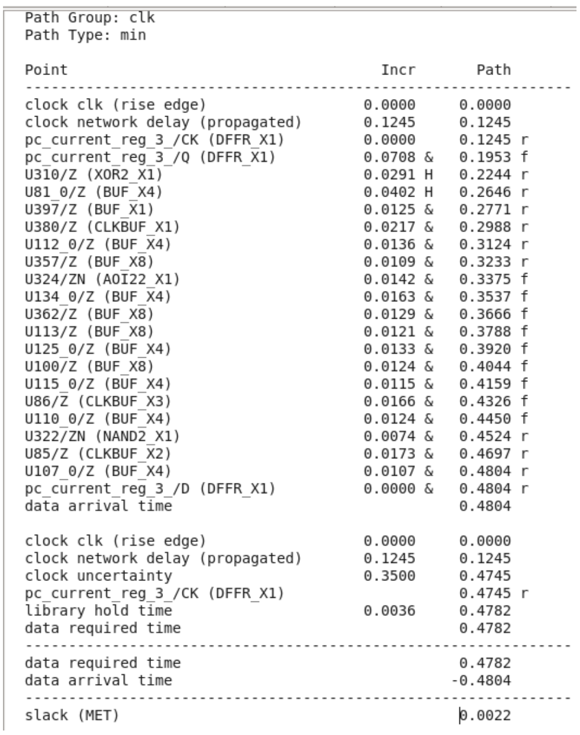
✓ **Worst setup Slack = 2.2284 ns**

✓ **Worst Hold Slack = 0.0022 ns**



```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : mips_16
Version: G-2012.06-SP2
Date   : Sat Dec  1 14:48:48 2018
****************************************


  Startpoint: pc_current_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[1] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  clock clk (rise edge)                  0.0000     0.0000
  clock network delay (propagated)       0.1245     0.1245
  pc_current_reg_1_/CK (DFFR_X1)         0.0000     0.1245 r
  pc_current_reg_1_/Q (DFFR_X1)          0.0896 &   0.2142 r
  pc_out[1] (out)                        0.0075 &   0.2216 r
  data arrival time                                 0.2216

  clock clk (rise edge)                  4.0000     4.0000
  clock network delay (propagated)       0.0000     4.0000
  clock uncertainty                     -0.3500     3.6500
  output external delay                 -1.2000     2.4500
  data required time                                2.4500
  ---------------------------------------------------------------
  data required time                                2.4500
  data arrival time                                -0.2216
  ---------------------------------------------------------------
  slack (MET)                                       2.2284

1
```

Figure 7 : Setup Timing paths



```
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  ---------------------------------------------------------------
  clock clk (rise edge)                  0.0000     0.0000
  clock network delay (propagated)       0.1245     0.1245
  pc_current_reg_3_/CK (DFFR_X1)         0.0000     0.1245 r
  pc_current_reg_3_/Q (DFFR_X1)          0.0708 &   0.1953 f
  U310/Z (XOR2_X1)                       0.0291 H   0.2244 r
  U81_0/Z (BUF_X4)                       0.0402 H   0.2646 r
  U397/Z (BUF_X1)                        0.0125 &   0.2771 r
  U380/Z (CLKBUF_X1)                     0.0217 &   0.2988 r
  U112_0/Z (BUF_X4)                      0.0136 &   0.3124 r
  U357/Z (BUF_X8)                        0.0109 &   0.3233 r
  U324/ZN (AOI22_X1)                     0.0142 &   0.3375 f
  U134_0/Z (BUF_X4)                      0.0163 &   0.3537 f
  U362/Z (BUF_X8)                        0.0129 &   0.3666 f
  U113/Z (BUF_X8)                        0.0121 &   0.3788 f
  U125_0/Z (BUF_X4)                      0.0133 &   0.3920 f
  U100/Z (BUF_X8)                        0.0124 &   0.4044 f
  U115_0/Z (BUF_X4)                      0.0115 &   0.4159 f
  U86/Z (CLKBUF_X3)                      0.0166 &   0.4326 f
  U110_0/Z (BUF_X4)                      0.0124 &   0.4450 f
  U322/ZN (NAND2_X1)                     0.0074 &   0.4524 r
  U85/Z (CLKBUF_X2)                      0.0173 &   0.4697 r
  U107_0/Z (BUF_X4)                      0.0107 &   0.4804 r
  pc_current_reg_3_/D (DFFR_X1)          0.0000 &   0.4804 r
  data arrival time                                 0.4804

  clock clk (rise edge)                  0.0000     0.0000
  clock network delay (propagated)       0.1245     0.1245
  clock uncertainty                      0.3500     0.4745
  pc_current_reg_3_/CK (DFFR_X1)                    0.4745 r
  library hold time                      0.0036     0.4782
  data required time                                0.4782
  ---------------------------------------------------------------
  data required time                                0.4782
  data arrival time                                -0.4804
  ---------------------------------------------------------------
  slack (MET)                                       0.0022
```

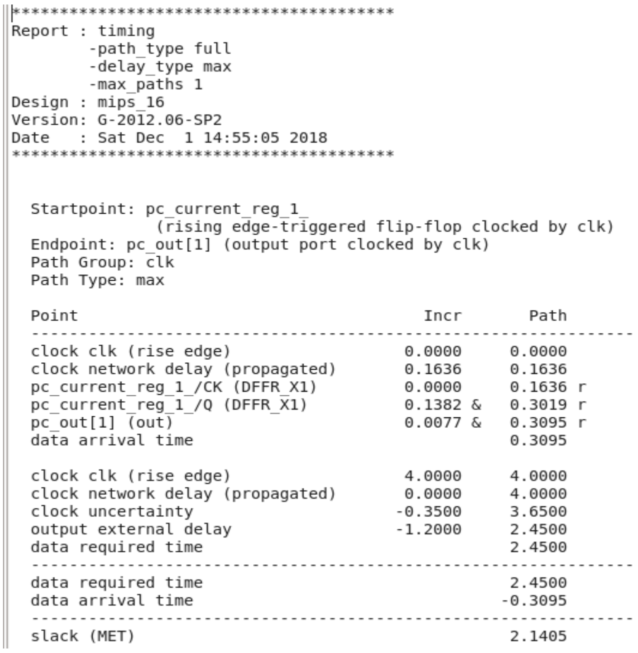
Figure 6 : Hold Timing paths

2. **Slow, Slow corner** → Initially, in this corner there are **no setup violations** exist but there are hold violations (**2 paths only are hold violated**). Therefore, we solve these hold violations automatically by **resizing the cells** and **inserting buffers (BUF_X2, BUF_X4)**

- **Finally, we meet our timing constraints without any violations**

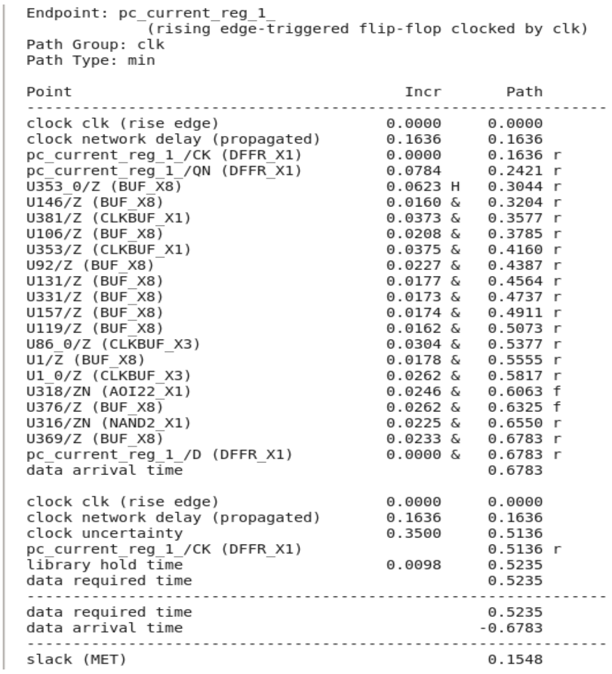
✓ **Worst setup Slack = 2.1405 ns**

✓ **Worst Hold Slack = 0.1548 ns**



```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : mips_16
Version: G-2012.06-SP2
Date   : Sat Dec  1 14:55:05 2018
****************************************


  Startpoint: pc_current_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_out[1] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  clock clk (rise edge)                  0.0000     0.0000
  clock network delay (propagated)       0.1636     0.1636
  pc_current_reg_1_/CK (DFFR_X1)         0.0000     0.1636 r
  pc_current_reg_1_/Q (DFFR_X1)          0.1382 &   0.3019 r
  pc_out[1] (out)                        0.0077 &   0.3095 r
  data arrival time                                 0.3095

  clock clk (rise edge)                  4.0000     4.0000
  clock network delay (propagated)       0.0000     4.0000
  clock uncertainty                     -0.3500     3.6500
  output external delay                 -1.2000     2.4500
  data required time                                2.4500
  ---------------------------------------------------------------
  data required time                                2.4500
  data arrival time                                -0.3095
  ---------------------------------------------------------------
  slack (MET)                                       2.1405
```

Figure 9 : Setup Timing paths



```
  Endpoint: pc_current_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  ---------------------------------------------------------------
  clock clk (rise edge)                  0.0000     0.0000
  clock network delay (propagated)       0.1636     0.1636
  pc_current_reg_1_/CK (DFFR_X1)         0.0000     0.1636 r
  pc_current_reg_1_/QN (DFFR_X1)         0.0784     0.2421 r
  U353_0/Z (BUF_X8)                      0.0623 H   0.3044 r
  U146/Z (BUF_X8)                        0.0160 &   0.3204 r
  U381/Z (CLKBUF_X1)                     0.0373 &   0.3577 r
  U106/Z (BUF_X8)                        0.0208 &   0.3785 r
  U353/Z (CLKBUF_X1)                     0.0375 &   0.4160 r
  U92/Z (BUF_X8)                         0.0227 &   0.4387 r
  U131/Z (BUF_X8)                        0.0177 &   0.4564 r
  U331/Z (BUF_X8)                        0.0173 &   0.4737 r
  U157/Z (BUF_X8)                        0.0174 &   0.4911 r
  U119/Z (BUF_X8)                        0.0162 &   0.5073 r
  U86_0/Z (CLKBUF_X3)                    0.0304 &   0.5377 r
  U1/Z (BUF_X8)                          0.0178 &   0.5555 r
  U1_0/Z (CLKBUF_X3)                     0.0262 &   0.5817 r
  U318/ZN (AOI22_X1)                     0.0246 &   0.6063 f
  U376/Z (BUF_X8)                        0.0262 &   0.6325 f
  U316/ZN (NAND2_X1)                     0.0225 &   0.6550 r
  U369/Z (BUF_X8)                        0.0233 &   0.6783 r
  pc_current_reg_1_/D (DFFR_X1)          0.0000 &   0.6783 r
  data arrival time                                 0.6783

  clock clk (rise edge)                  0.0000     0.0000
  clock network delay (propagated)       0.1636     0.1636
  clock uncertainty                      0.3500     0.5136
  pc_current_reg_1_/CK (DFFR_X1)                    0.5136 r
  library hold time                      0.0098     0.5235
  data required time                                0.5235
  ---------------------------------------------------------------
  data required time                                0.5235
  data arrival time                                -0.6783
  ---------------------------------------------------------------
  slack (MET)                                       0.1548
```

Figure 8 : Hold Timing paths

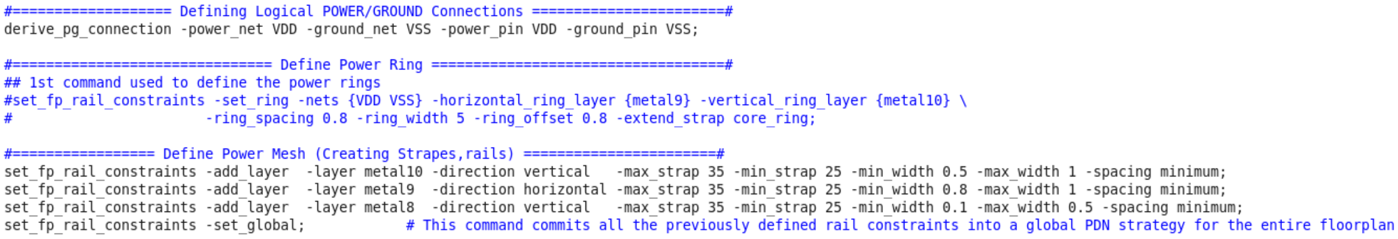
➢ Second Trial (Clock period = 2 ns & Core utilization = 0.4)

- Here, we can determine the core Area as follow:

$$\boxed{Core\ Area = \frac{Total\ Standard\ cell\ Area}{core\ utilization} = \frac{36929.311483}{0.4} = 92323.27871\ \mu m^2}$$

- After generating the floorplan, we immediately build the power mesh from metal8 through metal10, reducing both the number and width of power straps. Since higher core utilization (smaller Core Area) increases congestion, so the power grid is intentionally relaxed to free up additional routing resources as shown in the below script (figure 10)

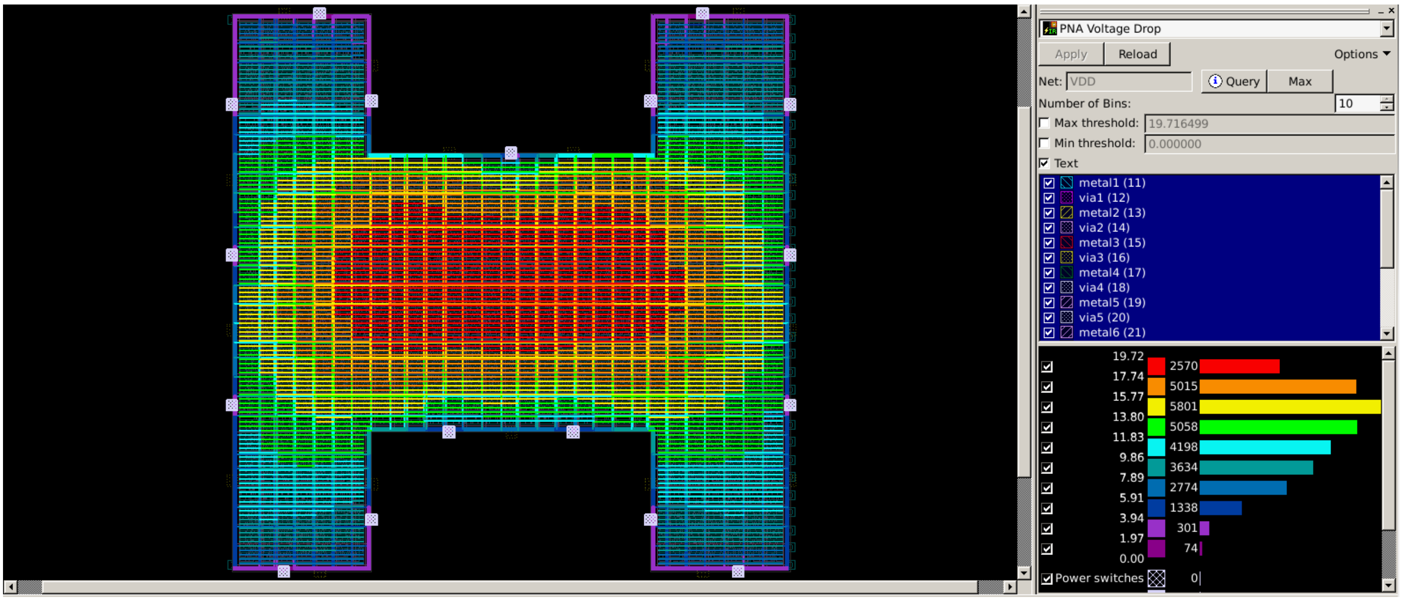
- In addition to that we remove the power ring as in small and low-power designs, the power mesh can directly connect to virtual power pads directly **without** needing a separate ring



```
#================== Defining Logical POWER/GROUND Connections ======================#
derive_pg_connection -power_net VDD -ground_net VSS -power_pin VDD -ground_pin VSS;

#============================== Define Power Ring ==================================#
## 1st command used to define the power rings
#set_fp_rail_constraints -set_ring -nets {VDD VSS} -horizontal_ring_layer {metal9} -vertical_ring_layer {metal10} \
#                        -ring_spacing 0.8 -ring_width 5 -ring_offset 0.8 -extend_strap core_ring;

#================ Define Power Mesh (Creating Strapes,rails) ======================#
set_fp_rail_constraints -add_layer  -layer metal10 -direction vertical   -max_strap 35 -min_strap 25 -min_width 0.5 -max_width 1 -spacing minimum;
set_fp_rail_constraints -add_layer  -layer metal9  -direction horizontal -max_strap 35 -min_strap 25 -min_width 0.8 -max_width 1 -spacing minimum;
set_fp_rail_constraints -add_layer  -layer metal8  -direction vertical   -max_strap 35 -min_strap 25 -min_width 0.1 -max_width 0.5 -spacing minimum;
set_fp_rail_constraints -set_global;           # This command commits all the previously defined rail constraints into a global PDN strategy for the entire floorplan
```

Figure 10 : Power mesh changes

- Here, we analyze the Maximum IR drop and the following figure “figure 11” ensure that we still satisfy our target → $\boxed{maximum\ IR\ drop\ =\ 19.72\ mv\ (\le 22\ mv)}$



PNA Voltage Drop

Net: VDD

Number of Bins: 10

☐ Max threshold: 19.716499

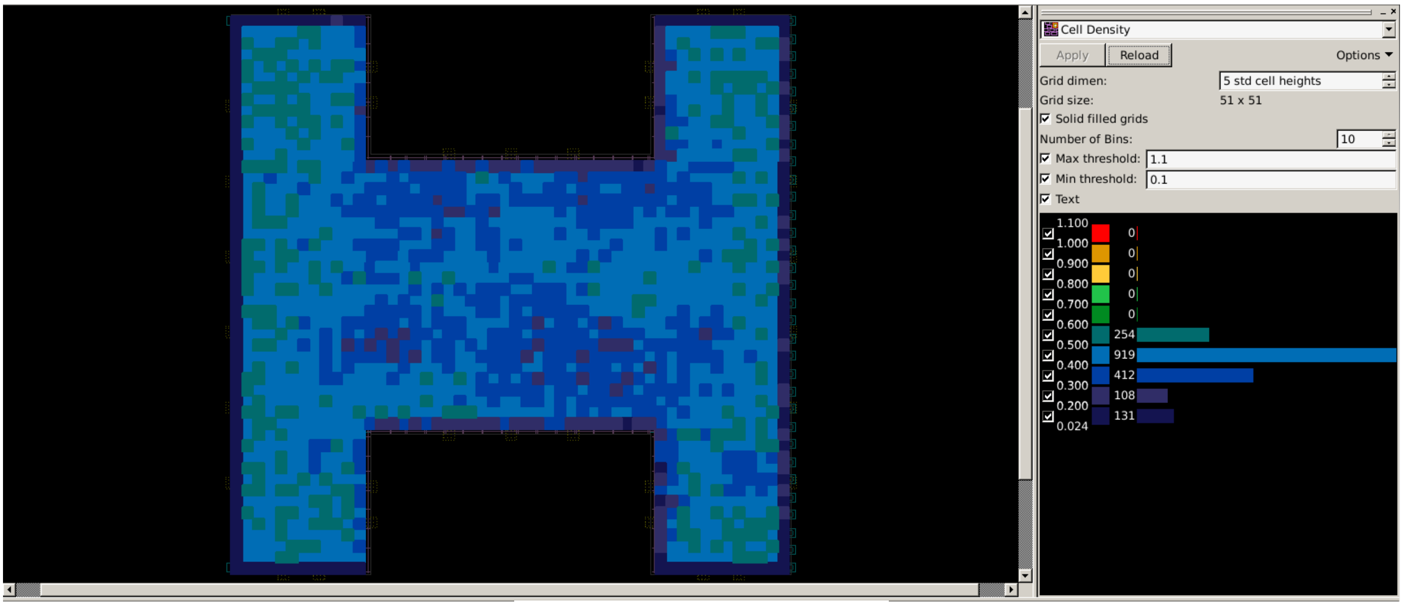
☐ Min threshold: 0.000000

☑ Text

Figure 11 : Voltage drop "IR drop"

❖ **Note: Maximum IR drop is very high as we expect due to that the power mesh is very weak**

- Once power planning is complete, we perform cell placement distributing all cells within the H-shaped core area. Then we inspect the resulting cell density map, pin density map and global routing congestion map to assess congestion and address any issues early, before routing.



Cell Density

Apply | Reload | Options

Grid dimen: 5 std cell heights

Grid size: 51 x 51

☑ Solid filled grids

Number of Bins: 10

☑ Max threshold: 1.1

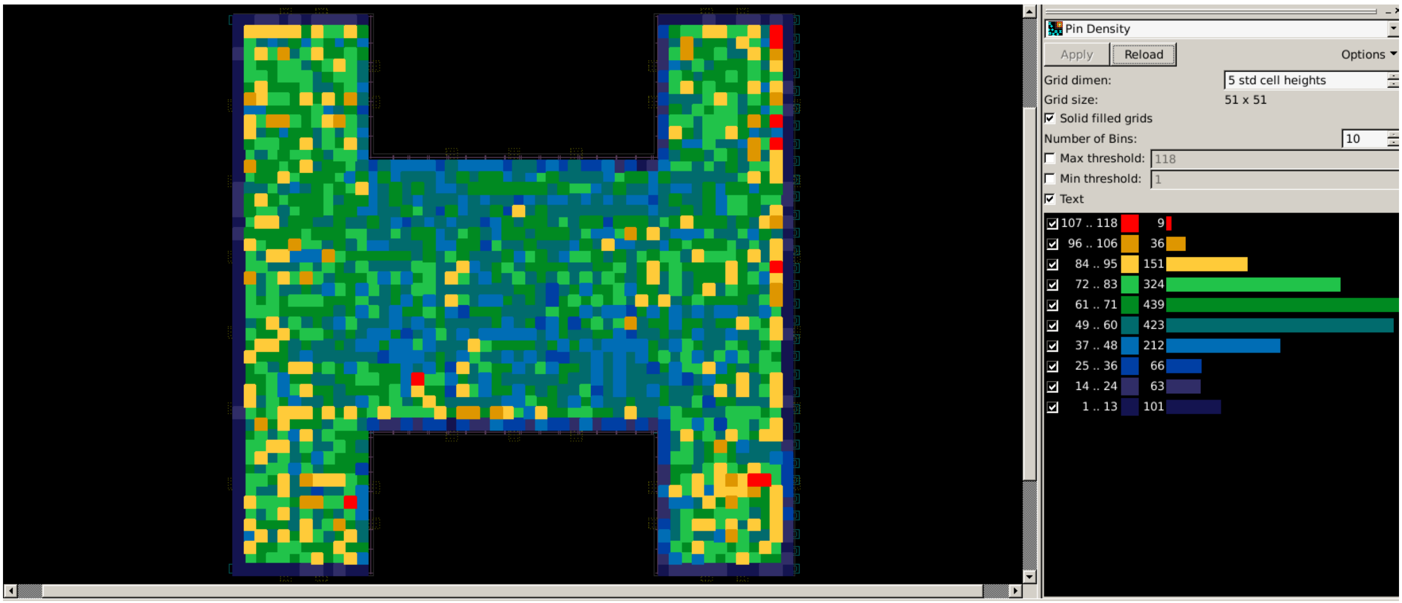
☑ Min threshold: 0.1

☑ Text

	Range		Count
☑	1.100 – 1.000	🟥	0
☑	1.000 – 0.900	🟧	0
☑	0.900 – 0.800	🟨	0
☑	0.800 – 0.700	🟩	0
☑	0.700 – 0.600	🟩	0
☑	0.600 – 0.500	🟦	254
☑	0.500 – 0.400	🟦	919
☑	0.400 – 0.300	🟦	412
☑	0.300 – 0.200	🟪	108
☑	0.200 – 0.024	🟪	131

Figure 12 : Cell Density Map view

✓ From the cell density map, we notice that our design is not congested as the max. cell density ranges from **0.5 to 0.6** (Moderate congested design)



Pin Density

Apply | Reload | Options

Grid dimen: 5 std cell heights

Grid size: 51 x 51

☑ Solid filled grids

Number of Bins: 10

☐ Max threshold: 118

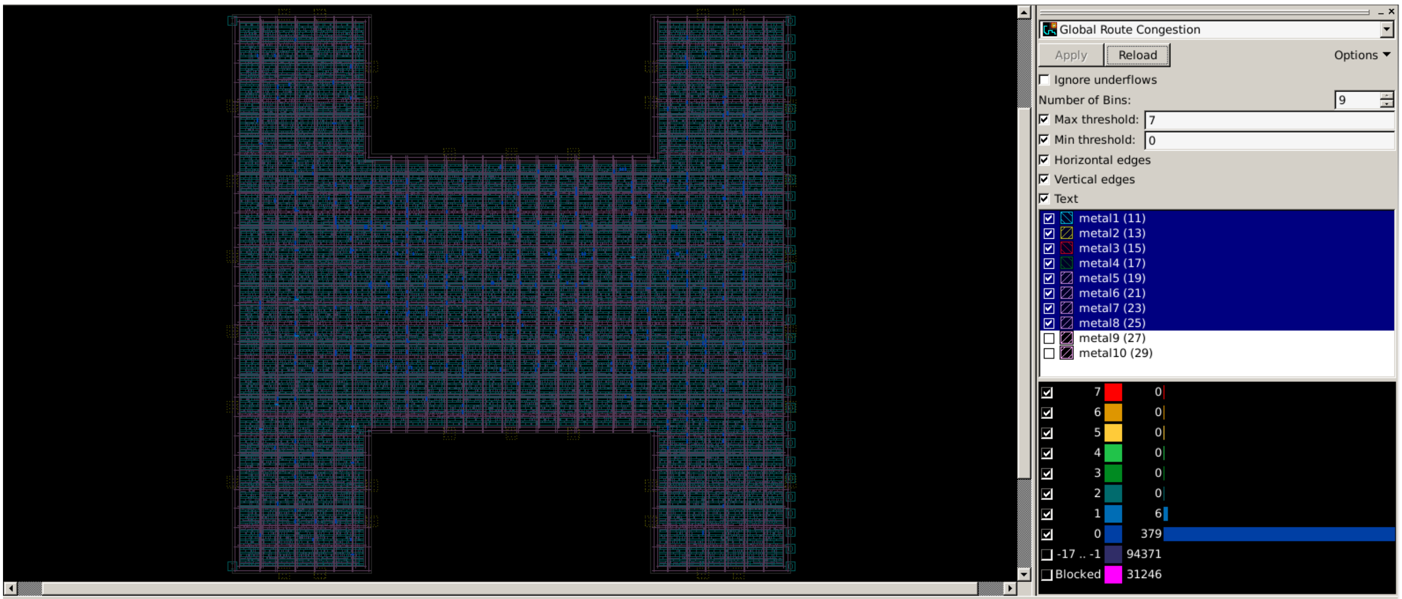
☐ Min threshold: 1

☑ Text

	Range		Count
☑	107 .. 118	🟥	9
☑	96 .. 106	🟧	36
☑	84 .. 95	🟨	151
☑	72 .. 83	🟩	324
☑	61 .. 71	🟩	439
☑	49 .. 60	🟦	423
☑	37 .. 48	🟦	212
☑	25 .. 36	🟦	66
☑	14 .. 24	🟪	63
☑	1 .. 13	🟪	101

Figure 13 : Pin Density Map view

✓ Form the pin density map, we notice that the whole core area has very high pin density especially at **right region of the H-shaped** due to the concentration of **all output pins** there which cause routing difficulty because many nets originate or terminate in that region increasing pin-to-pin routing demand [Max. pin density range from **107** to **118**]



Global Route Congestion

Apply | Reload | Options

□ Ignore underflows

Number of Bins: 9

☑ Max threshold: 7

☑ Min threshold: 0

☑ Horizontal edges

☑ Vertical edges

☑ Text

☑ metal1 (11)
☑ metal2 (13)
☑ metal3 (15)
☑ metal4 (17)
☑ metal5 (19)
☑ metal6 (21)
☑ metal7 (23)
☑ metal8 (25)
□ metal9 (27)
□ metal10 (29)

☑	7	🟥	0
☑	6	🟧	0
☑	5	🟨	0
☑	4	🟩	0
☑	3	🟩	0
☑	2	🟦	0
☑	1	🟦	6
☑	0	🟦	379
□	-17 .. -1	🟪	94371
□	Blocked	🟪	31246

Figure 14 : Global Route Congestion Map

- ✓ The global routing map shows overflow in only six grid windows, while all remaining grids are clear. Based on this, we move forward with the CTS and routing stages.

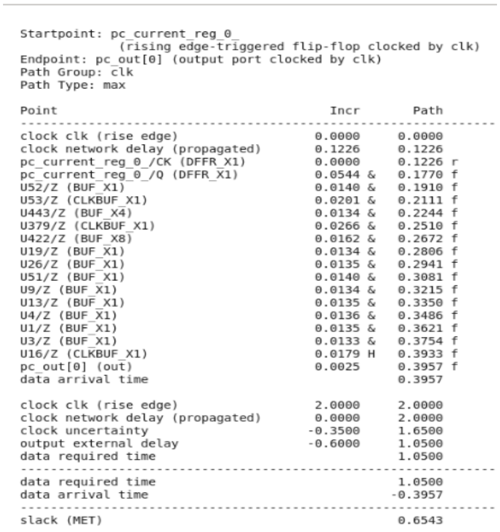
❖ Timing Sign-off Results

1. **Fast, Fast corner** → Initially, in this corner there are **no setup violations** exist but there are many hold violations (**16 paths are hold violated**). Therefore, we solve all these hold violations automatically by **resizing the cells** and **inserting buffers (BUF_X1, BUF_X2, BUF_X4, BUF_X8)**

- **Finally, we meet our timing constraints without any violations**

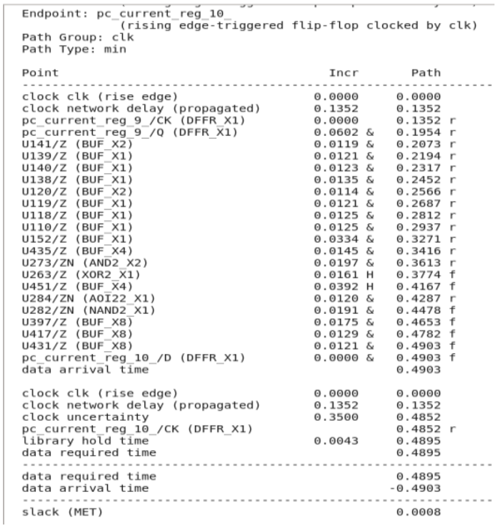
✓ **Worst setup Slack = 0.6543 ns**

✓ **Worst Hold Slack = 0.0008 ns**



```
Startpoint: pc_current_reg_0_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: pc_out[0] (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                      Incr       Path
--------------------------------------------------------------
clock clk (rise edge)                    0.0000     0.0000
clock network delay (propagated)         0.1226     0.1226
pc_current_reg_0_/CK (DFFR_X1)           0.0000     0.1226 r
pc_current_reg_0_/Q (DFFR_X1)            0.0544 &   0.1770 f
U52/Z (BUF_X1)                           0.0140 &   0.1910 f
U53/Z (CLKBUF_X1)                        0.0201 &   0.2111 f
U443/Z (BUF_X4)                          0.0134 &   0.2244 f
U379/Z (CLKBUF_X1)                       0.0266 &   0.2510 f
U422/Z (BUF_X8)                          0.0162 &   0.2672 f
U19/Z (BUF_X1)                           0.0134 &   0.2806 f
U26/Z (BUF_X1)                           0.0135 &   0.2941 f
U51/Z (BUF_X1)                           0.0140 &   0.3081 f
U9/Z (BUF_X1)                            0.0134 &   0.3215 f
U13/Z (BUF_X1)                           0.0135 &   0.3350 f
U4/Z (BUF_X1)                            0.0136 &   0.3486 f
U1/Z (BUF_X1)                            0.0135 &   0.3621 f
U3/Z (BUF_X1)                            0.0133 &   0.3754 f
U16/Z (CLKBUF_X1)                        0.0179 H   0.3933 f
pc_out[0] (out)                          0.0025     0.3957 f
data arrival time                                   0.3957

clock clk (rise edge)                    2.0000     2.0000
clock network delay (propagated)         0.0000     2.0000
clock uncertainty                       -0.3500     1.6500
output external delay                   -0.6000     1.0500
data required time                                  1.0500
--------------------------------------------------------------
data required time                                  1.0500
data arrival time                                  -0.3957
--------------------------------------------------------------
slack (MET)                                         0.6543
```

Figure 15 : Setup Timing Paths



```
Endpoint: pc_current_reg_10_
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Point                                      Incr       Path
--------------------------------------------------------------
clock clk (rise edge)                    0.0000     0.0000
clock network delay (propagated)         0.1352     0.1352
pc_current_reg_9_/CK (DFFR_X1)           0.0000     0.1352 r
pc_current_reg_9_/Q (DFFR_X1)            0.0602 &   0.1954 r
U141/Z (BUF_X2)                          0.0119 &   0.2073 r
U139/Z (BUF_X1)                          0.0121 &   0.2194 r
U140/Z (BUF_X1)                          0.0123 &   0.2317 r
U138/Z (BUF_X1)                          0.0135 &   0.2452 r
U120/Z (BUF_X2)                          0.0114 &   0.2566 r
U119/Z (BUF_X1)                          0.0121 &   0.2687 r
U118/Z (BUF_X1)                          0.0125 &   0.2812 r
U110/Z (BUF_X1)                          0.0125 &   0.2937 r
U152/Z (BUF_X1)                          0.0334 &   0.3271 r
U435/Z (BUF_X4)                          0.0145 &   0.3416 r
U273/ZN (AND2_X2)                        0.0197 &   0.3613 r
U263/Z (XOR2_X1)                         0.0161 H   0.3774 f
U451/Z (BUF_X4)                          0.0392 H   0.4167 f
U284/ZN (AOI22_X1)                       0.0120 &   0.4287 r
U282/ZN (NAND2_X1)                       0.0191 &   0.4478 f
U397/Z (BUF_X8)                          0.0175 &   0.4653 f
U417/Z (BUF_X8)                          0.0129 &   0.4782 f
U431/Z (BUF_X8)                          0.0121 &   0.4903 f
pc_current_reg_10_/D (DFFR_X1)           0.0000 &   0.4903 f
data arrival time                                   0.4903

clock clk (rise edge)                    0.0000     0.0000
clock network delay (propagated)         0.1352     0.1352
clock uncertainty                        0.3500     0.4852
pc_current_reg_10_/CK (DFFR_X1)                     0.4852 r
library hold time                        0.0043     0.4895
data required time                                  0.4895
--------------------------------------------------------------
data required time                                  0.4895
data arrival time                                  -0.4903
--------------------------------------------------------------
slack (MET)                                         0.0008
```

Figure 16 : Hold Timing Paths

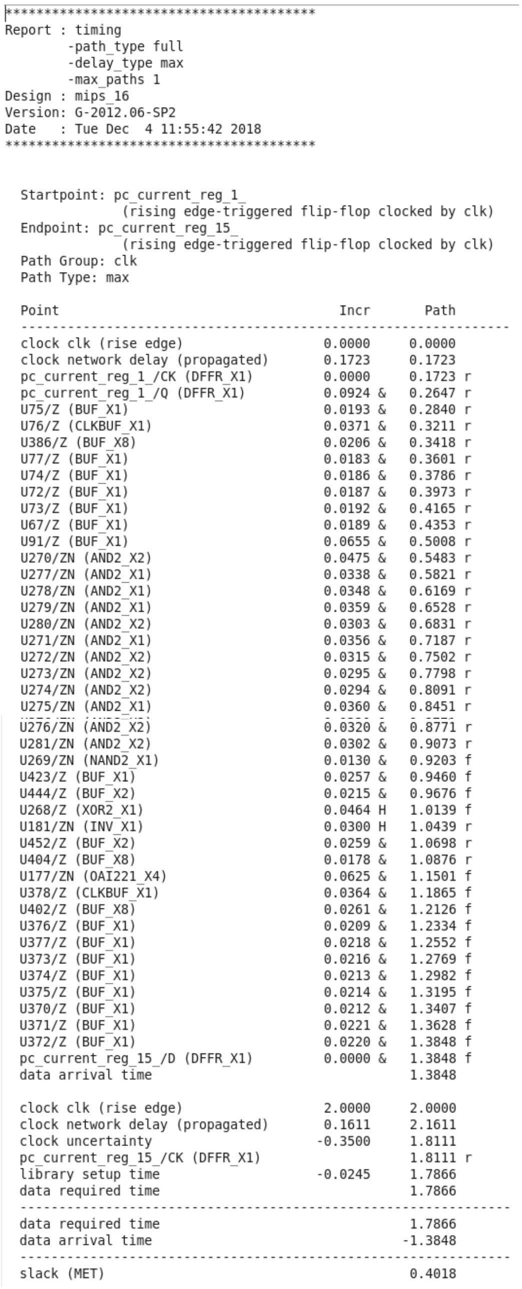
2. **Slow, Slow corner** → Initially, in this corner there are **no setup violations** exist but there are hold violations (**2 paths only are hold violated**). Therefore, we solve these hold violations automatically by **resizing the cells** and **inserting buffers (BUF_X2, BUF_X4)**

- Notice that in the ECO flow it appears setup violation due to large number of buffers inserted to solve hold violations in the fast corner

- **Finally, we meet our timing constraints without any violations**

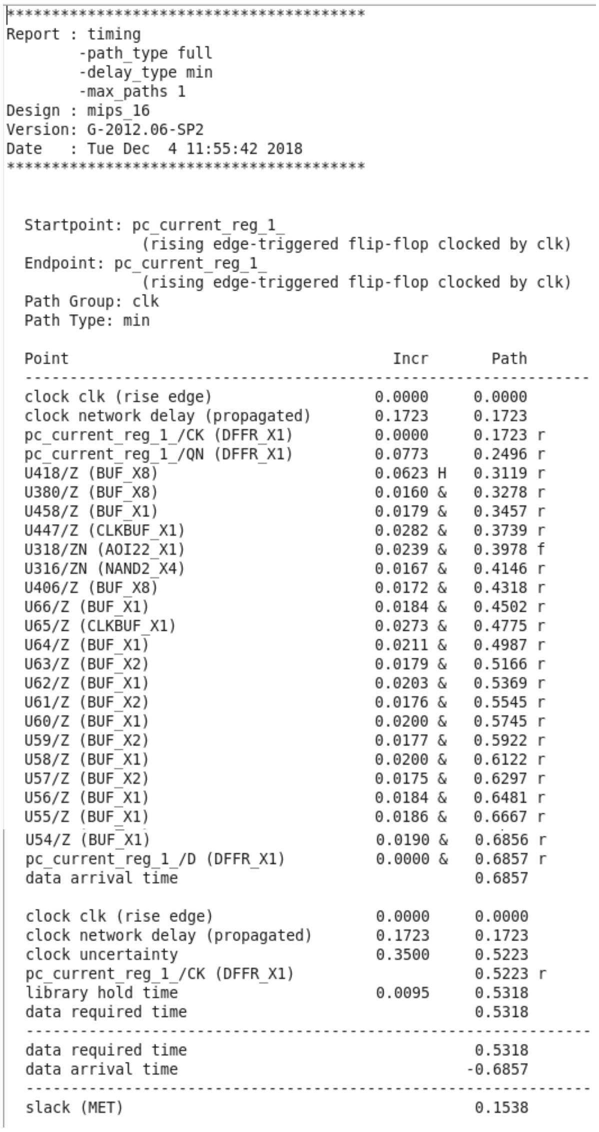
✓ **Worst setup Slack = 0.4018 ns**

✓ **Worst Hold Slack = 0.1538 ns**



```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
Design : mips_16
Version: G-2012.06-SP2
Date   : Tue Dec  4 11:55:42 2018
****************************************


  Startpoint: pc_current_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_current_reg_15_
              (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  ---------------------------------------------------------------
  clock clk (rise edge)                    0.0000     0.0000
  clock network delay (propagated)         0.1723     0.1723
  pc_current_reg_1_/CK (DFFR_X1)           0.0000     0.1723 r
  pc_current_reg_1_/Q (DFFR_X1)            0.0924 &   0.2647 r
  U75/Z (BUF_X1)                           0.0193 &   0.2840 r
  U76/Z (CLKBUF_X1)                        0.0371 &   0.3211 r
  U386/Z (BUF_X8)                          0.0206 &   0.3418 r
  U77/Z (BUF_X1)                           0.0183 &   0.3601 r
  U74/Z (BUF_X1)                           0.0186 &   0.3786 r
  U72/Z (BUF_X1)                           0.0187 &   0.3973 r
  U73/Z (BUF_X1)                           0.0192 &   0.4165 r
  U67/Z (BUF_X1)                           0.0189 &   0.4353 r
  U91/Z (BUF_X1)                           0.0655 &   0.5008 r
  U270/ZN (AND2_X2)                        0.0475 &   0.5483 r
  U277/ZN (AND2_X1)                        0.0338 &   0.5821 r
  U278/ZN (AND2_X1)                        0.0348 &   0.6169 r
  U279/ZN (AND2_X1)                        0.0359 &   0.6528 r
  U280/ZN (AND2_X2)                        0.0303 &   0.6831 r
  U271/ZN (AND2_X1)                        0.0356 &   0.7187 r
  U272/ZN (AND2_X2)                        0.0315 &   0.7502 r
  U273/ZN (AND2_X2)                        0.0295 &   0.7798 r
  U274/ZN (AND2_X2)                        0.0294 &   0.8091 r
  U275/ZN (AND2_X1)                        0.0360 &   0.8451 r
  U276/ZN (AND2_X2)                        0.0320 &   0.8771 r
  U281/ZN (AND2_X2)                        0.0302 &   0.9073 r
  U269/ZN (NAND2_X1)                       0.0130 &   0.9203 f
  U423/Z (BUF_X1)                          0.0257 &   0.9460 f
  U444/Z (BUF_X2)                          0.0215 &   0.9676 f
  U268/Z (XOR2_X1)                         0.0464 H   1.0139 f
  U181/ZN (INV_X1)                         0.0300 H   1.0439 r
  U452/Z (BUF_X2)                          0.0259 &   1.0698 r
  U404/Z (BUF_X8)                          0.0178 &   1.0876 r
  U177/ZN (OAI221_X4)                      0.0625 &   1.1501 f
  U378/Z (CLKBUF_X1)                       0.0364 &   1.1865 f
  U402/Z (BUF_X8)                          0.0261 &   1.2126 f
  U376/Z (BUF_X1)                          0.0209 &   1.2334 f
  U377/Z (BUF_X1)                          0.0218 &   1.2552 f
  U373/Z (BUF_X1)                          0.0216 &   1.2769 f
  U374/Z (BUF_X1)                          0.0213 &   1.2982 f
  U375/Z (BUF_X1)                          0.0214 &   1.3195 f
  U370/Z (BUF_X1)                          0.0212 &   1.3407 f
  U371/Z (BUF_X1)                          0.0221 &   1.3628 f
  U372/Z (BUF_X1)                          0.0220 &   1.3848 f
  pc_current_reg_15_/D (DFFR_X1)           0.0000 &   1.3848 f
  data arrival time                                   1.3848

  clock clk (rise edge)                    2.0000     2.0000
  clock network delay (propagated)         0.1611     2.1611
  clock uncertainty                       -0.3500     1.8111
  pc_current_reg_15_/CK (DFFR_X1)                     1.8111 r
  library setup time                      -0.0245     1.7866
  data required time                                  1.7866
  ---------------------------------------------------------------
  data required time                                  1.7866
  data arrival time                                  -1.3848
  ---------------------------------------------------------------
  slack (MET)                                         0.4018
```

Figure 18 : Setup Timing Paths



```
****************************************
Report : timing
        -path_type full
        -delay_type min
        -max_paths 1
Design : mips_16
Version: G-2012.06-SP2
Date   : Tue Dec  4 11:55:42 2018
****************************************


  Startpoint: pc_current_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: pc_current_reg_1_
              (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                    Incr       Path
  ---------------------------------------------------------------
  clock clk (rise edge)                    0.0000     0.0000
  clock network delay (propagated)         0.1723     0.1723
  pc_current_reg_1_/CK (DFFR_X1)           0.0000     0.1723 r
  pc_current_reg_1_/QN (DFFR_X1)           0.0773     0.2496 r
  U418/Z (BUF_X8)                          0.0623 H   0.3119 r
  U380/Z (BUF_X8)                          0.0160 &   0.3278 r
  U458/Z (BUF_X1)                          0.0179 &   0.3457 r
  U447/Z (CLKBUF_X1)                       0.0282 &   0.3739 r
  U318/ZN (AOI22_X1)                       0.0239 &   0.3978 f
  U316/ZN (NAND2_X4)                       0.0167 &   0.4146 r
  U406/Z (BUF_X8)                          0.0172 &   0.4318 r
  U66/Z (BUF_X1)                           0.0184 &   0.4502 r
  U65/Z (CLKBUF_X1)                        0.0273 &   0.4775 r
  U64/Z (BUF_X1)                           0.0211 &   0.4987 r
  U63/Z (BUF_X2)                           0.0179 &   0.5166 r
  U62/Z (BUF_X1)                           0.0203 &   0.5369 r
  U61/Z (BUF_X2)                           0.0176 &   0.5545 r
  U60/Z (BUF_X1)                           0.0200 &   0.5745 r
  U59/Z (BUF_X2)                           0.0177 &   0.5922 r
  U58/Z (BUF_X1)                           0.0200 &   0.6122 r
  U57/Z (BUF_X2)                           0.0175 &   0.6297 r
  U56/Z (BUF_X1)                           0.0184 &   0.6481 r
  U55/Z (BUF_X1)                           0.0186 &   0.6667 r
  U54/Z (BUF_X1)                           0.0190 &   0.6856 r
  pc_current_reg_1_/D (DFFR_X1)            0.0000 &   0.6857 r
  data arrival time                                   0.6857

  clock clk (rise edge)                    0.0000     0.0000
  clock network delay (propagated)         0.1723     0.1723
  clock uncertainty                        0.3500     0.5223
  pc_current_reg_1_/CK (DFFR_X1)                      0.5223 r
  library hold time                        0.0095     0.5318
  data required time                                  0.5318
  ---------------------------------------------------------------
  data required time                                  0.5318
  data arrival time                                  -0.6857
  ---------------------------------------------------------------
  slack (MET)                                         0.1538
```

Figure 17 : Hold Timing Paths

Summary Table

Trial no.	Changes done	Frequency (Clock Period)	Core Utilization	Timing signoff results		
1	No changes	250 MHz (4 ns)	0.25		ff	ss
				Setup slack	2.2284 ns	2.1405 ns
				Hold slack	0.0022 ns	0.1548 ns
2	Edit the power mesh	500 MHz (2 ns)	0.4		ff	ss
				Setup slack	0.6543 ns	0.4018 ns
				Hold slack	0.0008 ns	0.1538 ns

- The table indicates that the design can run at a maximum frequency of 500 MHz (2 ns). Although the slow corner shows a worst-case setup slack of 0.4018 ns (meaning a frequency higher than 2 ns is technically achievable).

- The core utilization can't exceed 0.4, as doing so would create severe congestion and cause routing engine to fail.