



Ain Shams University  
Faculty of Engineering - CHEP  
CESS Program

Fall 2019



# **Electronic Design Automation (CSE215)**

## **PROJECT PART (3): PHYSICAL SYNTHESIS**

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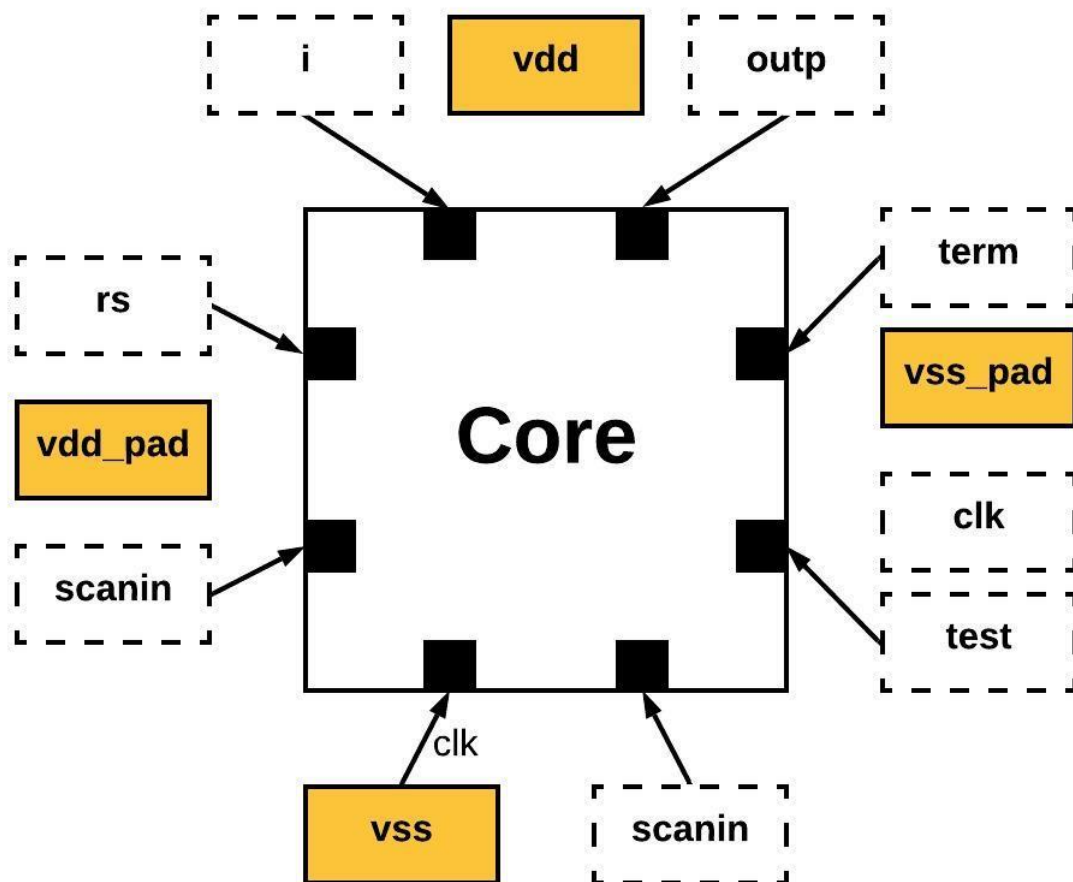
Program: CESS

## **INTRODUCTION:**

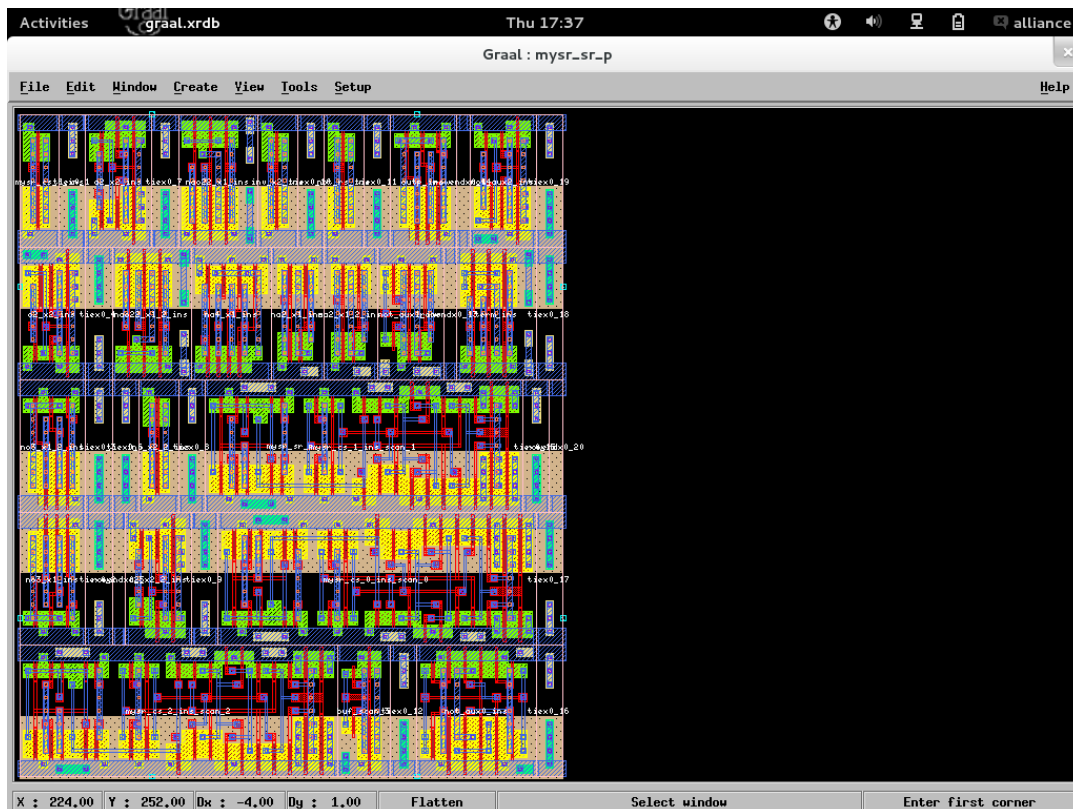
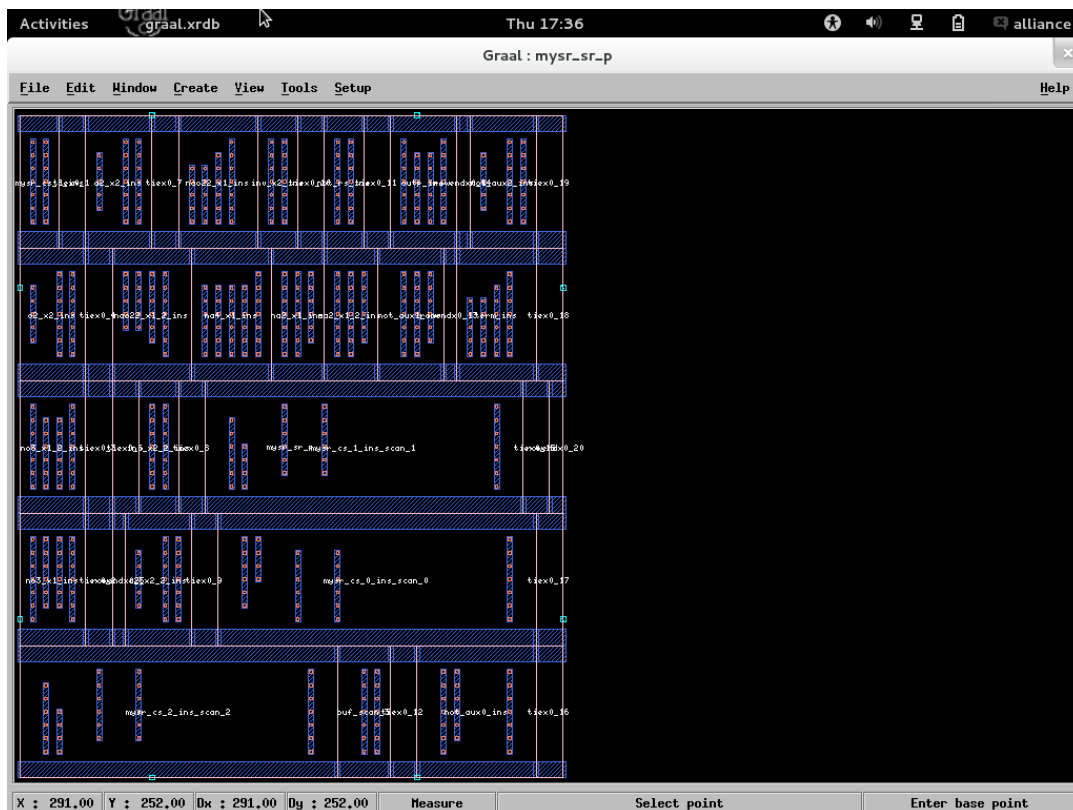
In this part of project, we perform the physical synthesis on the RTL design of project part (1) using some Alliance tools for placement and routing.

### 3. PART (3): PHYSICAL SYNTHESIS:

#### 3.1. Floorplanning:



## 3.2. Placement (ocp):



### 3.3. Routing:



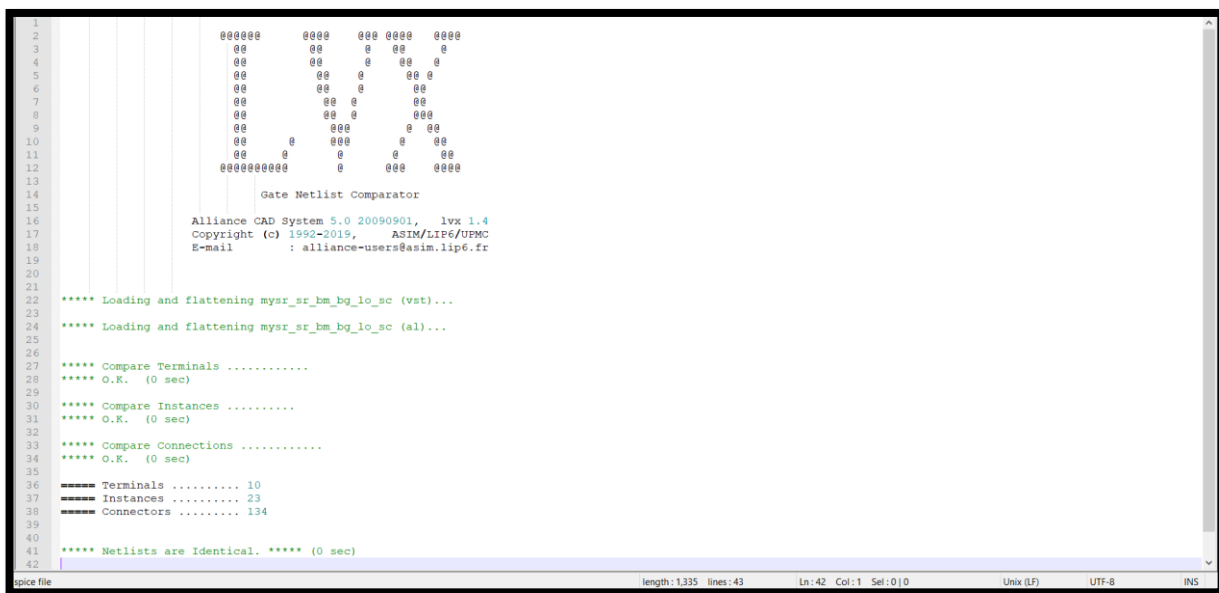
## 3.4. Post-Layout Verification:

### 3.4.1. Layout-vs-Schematic (cougar):

Netlist comparison is done on two steps; first the netlist is extracted using the **cougar** tool. The original netlist is in **vst** format. We'll have the extracted netlist in **al** format, in order not to overwrite files.

This is followed by netlist comparison using (lvx).

Below is a screenshot of the lvx.out file that confirms that the two Netlists are identical.



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      Gate Netlist Comparator

      Alliance CAD System 5.0 20090901, lvx 1.4
      Copyright (c) 1992-2019, ASIM/LIP6/UPMC
      E-mail : alliance-users@asim.lip6.fr

      ***** Loading and flattening mysr_sr_bm_bg_lo_sc (vst)...
      ***** Loading and flattening mysr_sr_bm_bg_lo_sc (al)...

      ***** Compare Terminals .....
      ***** O.K. (0 sec)

      ***** Compare Instances .....
      ***** O.K. (0 sec)

      ***** Compare Connections .....
      ***** O.K. (0 sec)

      ===== Terminals ..... 10
      ===== Instances ..... 23
      ===== Connectors ..... 134

      ***** Netlists are Identical. ***** (0 sec)

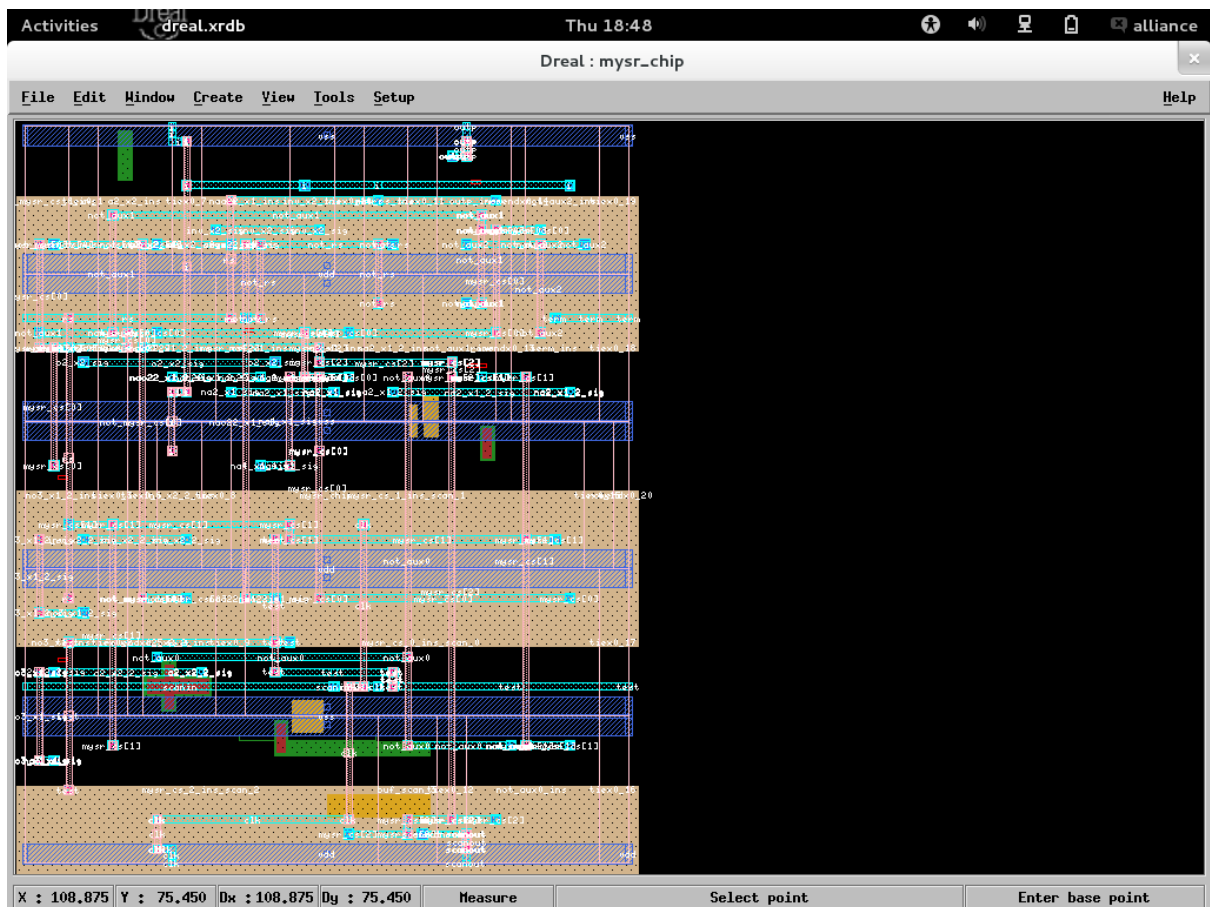
spice file length:1335 lines:43 Ln:42 Col:1 Sel:0|0 Unix (LF) UTF-8 INS
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```

## 2.5. Symbolic-to-Real Conversion (s2r):





## **APPENDIX:**

### **Floorplanning (pin\_order.ioc) file:**

```
LEFT( #IOs from bottom to top
      (IOPIN scanin.0);
      (IOPIN rs.0);      )
TOP( #IOs from left to right
     (IOPIN i.0);
     (IOPIN outp.0);      )
RIGHT( #IOs from bottom to top
       (IOPIN test.0);
       (IOPIN term.0);    )
BOTTOM( #IOs from left to right
        (IOPIN clk.0);
        (IOPIN scanout.0); )
```

## Makefile:

```
#----- mysr -----#
```

```
# s for syf
```

```
# bm for boom
```

```
# bg for boog
```

```
# lo for loon
```

```
# fb for flatbeh
```

```
# sc for scan
```

```
# p for floor planning
```

```
# nr for nero
```

```
# cg for cougar
```

```
# drc for druc_core
```

```
syf_all:mysr_sa.vbe \
```

```
    mysr_sj.vbe \
```

```
    mysr_sm.vbe \
```

```
    mysr_so.vbe \
```

```
    mysr_sr.vbe
```

```
    @echo "--->>> all syf done successfully"
```

```
boom_all:mysr_sa_bm.vbe \
```

```
    mysr_sj_bm.vbe \
```

```
    mysr_sm_bm.vbe \
```

```
    mysr_so_bm.vbe \
```

```
    mysr_sr_bm.vbe
```

```
@echo "--->>> all boom done successfully"
```

```
boog_all:mysr_sa_bm_bg.vst \
```

```
mysr_sj_bm_bg.vst \
```

```
mysr_sm_bm_bg.vst \
```

```
mysr_so_bm_bg.vst \
```

```
mysr_sr_bm_bg.vst
```

```
@echo "--->>> all boog done successfully"
```

```
loon_all:mysr_sa_bm_bg_lo.vst \
```

```
mysr_sj_bm_bg_lo.vst \
```

```
mysr_sm_bm_bg_lo.vst \
```

```
mysr_so_bm_bg_lo.vst \
```

```
mysr_sr_bm_bg_lo.vst
```

```
@echo "--->>> all loon done successfully"
```

```
flatbeh:mysr_sr_bm_bg_lo_fb.vbe
```

```
@echo "---->>> flatbeh and proof done successfully"
```

```
scan:mysr_sr_bm_bg_lo_sc.vst
```

```
@echo "--->>> scan done successfully"
```

```
ocp:mysr_sr_p.ap
```

```
@echo "--->>> placement done successfully"
```

```
nero:mysr_sr_bm_bg_lo_sc.ap
```

```
@echo "--->>> routing done successfully"
```

```
cougar_lvx:mysr_sr_bm_bg_lo_sc.al
```

```
    @echo "--->>> netlist extraction and comparison done  
successfully"
```

```
drc:druc_core
```

```
    @echo "--->>> design rule checker done successfully"
```

```
s2r:mysr_chip.cif
```

```
    @echo    "--->>>    symbolic    to    real    layout    done  
successfully"
```

```
#----- mysr rules -----#
```

```
#----- rename -----#
```

```
vhd_to_fsm:
```

```
    rename .vhd .fsm *.vhd
```

```
    @echo "--->>> renamed"
```

```
#----- syf -----#
```

```
mysr_sa.vbe:mysr.fsm
```

```
    @echo "--->>> encoding -> a"
```

```
    syf -CEV -a mysr mysr_sa > mysr_sa.out
```

```
mysr_sj.vbe:mysr.fsm
```

```
    @echo "--->>> encoding -> j"
```

```
syf -CEV -j mysr mysr_sj > mysr_sj.out
```

```
mysr_sm.vbe:mysr.fsm
```

```
@echo "--->>> encoding -> m"
```

```
syf -CEV -m mysr mysr_sm > mysr_sm.out
```

```
mysr_so.vbe:mysr.fsm
```

```
@echo "--->>> encoding -> o"
```

```
syf -CEV -o mysr mysr_so > mysr_so.out
```

```
mysr_sr.vbe:mysr.fsm
```

```
@echo "--->>> encoding -> r"
```

```
syf -CEV -r mysr mysr_sr > mysr_sr.out
```

```
#----- boom -----#
```

```
%_bm.vbe:%.vbe
```

```
@echo "--->>> boolean minimization -> $_bm"
```

```
boom -V -d 50 $* $_bm > $_bm.out
```

```
#----- boog -----#
```

```
%_bg.vst:%.vbe paramfile.lax
```

```
@echo "--->>> logical synthesis -> $_bg"
```

```
boog -x 1 -l paramfile $* $_bg > $_bg.out
```

```
#----- loon -----#
```

```

%_lo.vst:%.vst paramfile.lax
    @echo "--->>> netlist optimization -> $_lo"
    loon -x 1 -l paramfile $* $_lo > $_lo.out

#----- flatbeh -----#

%_bm_bg_lo_fb.vbe:%_bm_bg_lo.vst %.vbe
    @echo "--->>> formal checking -> $"
    flatbeh      $_bm_bg_lo      $_bm_bg_lo_fb      >
$_bm_bg_lo_fb.out
    proof -d $* $_bm_bg_lo_fb > $_proof.out

#----- ac_scapin_registers -----#

ac_scapin_registers:
    cat mysr_sr_bm_bg_lo.vst | grep sff

#----- scan -----#

%_sc.vst:%.vst scan.path
    @echo "--->>> scan path insertion -> $"
    scapin -VRB $* scan $_sc > $_sc.out

#----- ocp -----#

%_p.ap:pin_order.ioc $_bm_bg_lo_sc.vst

```

```
@echo "--->>> placement $_p.ap"
MBK_IN_LO=vst; export MBK_IN_LO; \
MBK_OUT_PH=ap; export MBK_OUT_PH; \
ocp -v -ring -ioc pin_order $_bm_bg_lo_sc $_p >
$_p.out
```

placement\_graal:

```
RDS_TECHO_NAME=./techno/techno-symb.rds; \
export RDS_TECHNO_NAME; \
graal -l mysr_sr_p
@echo "--->>> placement_graal done successfully"
```

#----- nero -----#

```
$_bm_bg_lo_sc.ap:$_p.ap $_bm_bg_lo_sc.vst
@echo "--->>> routing $_bm_bg_lo_sc.ap"
MBK_IN_LO=vst; export MBK_IN_LO; \
MBK_IN_PH=ap; export MBK_IN_PH; \
MBK_OUT_PH=ap; export MBK_OUT_PH; \
nero -V -p $_p $_bm_bg_lo_sc $_bm_bg_lo_sc >
$_bm_bg_lo_sc_nr.out
```

routing\_graal:

```
RDS_TECHO_NAME=./techno/techno-symb.rds; \
export RDS_TECHNO_NAME; \
graal -l mysr_sr_bm_bg_lo_sc
@echo "--->>> routing_graal done successfully"
```

```
#----- cougar_lvx -----#
```

```
%.a1:%.ap
```

```
MBK_IN_PH=ap; export MBK_IN_PH; \  
MBK_OUT_LO=a1; export MBK_OUT_LO; \  
RDS_TECHNO_NAME=./techno/techno-035.rds; \  
export RDS_TECHNO_NAME; \  
cougar -v $* > $_cg.out  
lvx vst a1 $* $* -f > $_lvx.out
```

```
#----- drc -----#
```

```
druc_core:mysr_sr_bm_bg_lo_sc.ap
```

```
MBK_IN_PH=ap; export MBK_IN_PH; \  
RDS_OUT=cif; export RDS_OUT; \  
RDS_TECHO_NAME=./techno/techno-symb.rds; \  
export RDS_TECHNO_NAME; \  
druc mysr_sr_bm_bg_lo_sc > mysr_sr_bm_bg_lo_sc_drc.out
```

```
#----- s2r -----#
```

```
mysr_chip.cif:mysr_sr_bm_bg_lo_sc.ap
```

```
MBK_IN_PH=ap; export MBK_IN_PH; \  
RDS_OUT=cif; export RDS_OUT; \  
RDS_TECHNO_NAME=./techno/techno-035.rds; \  
export RDS_TECHNO_NAME; \  

```



```
s2r -v -r mysr_sr_bm_bg_lo_sc mysr_chip >  
mysr_chip_s2r.out
```

```
chip_dreal:
```

```
RDS_IN=cif; export RDS_IN; \  
RDS_TECHNO_NAME=./techno/techno-035.rds; \  
export RDS_TECHNO_NAME; \  
dreal -l mysr_chip  
@echo "--->>> chip_dreal done successfully"
```

```
#----- clear -----#
```

```
clean :
```

```
rm -f *.vbe *.enc *~  
@echo "Erase all the files generated by the makefile"
```