Electronic Design Automation
CSE 215

Course Project

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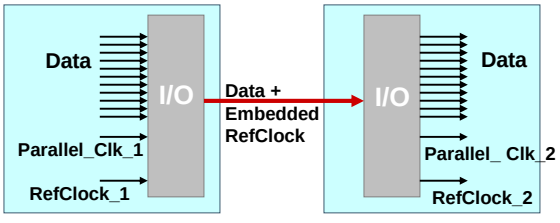
High Speed Serial Links



Serial Link (SerDes)

- Send data serially instead of parallel busses.
- Example: USB, SATA, …
- High-speed clock (RefClock) = Serial transmission rate
- Parallel data clock (Parallel_Clk) = RefClock/Data bus width
- Characteristics
  - Point-to-point differential signaling → Higher line speeds
  - No separate clock signal (embedded clks), clock is extracted at the receiver.
  - Can use multiple parallel lanes → Bandwidth scalability

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Needs a Communication Protocol

- Procedure to initialize the link and be sure that both sides are ready to receive data
- Line encoding algorithm
- Alignment, clock correction, idle sequences
- Packet composition
- Error correction algorithm

- Standard *versus* Custom protocols??

Project: 2-String Recognizer

- A finite state recognizer has one input (In) and two outputs (Out) and (Termination), in addition to the (Reset) and (Clock) inputs (+VDD and VSS).
- The output is asserted whenever the input sequence 010 (detection string) has been observed, ***as long as*** the sequence 100 (termination string) has never been seen.
- Once 100 appears, the (Termination) output is asserted and the output remains 0 till the (Reset) is asserted.
- Examples:

In	11011010010…
Out	00000001000000…
Term	00000000111111…

In	00101010010…
Out	00010101000000…
Term	00000000111111…

Project Implementation

- Project statement and deadline, see course web site.
- Guideline files throughout the lectures. Check the “Project Files” folder.

First Step – Project Part 1:

- Design the state diagram. Choose ***Mealy*** or ***Moore*** outputs. Must explicitly state your choice in the documentation.
- Implement the FSM in VHDL.
- Prepare a ModelSim testbench to validate your design with proper assertions to be used throughout the project.
  - The more the assertions, the more effective the testbench will be in testing different phases of the design.

- Best to do each part of the project after the lecture directly and be prepared for the next step.