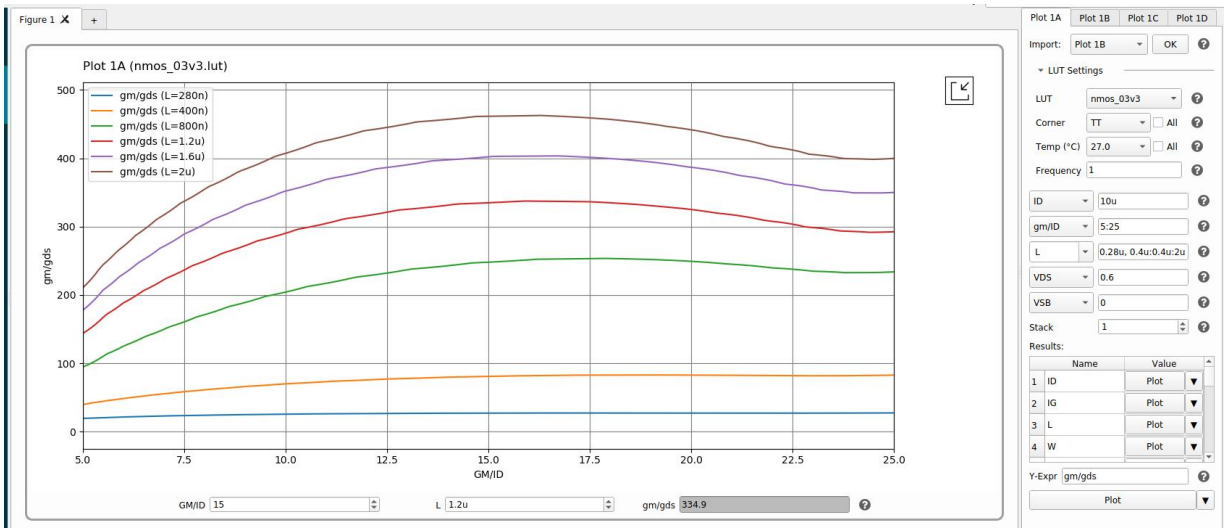
Lab 07

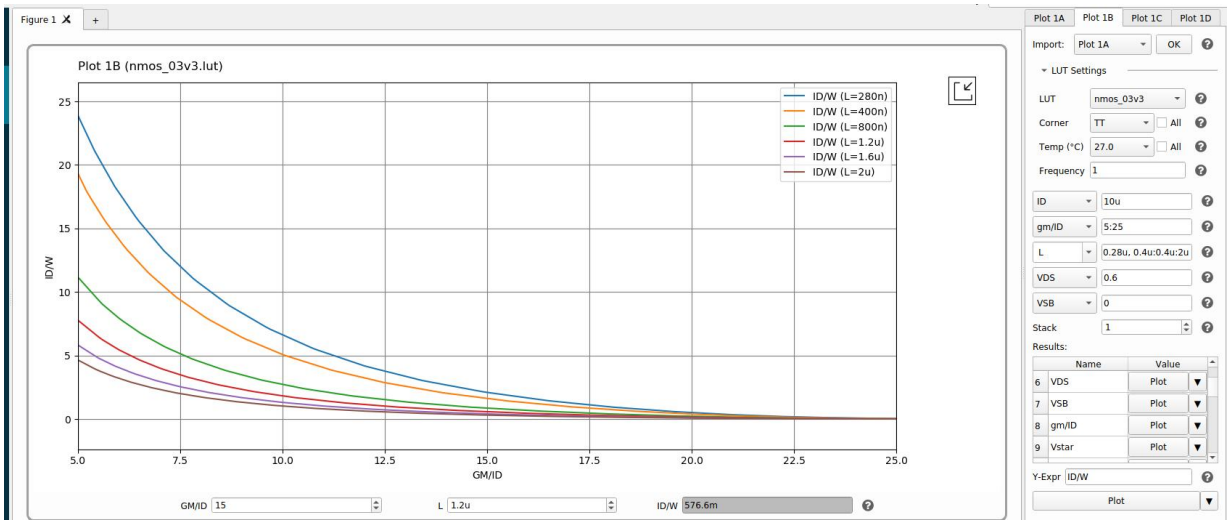
Part 1: gm/ID Design Charts:

Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS =VDD/3 and L = 0.28u, 0.4u:0.4u:2u:

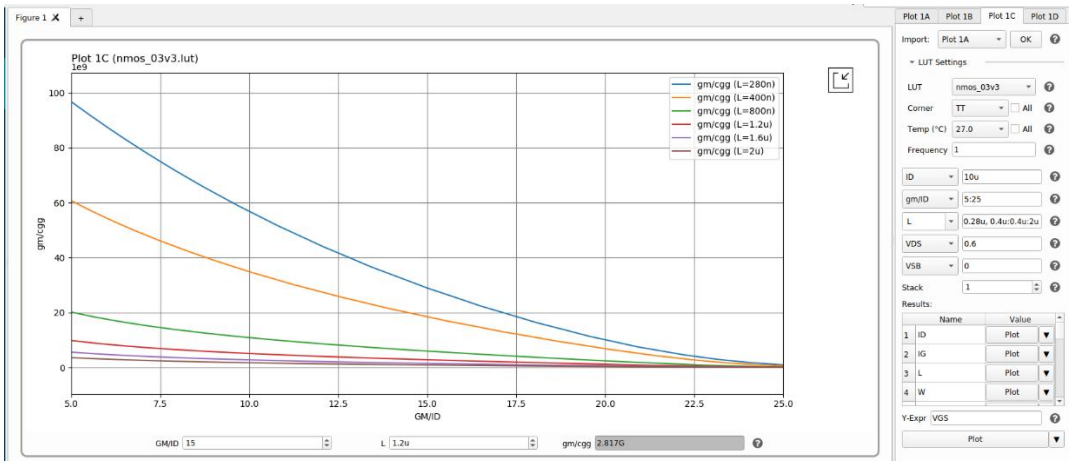
- NMOS:
  - gm/gds



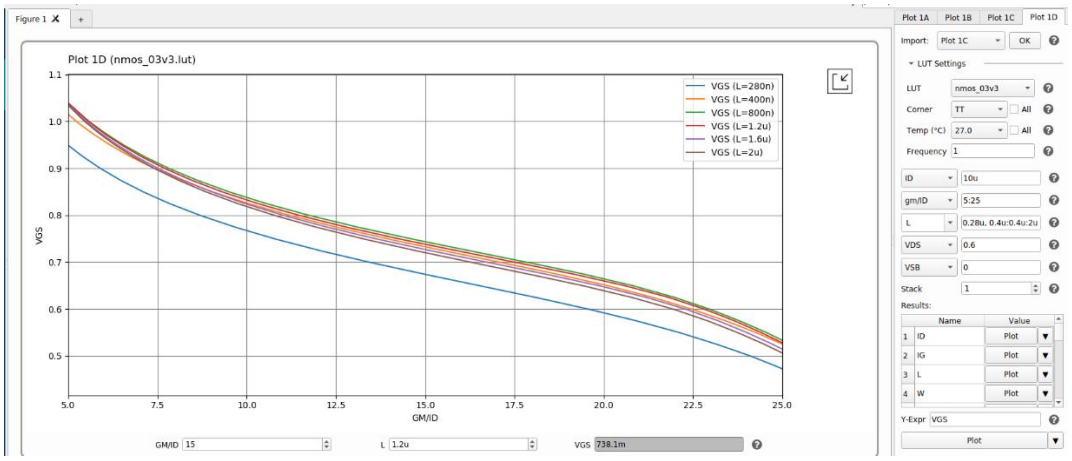
  - ID/W



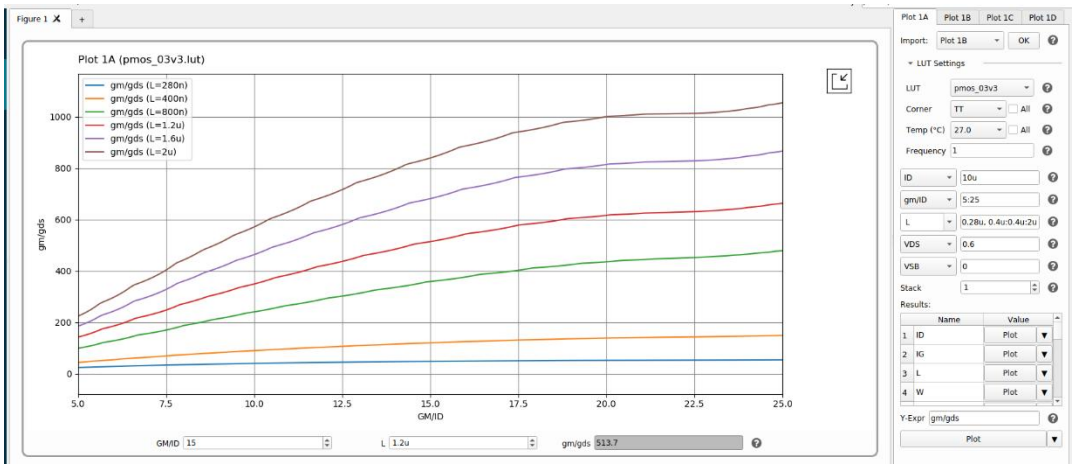
- gm/cgg



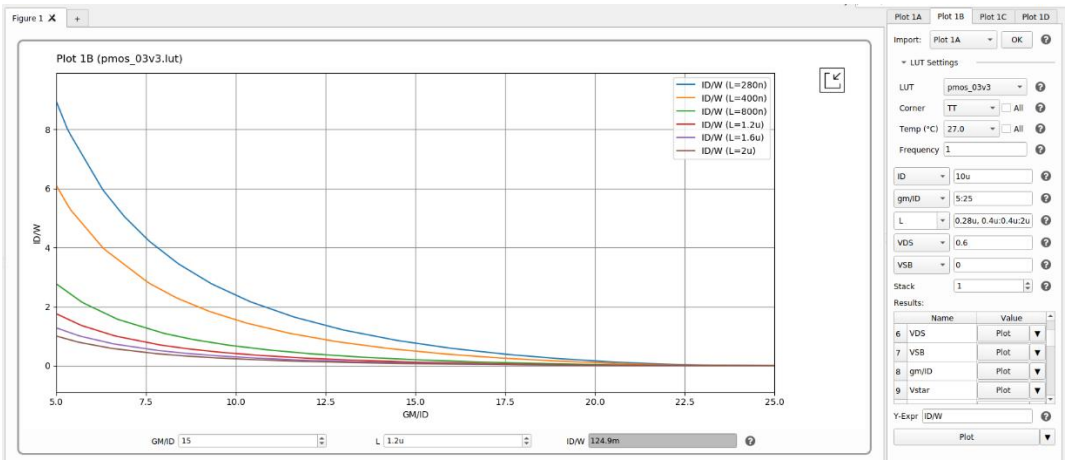
- VGS



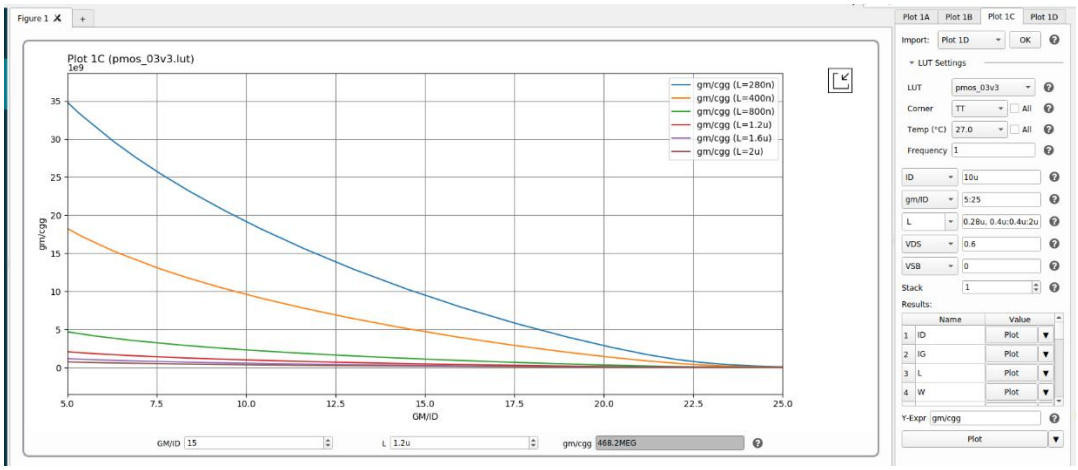
- PMOS:
  - gm/gds



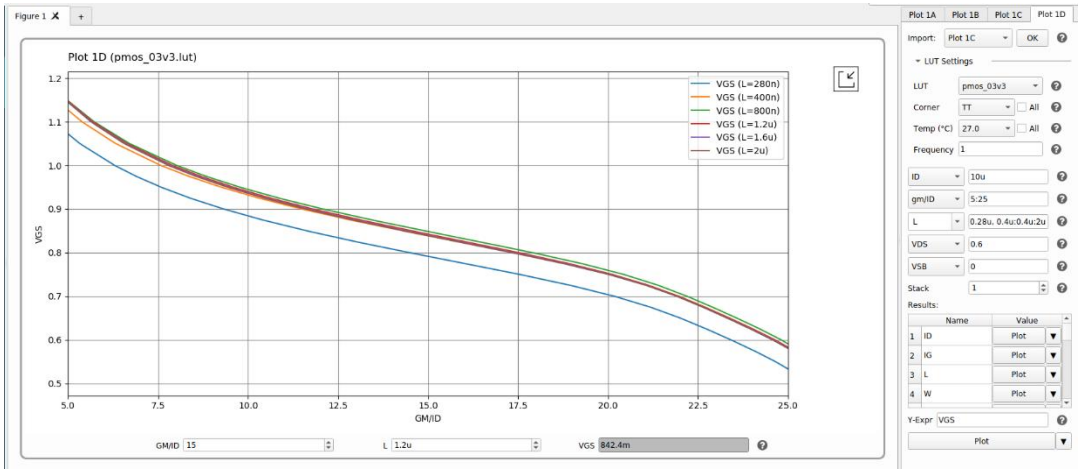
- ID/W



- gm/cgg



- VGS



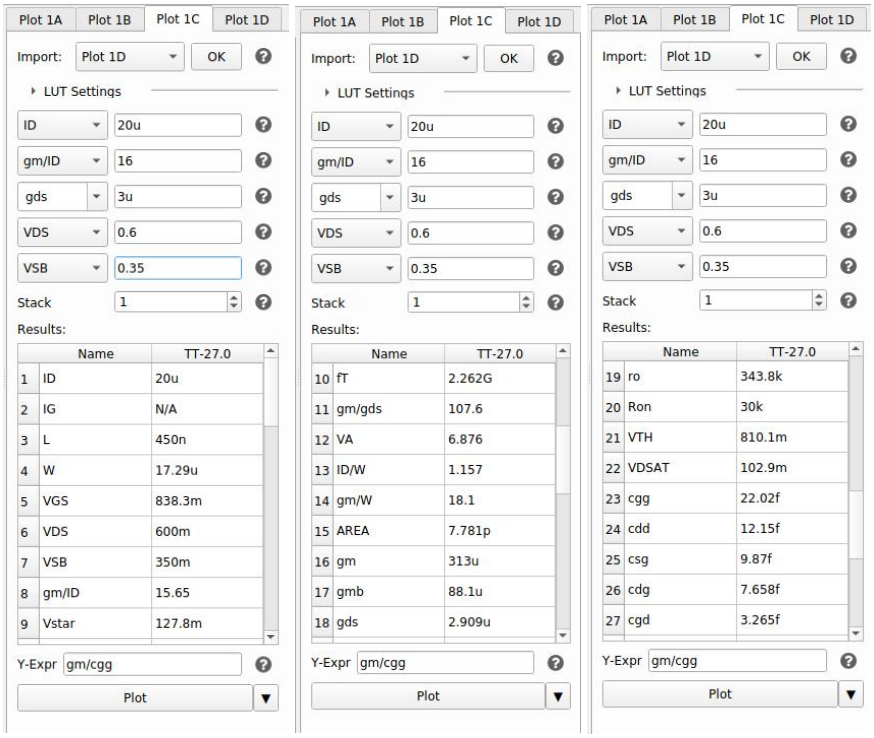
Part 2: OTA Design:

- **Specs:**

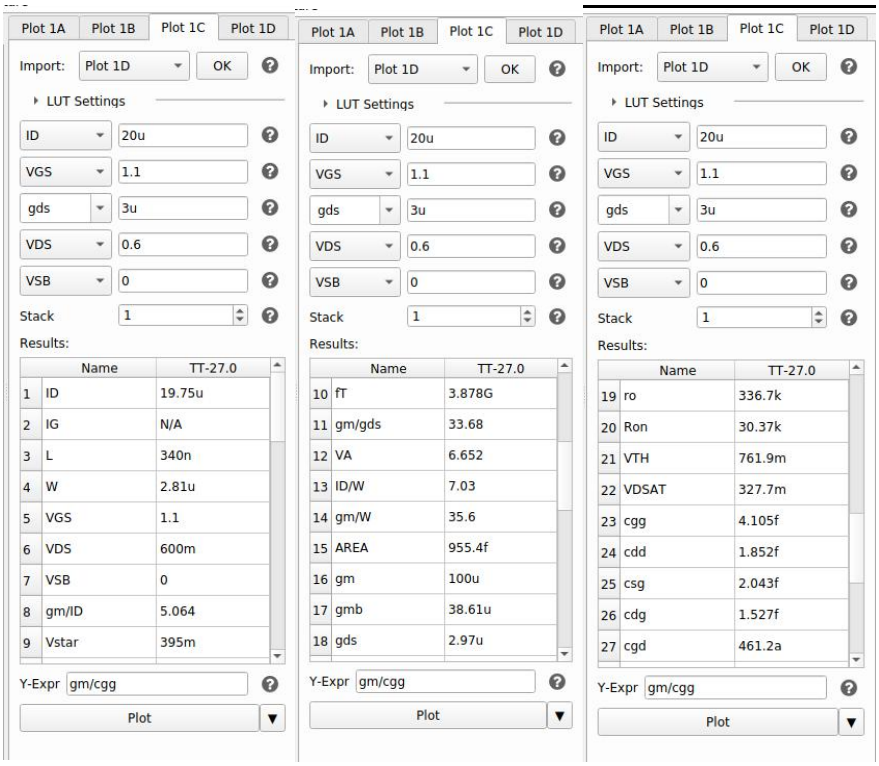
Parameter	value
VDD	$1.8V$
Load	$5pF$
Open loop dc voltage gain	$\geq 34\ dB$
CMMR at dc	$\geq 74\ dB$
Phase margin	$\geq 70°$
CM input range low	$\leq 1\ V$
CM input range high	$\geq 1.5\ V$
GBW	$\geq 10\ MHz$

- **Detailed design procedure and hand analysis:**

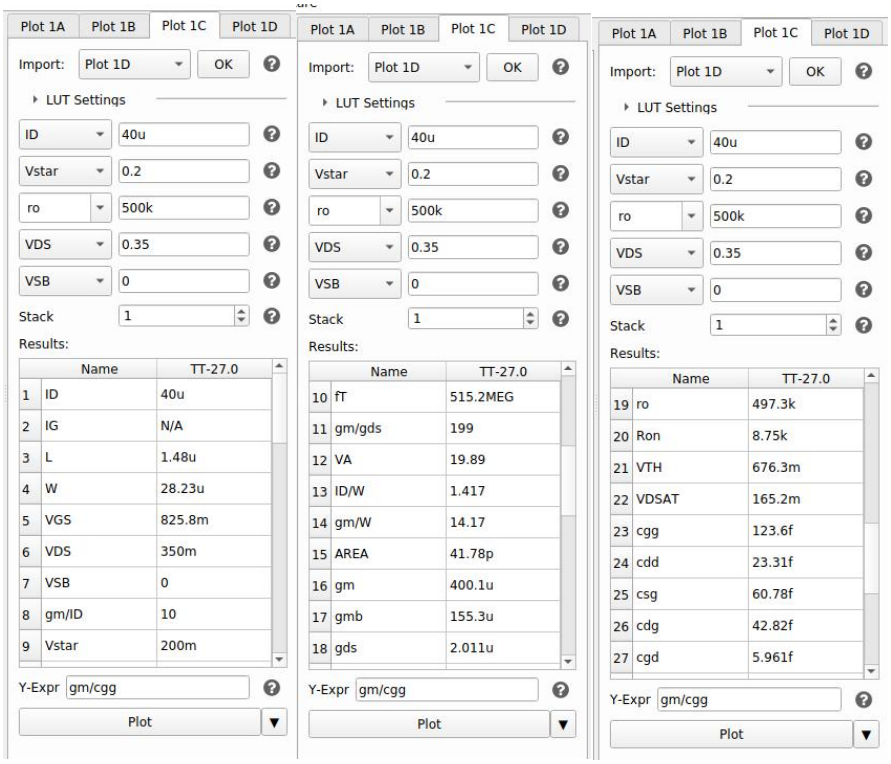
- We will choose a single stage 5T-OTA as the gain isn't very high and we can use a single stage to achieve it. The input pair will be NMOS as the CM input range is closer to VDD.
- First, we will design the input pair. We know that $GBW = \frac{gm12}{2\pi * CL} \geq 10MHz\ then\ gm12 \geq 314.16\mu S$. Taking margin, we will choose $gm = 320\mu S$.
- We will assume a reasonable gm/ID wit value 16 so the current in each branch will be 20 μA.
- We will assume that $ro12 = ro34$ then from the gain spec we want $\frac{gm}{2 * gds} \geq 50$ then $gds \leq 3.1416\mu S$, we will take a margin and choose $gds = 3\mu S$.
- There is a body effect in the input pair we will assume approximate value of 0.35V and put VDS=0.6V as given.
- From the SA values in the next page, we W=17.29 $\mu m\ and\ L = 450nm$.



- Now, we will design the active load transistors. We know that $ID = 20\mu A$ in each branch from the input pair design. We also assumed that $gds12 = gds34 = 3\mu S$.
- From CM input range high $VCM = Vth1{,}2 - |VGS3{,}4| + VDD \geq 1.5$
  We got VGS1,2≈ $0.84V$ and $VDsat1{,}2 \approx 0.1$ then VGS3,4≤ 1.11
  We got $W = 2.81\mu m$ and $L = 340nm$.



- Now, we will design the tail current mirror. We know that the current in the transistor is $40\mu A$.
- From the CM input range low: $VCM = VGS1{,}2 + VDsat5 \leq 1\ then\ VDsat5 \leq 0.16$. And we know that v^* is always higher than Vdsat then we may choose $v^* = 0.2V$. From CMRR spec we find that $ACM \leq -40dB$ then $\frac{1}{2*gm3{,}4*ro5} \leq 0.01.\ ro5 \geq 500K\Omega$.
- We put VDS=0.35V as we put the VSB for the input pair with the samevaluse and $VSB1{,}2 = VDS5$.
- We got $W = 28.23\mu m$ and $L = 1.48\mu m$.
- To get sizing for M6: L6=L5=1.48 μm and $\frac{W6}{W5} = \frac{10\mu A}{40\mu A}$ then $W6 = 7.0575\ \mu m$.

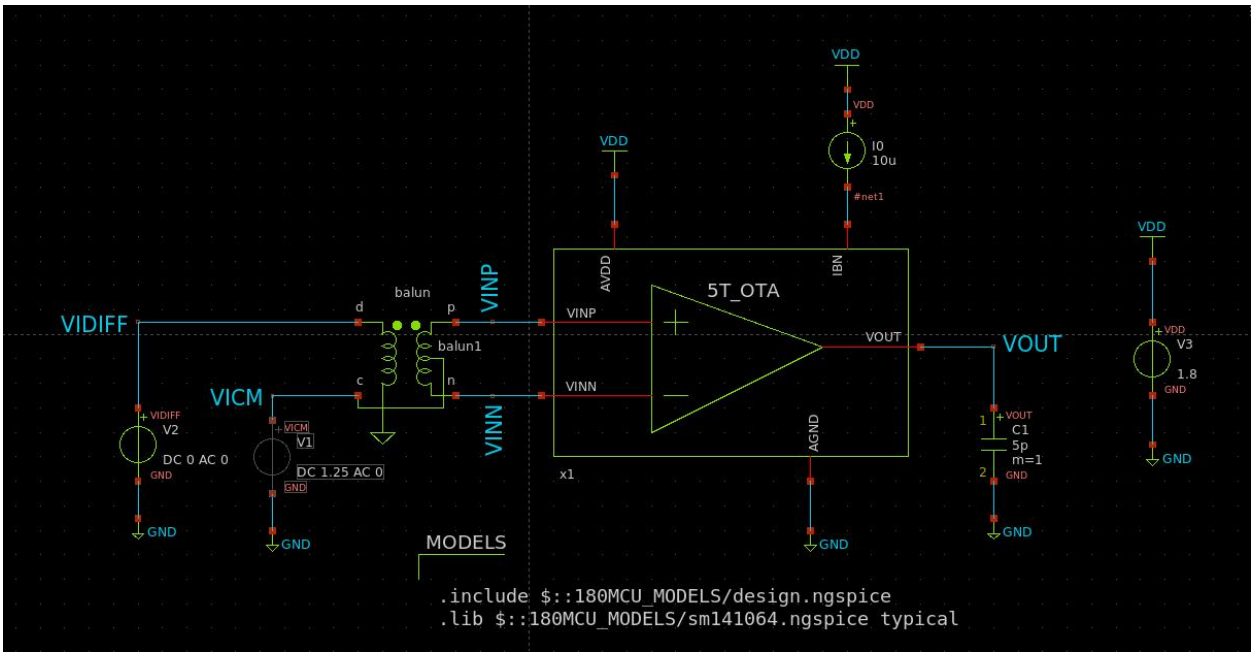


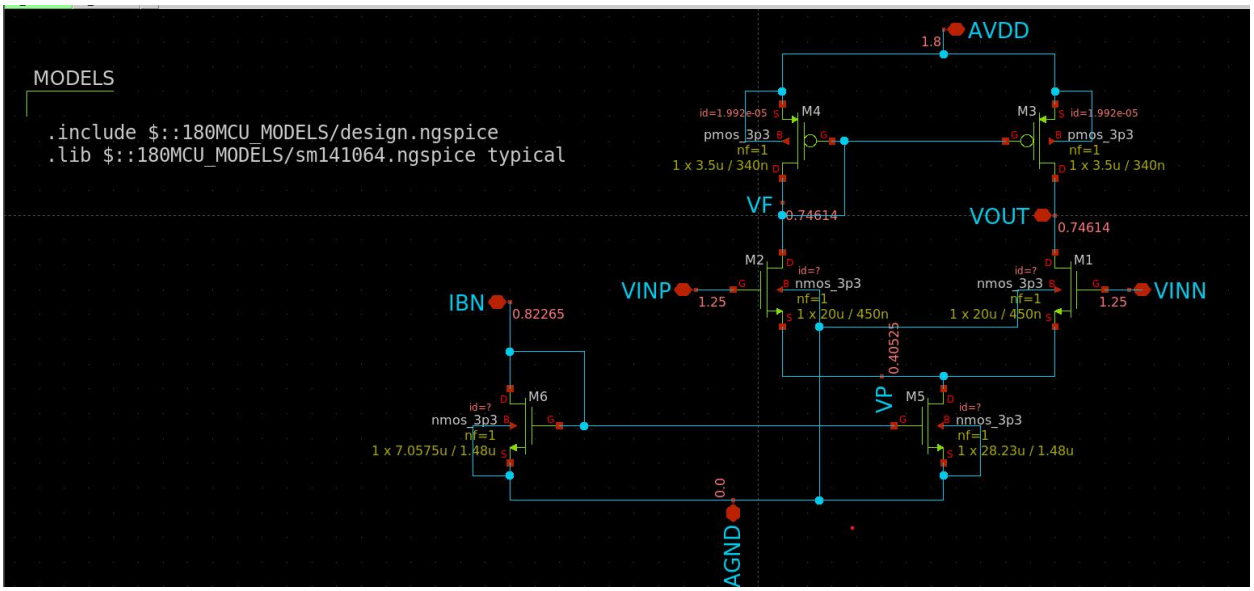
- **Transistors calculated parameters:**

NUM	W	L	gm	ID	gm/ID	VDsat	Vov	V^*
M1,2	$17.3\ \mu m$	$450nm$	$313\ \mu S$	$20\ \mu A$	15.65	$103mV$	$28.2mV$	$127.8mV$
M3,4	$2.8\mu m$	$340nm$	$100\ \mu S$	$20\ \mu A$	5	$327.7mV$	$338.1mV$	$400mV$
M5	$28.2\ \mu m$	$1.48\ \mu m$	$400\ \mu S$	$40\ \mu A$	10	$165.2mV$	$149.5mV$	$200mV$
M6	$7.05\ \mu m$	$1.48\ \mu m$	$100\ \mu S$	$10\ \mu A$	10	$165.2mV$	$149.5mV$	$200mV$

Part 3: Open-Loop OTA Simulation:

Schematic of the OTA with DC node voltages clearly annotated:





```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm6.m0           m.x1.xm4.m0           m.x1.xm3.m0
     model           nmos_3p3.10            pmos_3p3.8            pmos_3p3.8
        id                  1e-05           1.99096e-05           1.99096e-05
        gm           0.000101295           0.000102627           0.000102627
       gds            2.5173e-07            1.8722e-06            1.8722e-06
      gmbs           3.94132e-05           3.96305e-05           3.96305e-05
       vgs              0.822648              1.09261               1.09261
       vth              0.676836             0.757213              0.757213
       vds              0.822646               1.0926                1.0926
     vdsat              0.163568             0.326462              0.326462
       cgs          -2.27501e-14          -2.51545e-15          -2.51545e-15
       cgd          -4.94816e-18           9.29301e-18           9.29301e-18
       csb          -5.54631e-15          -6.02479e-16          -6.02479e-16
       cdb          -3.70319e-15          -4.02314e-16          -4.02314e-16

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm5.m0           m.x1.xm2.m0           m.x1.xm1.m0
     model           nmos_3p3.14           nmos_3p3.12           nmos_3p3.12
        id           3.98192e-05           1.99096e-05           1.99096e-05
        gm           0.000404564            0.00031354            0.00031354
       gds           1.59919e-06           4.21413e-06           4.21413e-06
      gmbs           0.000157466           8.61308e-05           8.61308e-05
       vgs              0.822648              0.852176              0.852176
       vth              0.677106              0.826178              0.826178
       vds              0.397819              0.309558              0.309558
     vdsat                0.1638              0.102298              0.102298
       cgs          -9.11125e-14           -9.5649e-15           -9.5649e-15
       cgd          -2.22179e-16          -4.03201e-18          -4.03201e-18
       csb          -2.22359e-14          -1.68521e-15          -1.68521e-15
       cdb          -1.49567e-14          -1.13408e-15          -1.13408e-15
```

```
 === Calculated Parameters ===
M1: gm/id = 15.7481 S/A, Vstar = 0.126999 V, ro = 237297 ohms
M2: gm/id = 15.7481 S/A, Vstar = 0.126999 V, ro = 237297 ohms
M3: gm/id = 5.15467 S/A, Vstar = 0.387998 V, ro = 534132 ohms
M4: gm/id = 5.15467 S/A, Vstar = 0.387998 V, ro = 534132 ohms
M5: gm/id = 10.16 S/A, Vstar = 0.19685 V, ro = 625316 ohms
M6: gm/id = 10.1295 S/A, Vstar = 0.197443 V, ro = 3.97251E+06 ohms
ngspice 1 ->
```

The change in ro1,2 and ro3,4 is because of the change in VDS

Note: I changed W1,2 and W3,4 slightly as some specs weren't achieved. We will discus this at its part and the updated OP will be in the updated section.

• Is the current (and gm) in the input pair exactly equal?

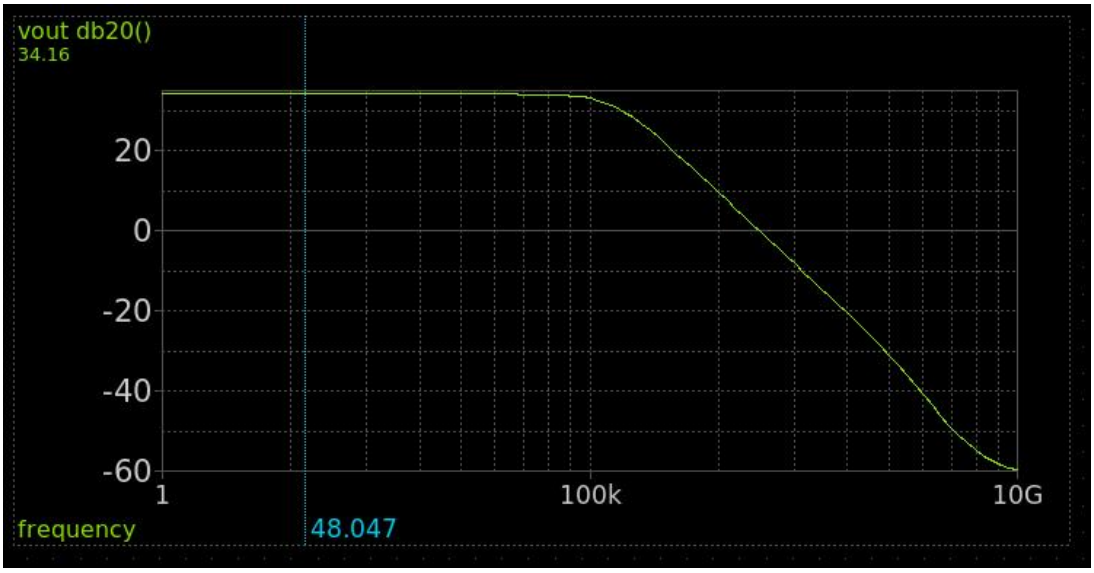
Yes, the current and gm of the input pair is equal as they have the same bias point and no mismatch.

• What is DC voltage at VOUT? Why?

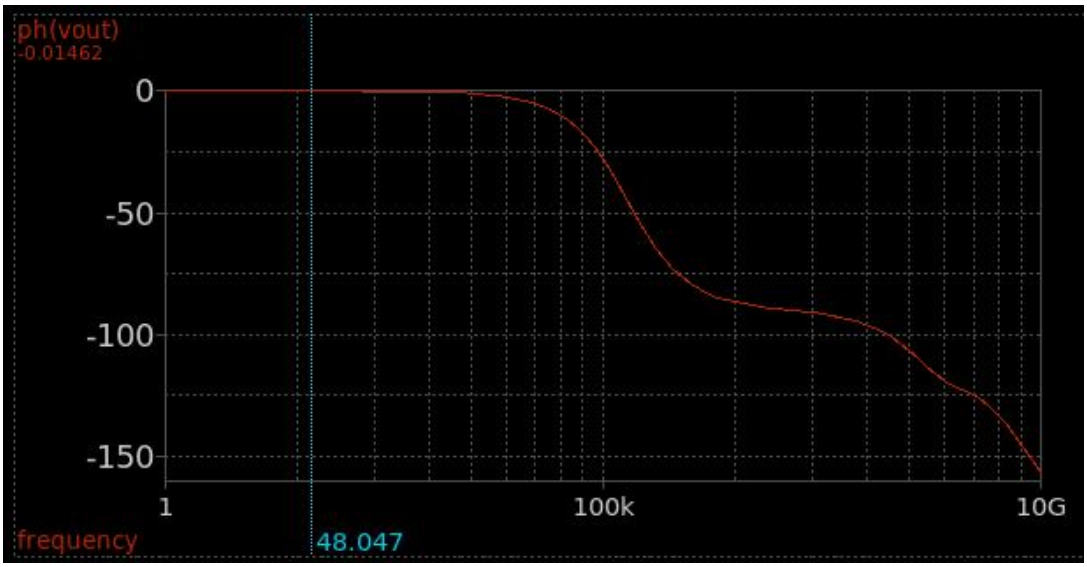
$Vout = 0.746V$ as it can be got from $vout = VF = VDD - |VGS3{,}4| = 0.746$ and Vout=VF as if we tried to assume Vout<VF then VDS3>VDS4 and M3,M4 have the same VGS which means more current in the right branch but VDS1<VDS2 which means more current in the left branch so it is wrong and if we assumed Vout>VF we will get the same result so Vout=VF.

2) Diff small signal ccs:

- Diff gain in dB:



- Diff gain phase:



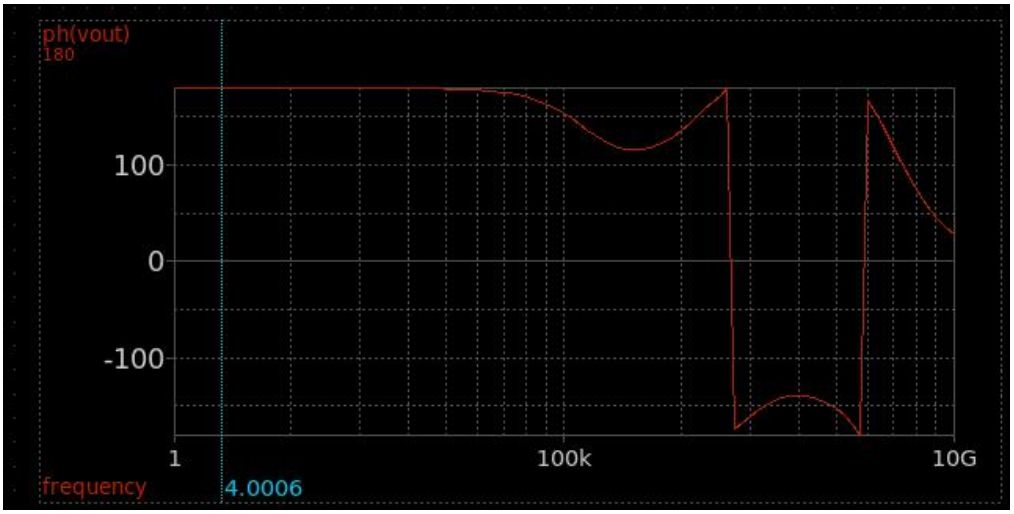
- Hand Analysis:
  $Ad = gm1{,}2 * (ro1{,}2 // ro3{,}4) = 51.5 = 34.24dB.$

	Hand Analysis	Simulation
Diff gain	34.24dB	$34.16dB$

3) CM small signal ccs:

- CM gain in dB:

- CM gain phase:



Note: the phase here is calculated from -180 to 180 but if it was calculated from 0 to 360 the graph would be smooth without this sharp transition.

The increase of CM gain at high frequencies is because at high frequencies the capacitors at node VP will have low impedance which reduces the degeneration impedance and increases the CM gain.

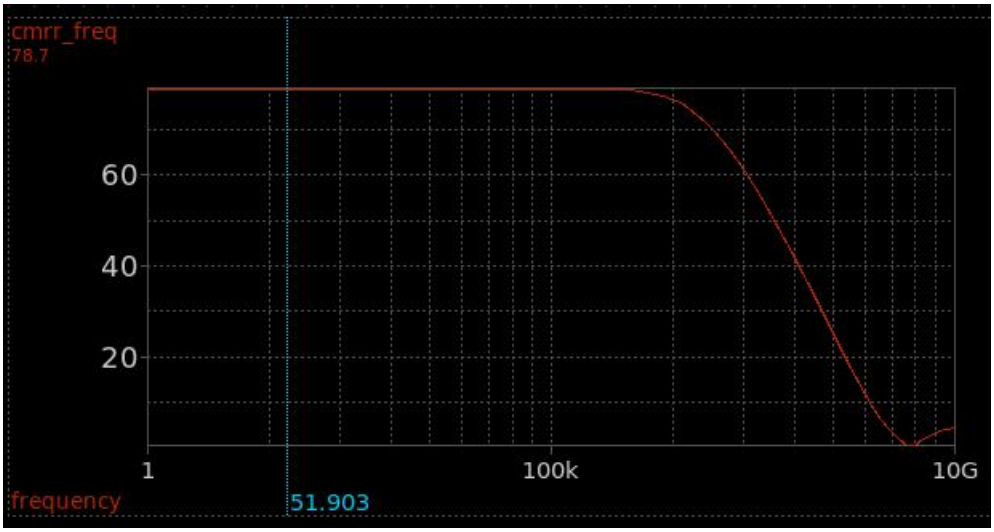
- Hand Analysis:

$$ACM = \frac{1}{2*gm3,4*ro5} = 7.79 * 10^{-3} = -42.16dB$$

	Hand Analysis	Simulation
CM gain	$-42.16dB$	$-44.54dB$

4) CMRR:

• Plot VOUT vs VID:



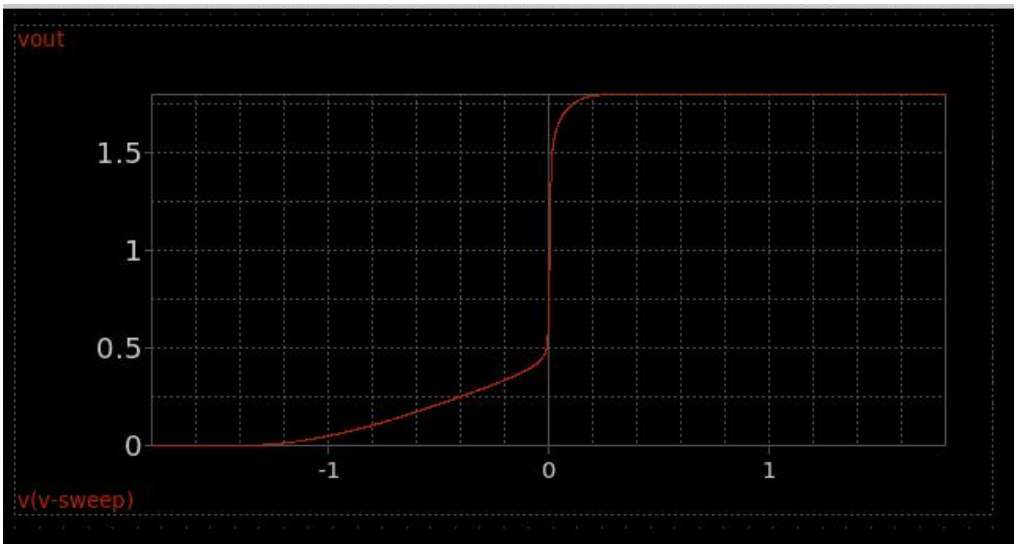
- Hand Analysis:

$$CMRR = \frac{Ad}{ACM} = 6611 = 76.4dB.$$

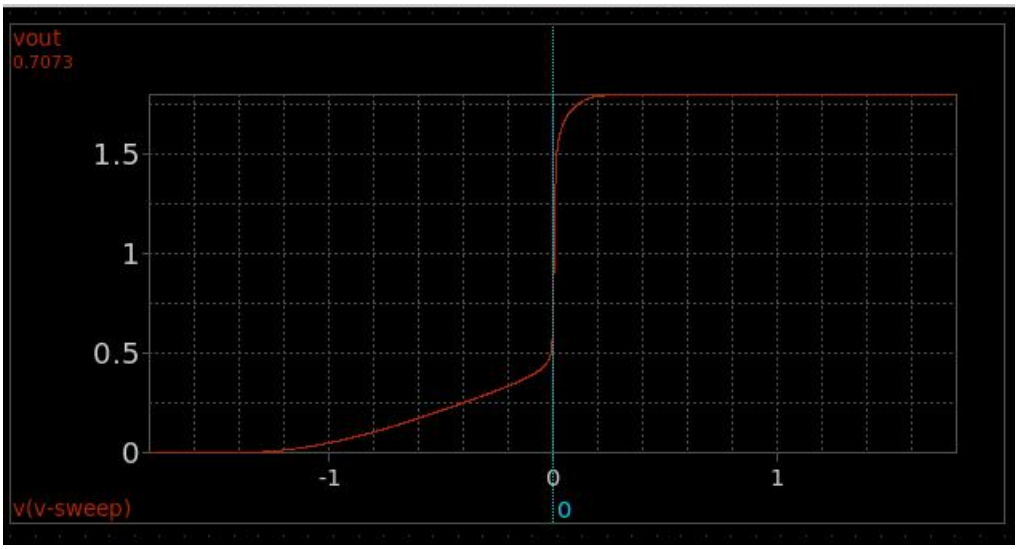
	Hand Analysis	Simulation
CMRR	$76.4dB$	$78.7dB$

5) Diff large signal ccs:

• Plot VOUT vs VID:

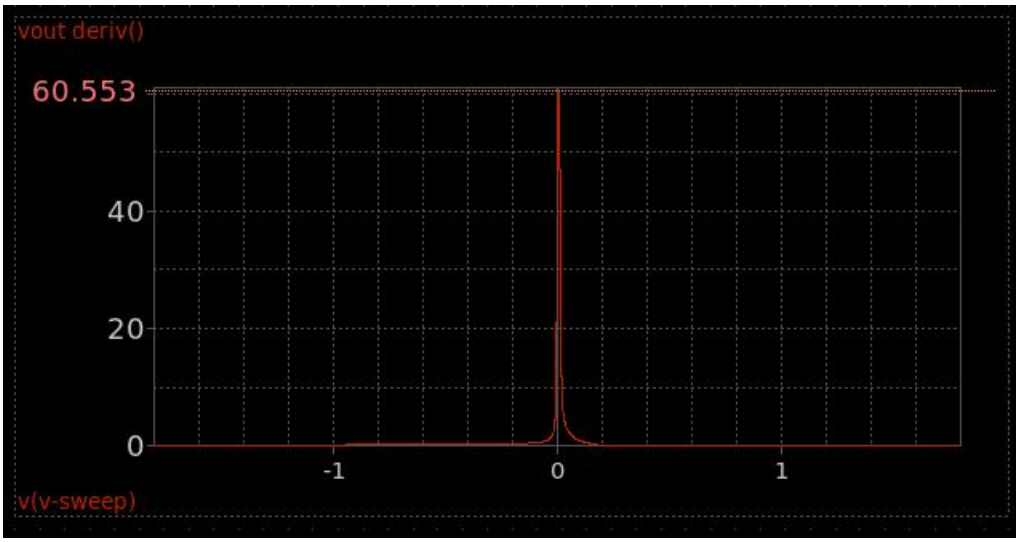


• From the plot, what is the value of Vout at VID = 0? Why?



$Vout = 07073$ approximately equals what we got when we got at page 7 Vout was 0.746 and this is expected as at VID=0 this is CM Bias so they should be the same and equal VF.

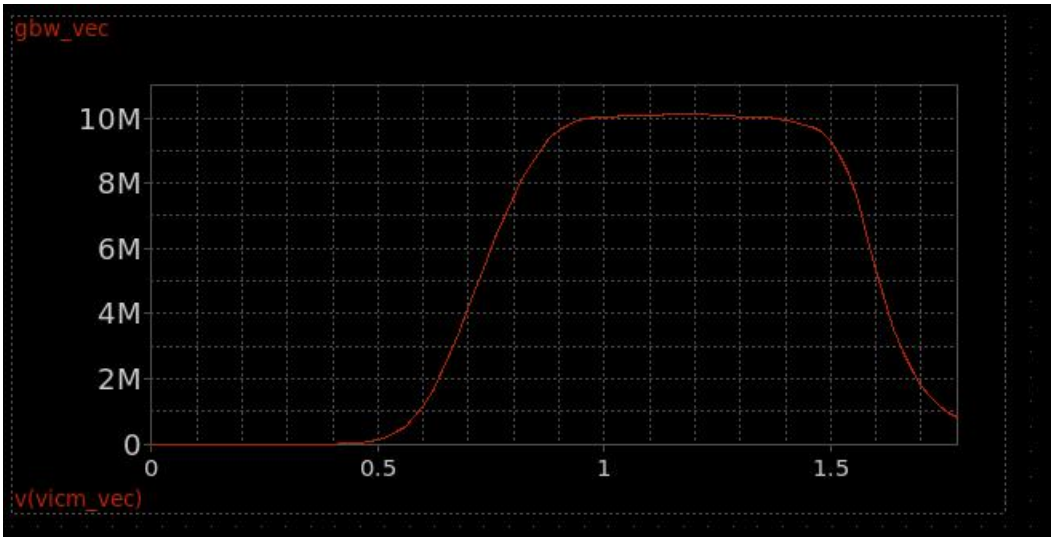
• Plot the derivative of VOUT vs VID. Compare the peak with Avd:



The peak =60.55 and $Avd = 51$ so the peak is higher than Avd but they should be the same value as they are the same thing but may be the problem is that the slope is very high so any small change changes the value and the step is quite high which increases the error in calculating the slope.

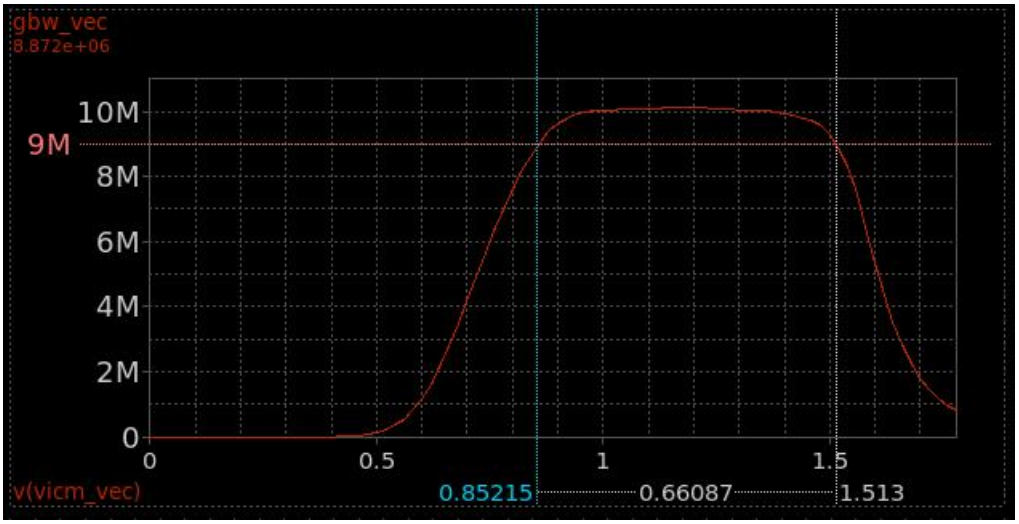
6) CM large signal ccs (GBW vs VICM):

• Plot GBW vs VICM:



• Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW

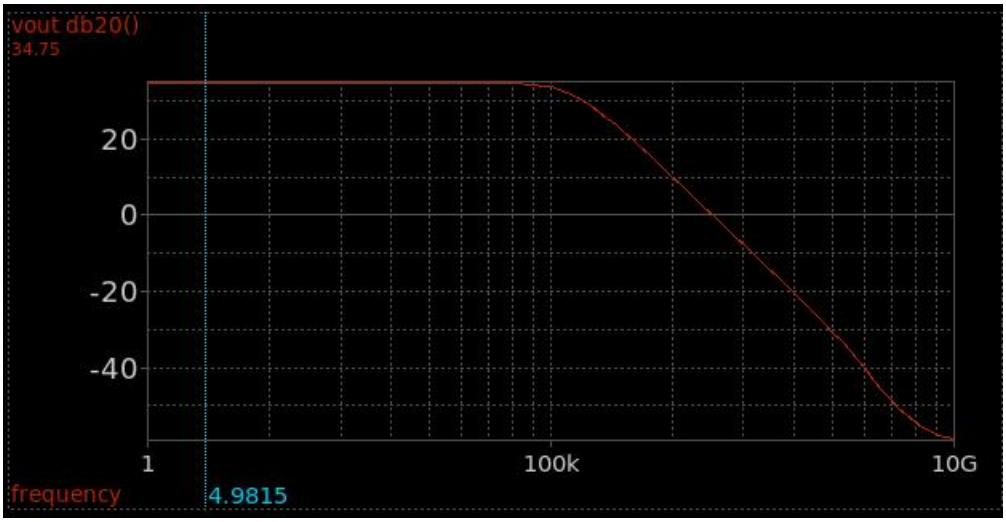
```
No. of Data Rows : 101
gain                =  1.373074e-01 at=  1.000000e+00
bw                  =  5.853156e+06
max_gbw             =  1.010622e+07 at=  7.943282e+05
min_vincm           =  8.633484e-01
max_vincm           =  1.510460e+00
min_vincm = 8.633484e-01
max_vincm = 1.510460e+00
cmir = 6.471116e-01
binary raw file "5t_ota_tb_cmir1.raw"
```



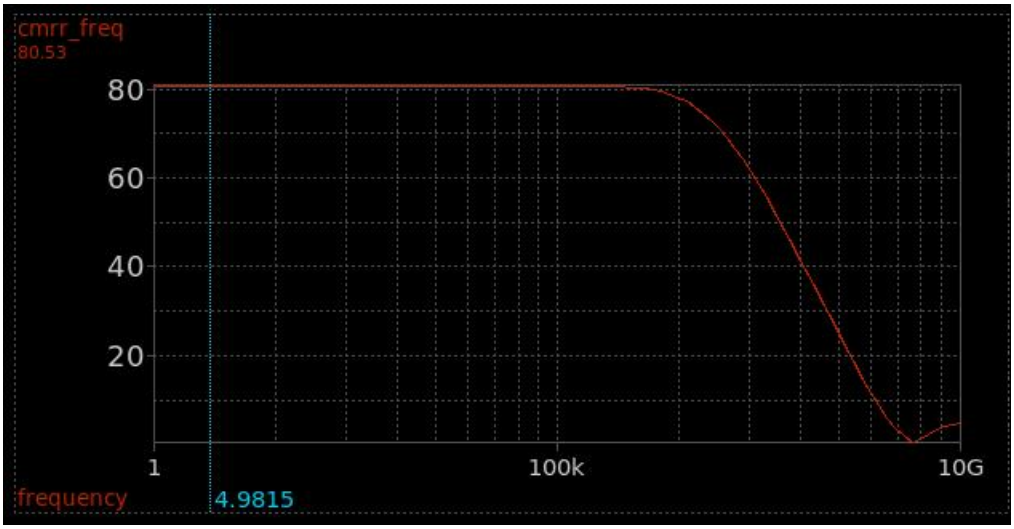
- We have $0.8633 < VICM < 1.51$ and the input range$= 0.647V$.
- The VICM max and GBW specs weren't achieved so
- First, We changed W3,4 from $2.8\mu m\ to\ 3.5\mu m$ to decrease Vstar3,4 so decrease VGS3,4 and we know $VCMmax = Vth1{,}2 - |VGS3{,}4| + VDD$ so we achieved the VCM max spec.
- Second, We changed W from $17.3\mu m\ to\ 20\mu m$ to increase gm1,2 for the same current so increase the GBW.

Checking that all specs are achieved after the edit of values:

Open loop DC gain:



CMRR:



- And the specs on GBW and CM input range are achieved in the last section so all specs are achieved.

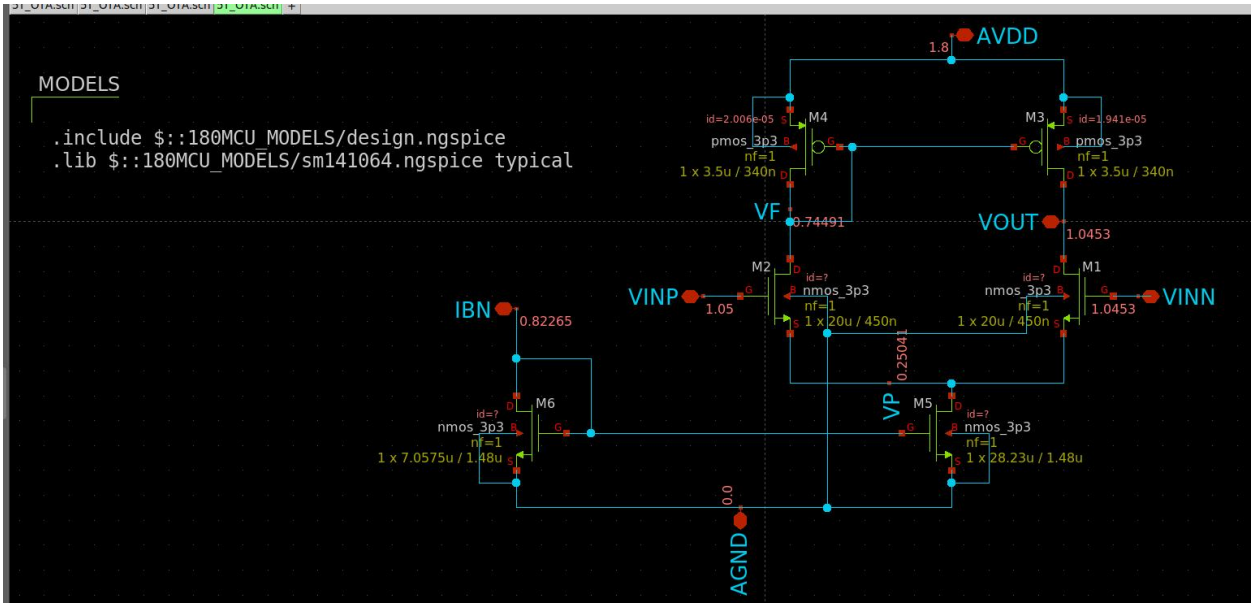
OP after edit:

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm6.m0          m.x1.xm4.m0          m.x1.xm3.m0
     model           nmos_3p3.10           pmos_3p3.8           pmos_3p3.8
        id                 1e-05          1.99155e-05          1.99155e-05
        gm           0.000101295          0.000116359          0.000116359
       gds            2.5173e-07          1.97368e-06          1.97368e-06
      gmbs           3.94132e-05          4.48433e-05          4.48433e-05
       vgs              0.822648              1.05386              1.05386
       vth              0.676836             0.759278             0.759278
       vds              0.822646              1.05385              1.05385
     vdsat              0.163568             0.292858             0.292858
       cgs          -2.27501e-14         -3.10674e-15         -3.10674e-15
       cgd          -4.94816e-18          1.15095e-17          1.15095e-17
       csb          -5.54631e-15         -7.46806e-16         -7.46806e-16
       cdb          -3.70318e-15         -4.98697e-16         -4.98697e-16

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm5.m0          m.x1.xm2.m0          m.x1.xm1.m0
     model           nmos_3p3.14          nmos_3p3.12          nmos_3p3.12
        id           3.98309e-05          1.99155e-05          1.99155e-05
        gm           0.000404684          0.000325502          0.000325502
       gds           1.56692e-06          3.93367e-06          3.93367e-06
      gmbs           0.000157513          8.90995e-05          8.90995e-05
       vgs              0.822648             0.844747             0.844747
       vth              0.677106               0.8281               0.8281
       vds              0.405248             0.340883             0.340883
     vdsat                0.1638            0.0973635            0.0973635
       cgs          -9.11035e-14         -1.04883e-14         -1.04883e-14
       cgd          -2.08558e-16          3.48632e-18          3.48632e-18
       csb          -2.22338e-14         -1.84823e-15         -1.84823e-15
       cdb          -1.49491e-14         -1.24124e-15         -1.24124e-15
```

PART 4: Closed-Loop OTA Simulation:

1) Schematic of the OTA with DC OP point clearly annotated:



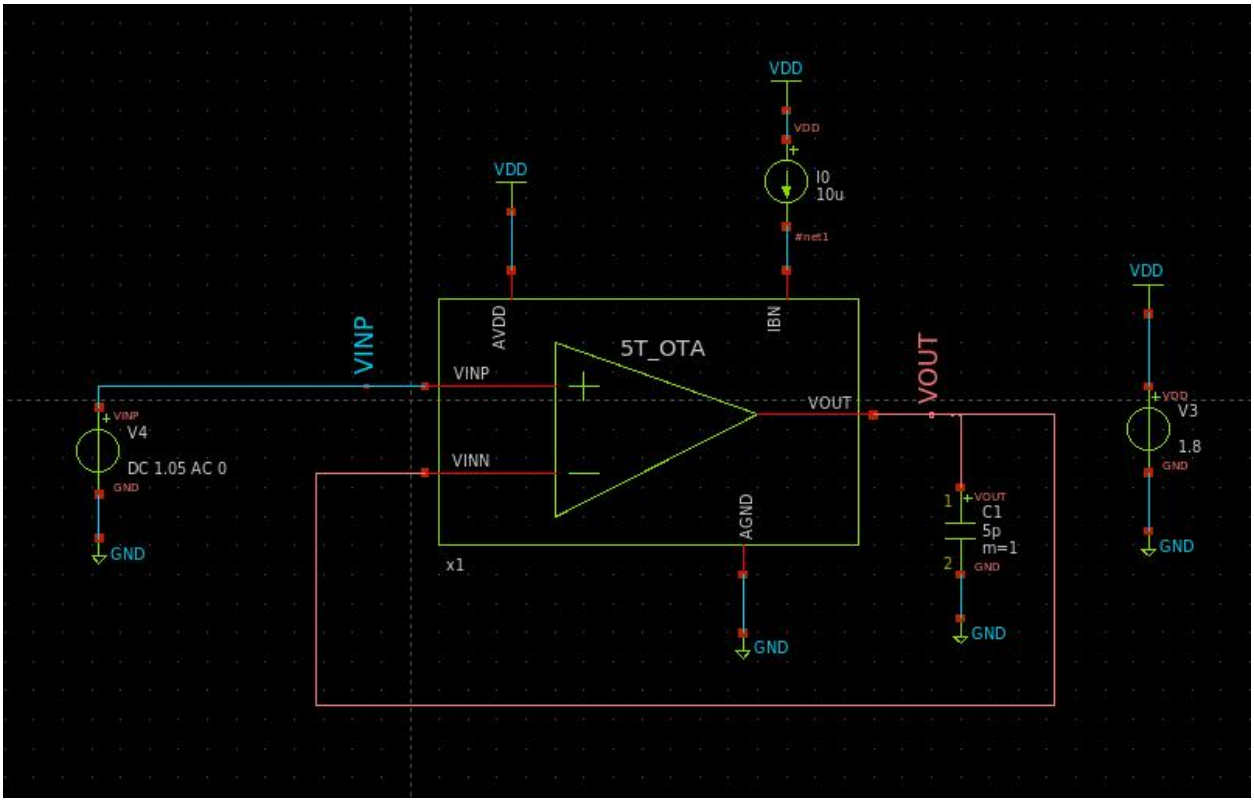
BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm6.m0	m.x1.xm4.m0	m.x1.xm3.m0
model	nmos_3p3.10	pmos_3p3.8	pmos_3p3.8
id	1e-05	2.00605e-05	1.94124e-05
gm	0.000101295	0.000116741	0.000113419
gds	2.5173e-07	1.98442e-06	2.37575e-06
gmbs	3.94132e-05	4.49942e-05	4.38298e-05
vgs	0.822648	1.05508	1.05508
vth	0.676836	0.759271	0.760992
vds	0.822646	1.05507	0.754642
vdsat	0.163568	0.293854	0.292466
cgs	-2.27501e-14	-3.10768e-15	-3.11105e-15
cgd	-4.94816e-18	1.15122e-17	8.45108e-18
csb	-5.54631e-15	-7.46937e-16	-7.49228e-16
cdb	-3.70318e-15	-4.98784e-16	-5.01718e-16

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm5.m0	m.x1.xm2.m0	m.x1.xm1.m0
model	nmos_3p3.14	nmos_3p3.12	nmos_3p3.12
id	3.94729e-05	2.00605e-05	1.94124e-05
gm	0.000399697	0.000328428	0.000320694
gds	4.12506e-06	3.18934e-06	2.65419e-06
gmbs	0.000155591	9.67358e-05	9.44281e-05
vgs	0.822648	0.799593	0.794937
vth	0.677106	0.784446	0.783693
vds	0.250403	0.494505	0.794935
vdsat	0.1638	0.096036	0.0940614
cgs	-9.14452e-14	-1.03867e-14	-1.014e-14
cgd	-1.11189e-15	1.43793e-17	1.85473e-17
csb	-2.23542e-14	-1.98344e-15	-1.93907e-15
cdb	-1.53579e-14	-1.32668e-15	-1.29428e-15

- Closed loop schematic:



• Is the current (and gm) in the input pair exactly equal? Why?

No, they aren't equal as $AOL = \frac{Vout}{Verr}$ _and note that Vout here is the change in Vout_ from this relation we find that Verr has a small value we can calculate it $Verr = \frac{1.05-0.746}{51.5} = 5.9 * 10^{-3}$ and we know that $Verr = VINP - VINN = 1.05 - VINN = 5.9 * 10^{-3}\ then\ VINN = 1.044.$ ad this change in VGS changes the current and gm more current will be in the branch of VINP as it has higher VGS.

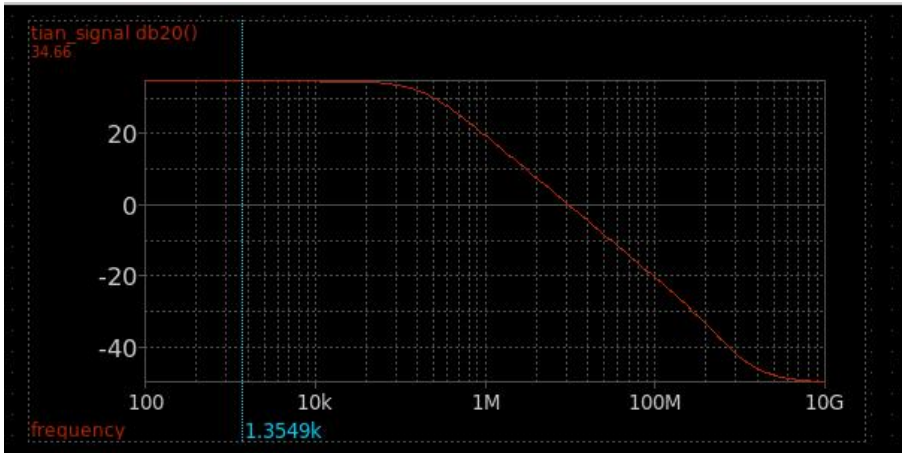
• Calculate the mismatch in ID and gm:

$$Current\ mismatch = \frac{20-19.4}{20} * 100 = 3\%$$

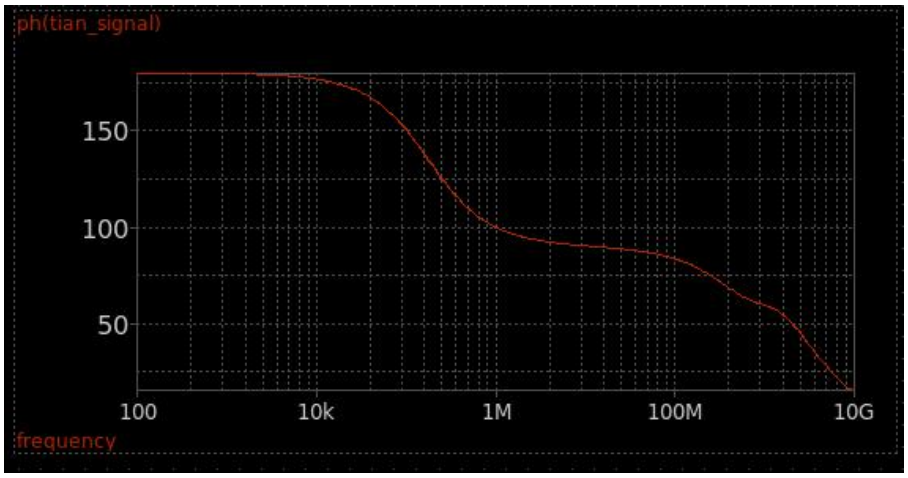
$$gm\ mismatch = \frac{328.4-320.7}{328.4} * 100 = 2.3447\%$$

2) Loop gain:

• Plot loop gain in dB and phase vs frequency:



- LG phase:



- PM spec:

```
gain_crossover_freq =  9.565370e+06
phaseatzerogain     =  9.042466e+01
pm = 8.957534e+01
```

➢ We can find that $PM = 89.5 > 70$ which meets the spec.

• Compare DC gain and GBW with those obtained from open-loop simulation. Comment.

	Loop gain	Open loop
Gain	54	54.64
GBW	$9.565MHz$	$10MHz$

- Comment:

The $LG = beta * Aol$ and beta=1 then $LG = Aol$ and it is expected to have the same gain and GBW. We took GBW for LG =gain cross over freq but it will be slightly higher.

Closed loop results:

```
gain                =  9.791690e-01 at=  1.000000e+00
bw                  =  1.007271e+07
gbw = 9.862885e+06
binary raw file "Lab7_AC.raw"
```

	Closed loop	Open loop
Gain	0.979	54.64
GBW	$9.86MHz$	$10MHz$

- Comment:

➢ The closed loop gain is divided by the factor (1+LG) which equals 55.64 so $ACL = \frac{54.64}{55.64} = 0.982$ which is true and GBW was expected to be the same as the BW will increase with the same factor (1+LG) so GBW is constant which is approximately true.

• Compare simulation results with hand calculations in a table:

Hand Analysis:

$ACL = \frac{54.64}{55.64} = 0.982$.

$GBWcl = GBWol = 10MHz.$

	Hand Analysis	Simulation
Gain	0.982	0.979
GBW	$10MHz$	$9.86MHz$

Spec comparison:

Parameter	required	result
Open loop dc voltage gain	$\geq 34\ dB$	$34.75dB$
CMMR at dc	$\geq 74\ dB$	$78.7dB$
Phase margin	$\geq 70°$	$89.5°$
CM input range low	$\leq 1\ V$	$0.8633V$
CM input range high	$\geq 1.5\ V$	$1.51V$
GBW	$\geq 10\ MHz$	$10MHz$