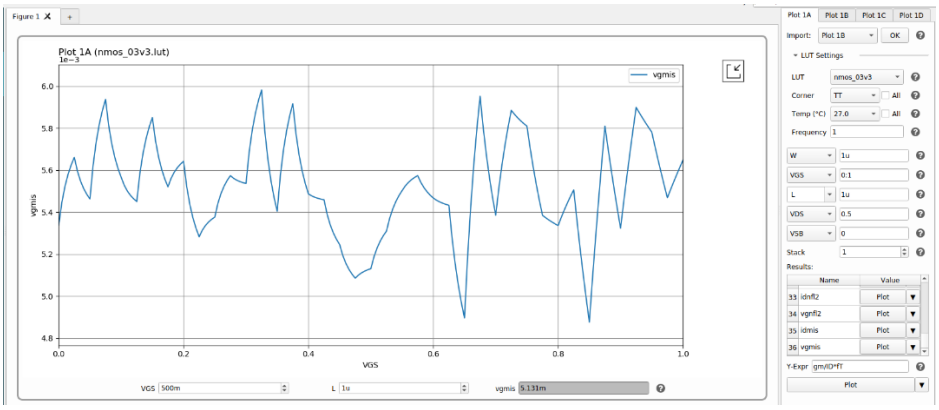
Lab 05

PART 1: Sizing chart:

- **Specs:**

Parameter	value
Input Current	$10\mu A$
Output Current	$20\mu A$
Change in current for $\Delta \boldsymbol{Vout} = \boldsymbol{1V}$	$\leq 10\%$
Mismatch percentage	$\leq 2\%$
Compliance voltage	$\leq 150mV$
Area	Minimize

- **Sinking current means which device type? NMOS or PMOS?**
  To sink current, we need to use NMOS.
- **The % Change in current translates to a spec on the λ = 1/VA of the device. How much is the required λ?**
  By substituting in square law we find $1.1ID = ID(1 + \lambda * 1)$ then $\lambda \leq 0.1\, V^{-1}$.
- **Choosing The current mirror bias point depending on trade-offs:**
  We will choose the $V^* = 150mv$ which is the highest value that achieves the compliance voltage condition. We chose it to minimize Area and mismatch errors systematic or random.
- **Mismatch effect (Vgmis Vs Vgs):**



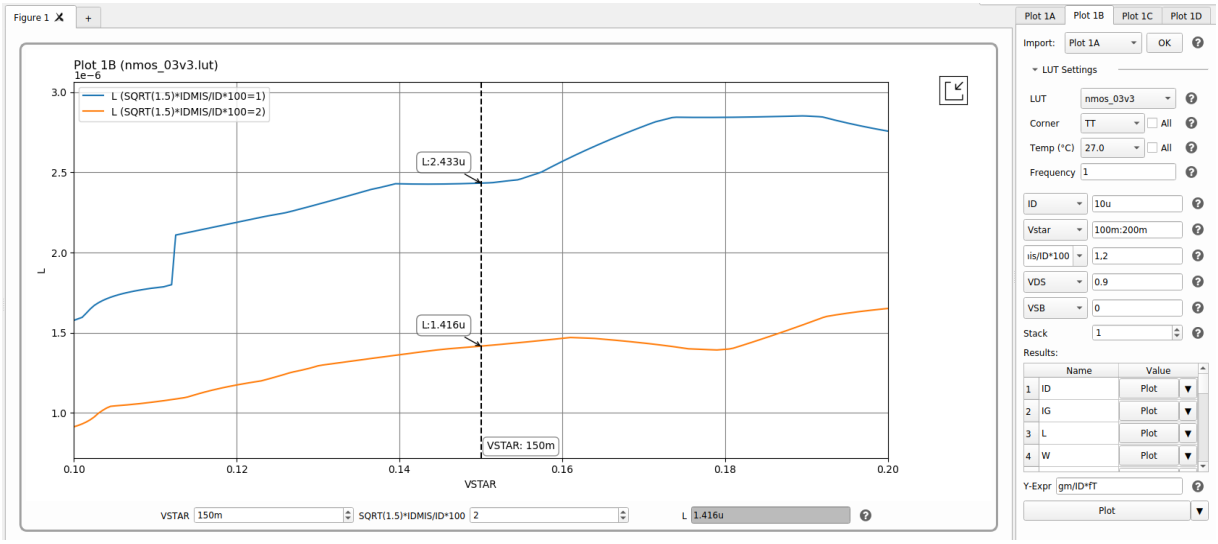
- **From the model file, calculate σVT (var_vth at WxL = 1um2) and compare it to the value in ADT. Which one is higher, why?**

```
.param
+ par_vth=0.007148
+ par_k=0.007008
+ par_l=1.5e-7
+ par_w=-1e-7
+ par_leff='l-par_l'
+ par_weff='par*(w-par_w)'
+ p_sqrtarea='sqrt((par_leff)*(par_weff))'

.param
+ var_k='0.7071*par_k* 1e-06 / p_sqrtarea'
+ mis_k=agauss(0,var_k,1)

.param
+ var_vth='0.7071*par_vth* 1e-06 / p_sqrtarea'
+ mis_vth=agauss(0,var_vth,1)

m0 d g s b nmos_3p3 w=w l=l as=as ad=ad ps=ps pd=pd nrd=nrd nrs=nrs
+delvto='mis_vth*sw_stat_mismatch'  sa=sa sb=sb nf=nf sd=sd
.ends nmos_3p3
```

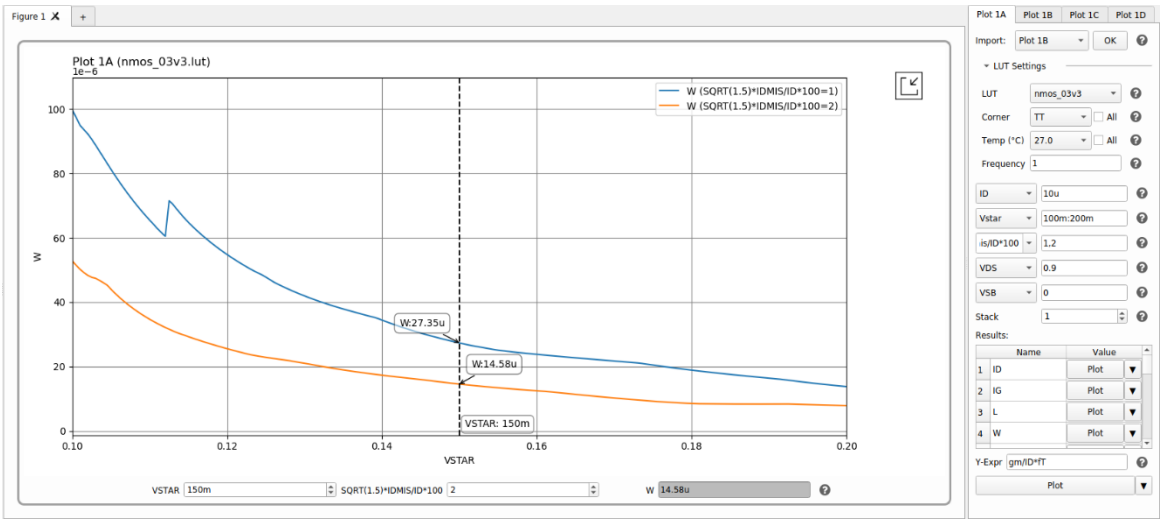
Calculating from file: $mismatch = \frac{0.7071*0.007148*10^{-6}}{\sqrt{(L-1.5*10^{-7})*(W+10^{-7})}}$ $for\ L\ and\ W = 1\mu m$ we find that $mismatch = 5.227mv$.

Averaging the simulated graph, we find that $mismatch = 5.5mv$. so the ADT simulated result is higher as it takes into account other variation like ro but the calculated is for Vth only. Also, the randomness affects the results slightly but ADT results are always higher.

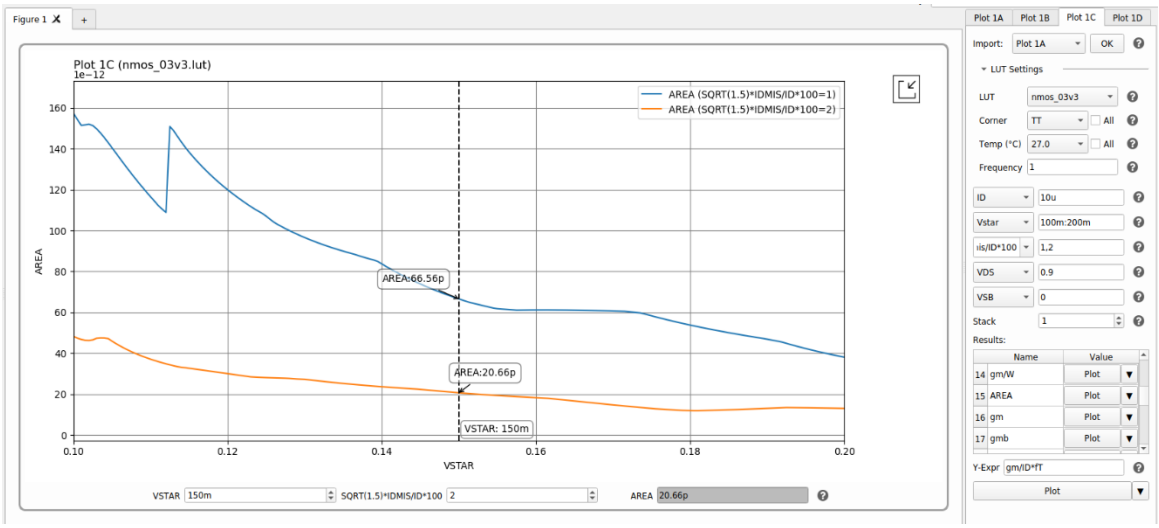
- **Examine these trade-offs using SA. Use SA to plot the sizing at a constant $\sigma(Iout)/Iout$:**
  - L VS current bias point:



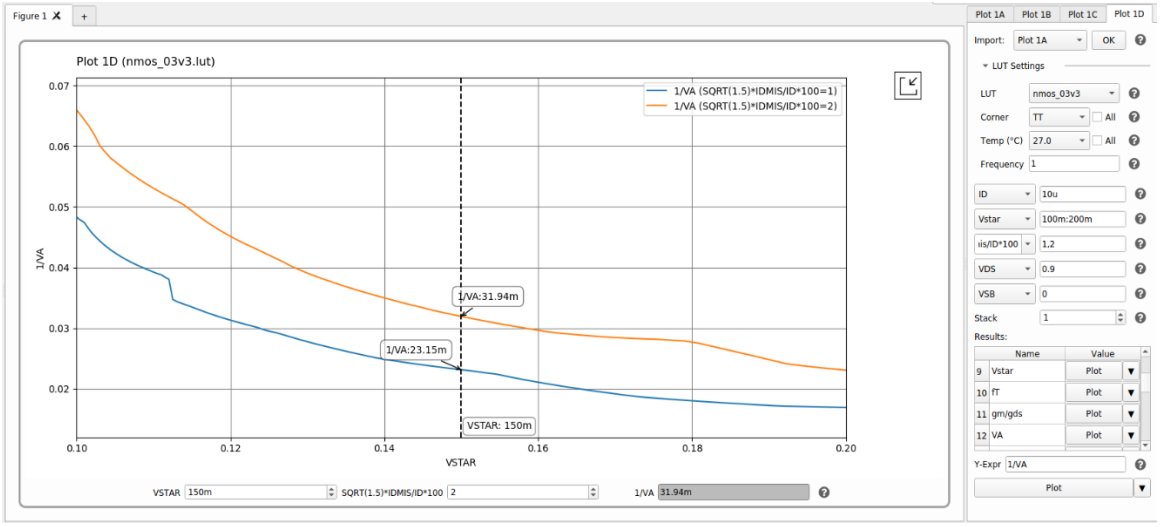
- W VS bias point:



- Area VS bias point:



- λ VS bias point:

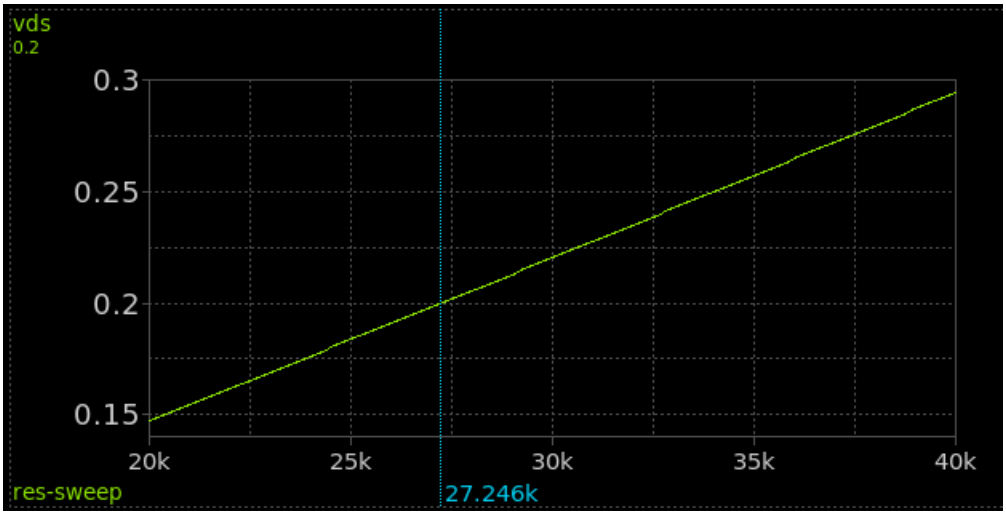


- **Report the above plot with a cursor added at the required $V*$. Does this point satisfy the mismatch and λ constraints?**
  The point satisfies the constrains as $\lambda = 0.03194 < 0.1$. so we will choose the point on the curve of 2% current mismatch which satisfies all conditions and gets minimum area.
- **Report the device sizing and $\boldsymbol{\sigma(Iout)/Iout}$ at the selected design point:**
  The sizing we choose is $\frac{W}{L} = \frac{14.58\mu m}{1.416\mu m}$ and $\boldsymbol{\sigma(Iout)}/Iout$=2%.

Part 2: Current Mirror Simulation:

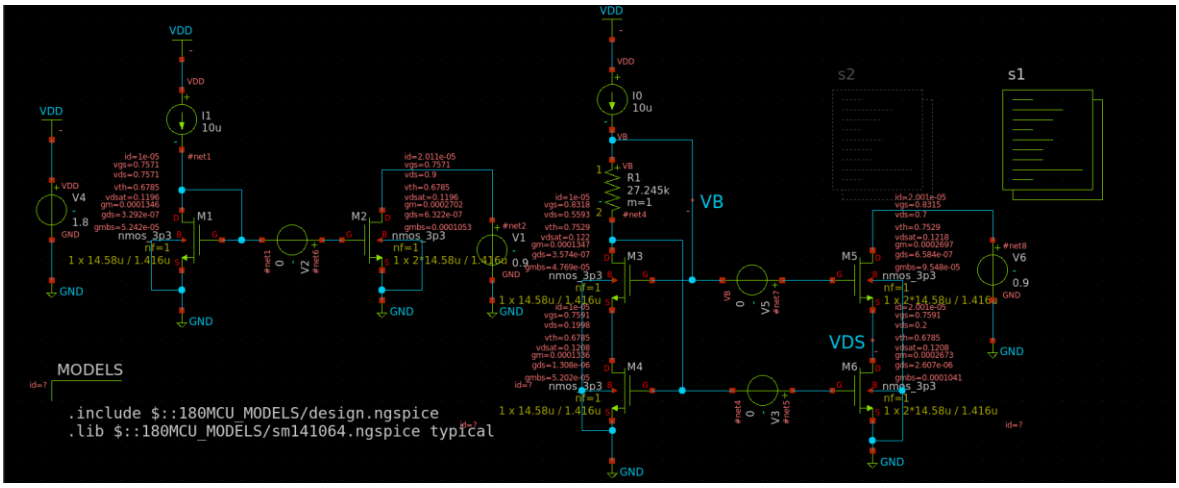
1. Design and OP (Operating Point) Analysis:

- **Calculating RB:**
  $RB = \frac{VGS5+VDS6-VGS4}{IB} \approx \frac{VDS6}{IB} = \frac{0.2}{10*10^{-6}} = 20k\Omega$ it is an approximated result as VGS5 is higher than VGS4 because of body effect. We can sweep to get the actual result.



  We got $RB = 27.246k\Omega$.
- **Is the selected RB value larger or smaller than the rough analytical value? Why?**
  The value we chose is larger as we expected as the VGS5 has higher value because of the body effect which increases VTH.

- **Simulate the OP point. Report a snapshot clearly showing the following parameters**:

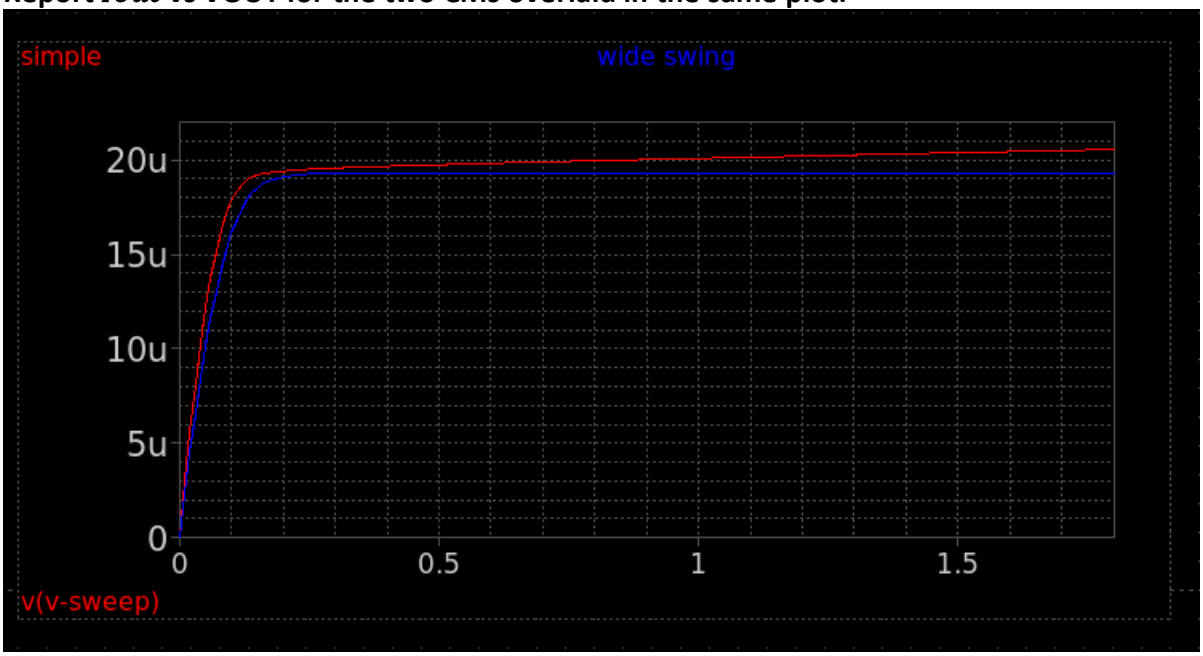


- **Do all transistors operate in saturation?**

  Yes, all transistors are in saturation region as VDS>VDSsat for all transistors.

2. DC Sweep (*Iout* vs VOUT):

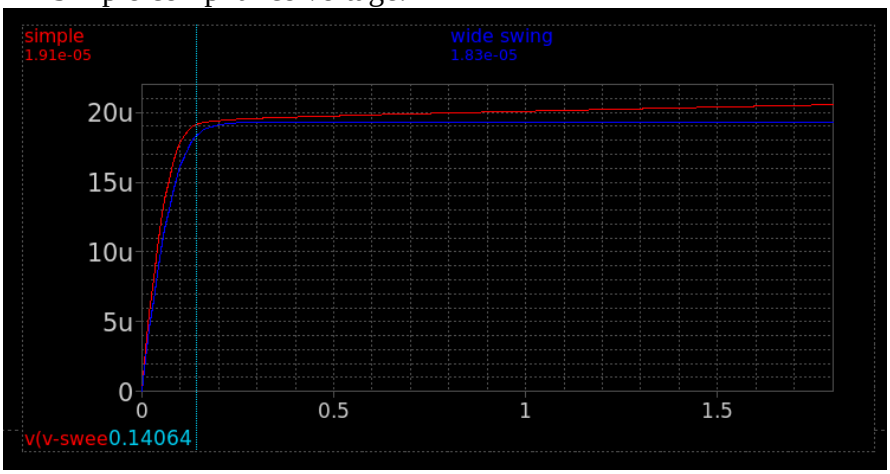
- **Report *Iout* vs VOUT for the two CMs overlaid in the same plot:**



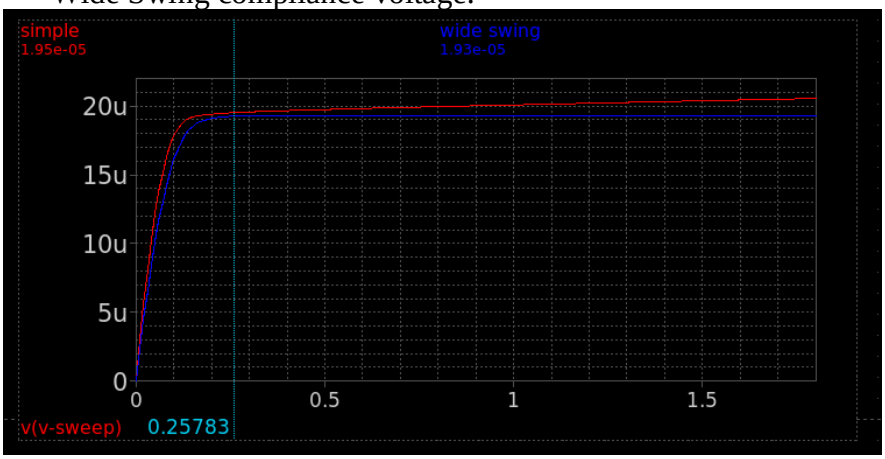
- **Comment on the difference between the two circuits:**

  The Wide Swing circuit allows more accurate mirroring as it makes VDS1≈VDS2. The wide swing has also higher Rout which is better. It has a slightly higher compliance voltage than the simple but it is not a major drawback.

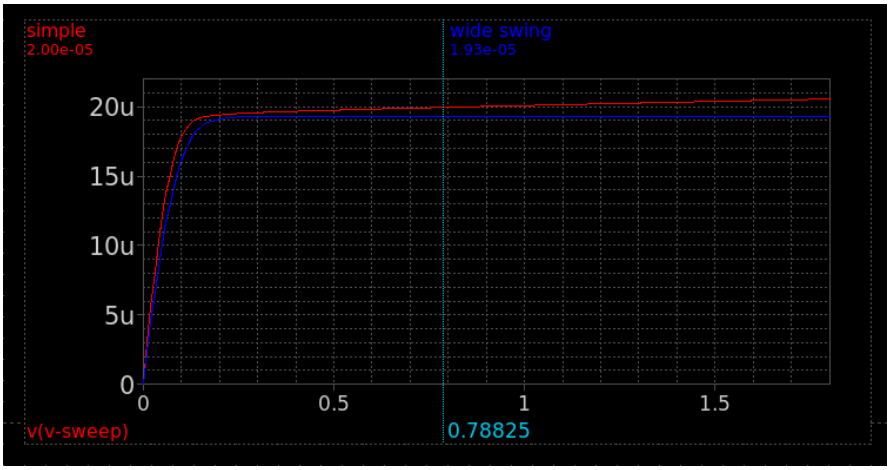
- **From the plot, find an estimate for the compliance voltage of each current mirror:**
  - Simple compliance voltage:



  - Wide Swing compliance voltage:

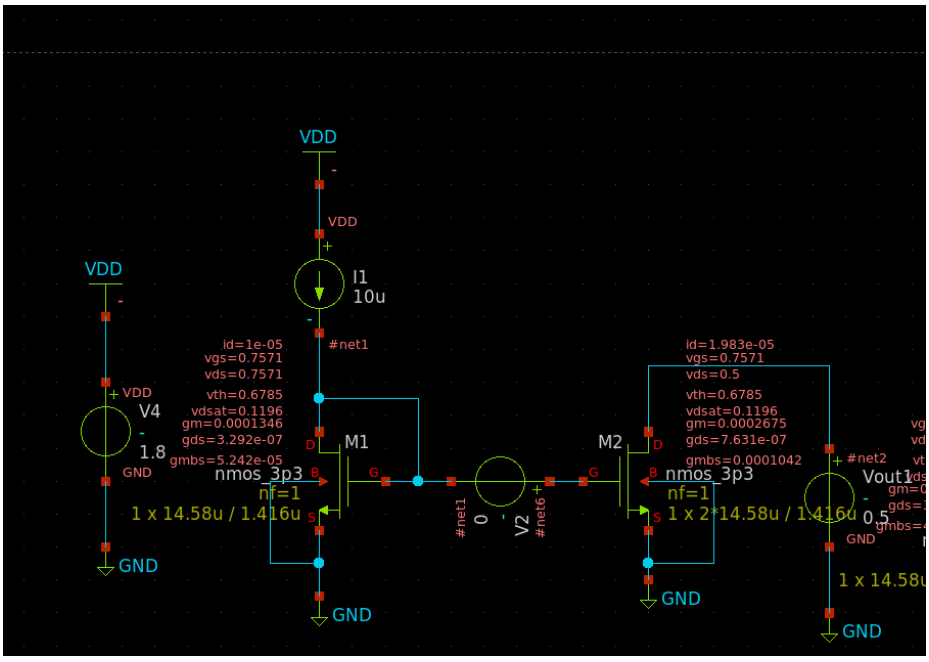


- ***Iout* of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?**

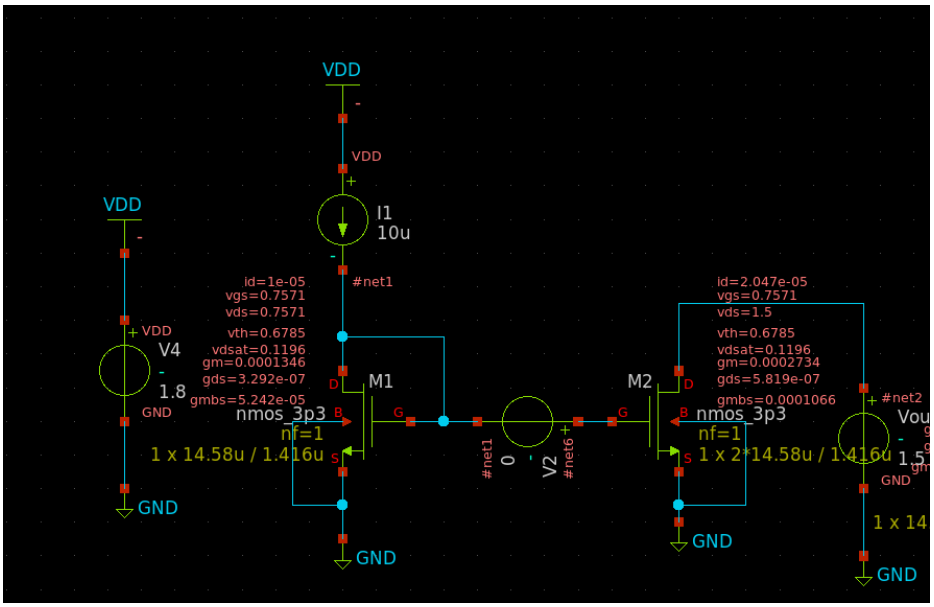


Iout here is exactly $20\mu A$ as at this point VDS2$\approx VDS1$.

- **For the simple current mirror, calculate the percent change in $Iout$ when VOUT changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part1:**
  - At Vout=0.5:



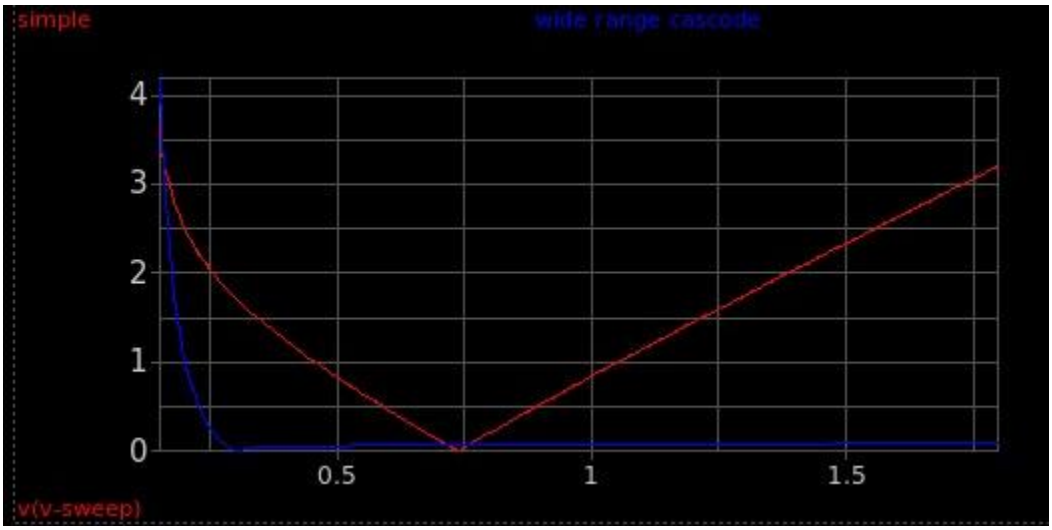
  - At Vout=1.5:



$change\ in\ Iout = \frac{20.47-19.83}{19.83} * 100 = 3.22\%$

Comparing it to the lambda in part1 $\lambda = 0.03194$, we expected in part1 that the change will be $\lambda * 100\%$ so the results are approximately the same.

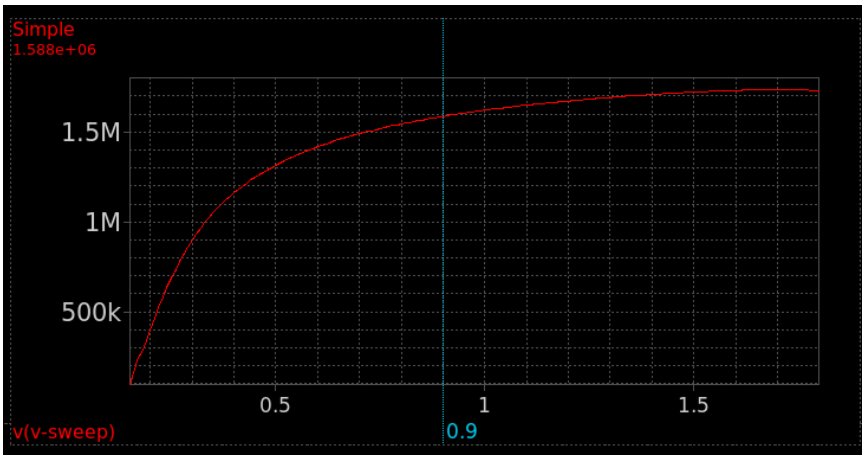
- **Report the percent of error in $Iout$ vs VOUT overlaid:**

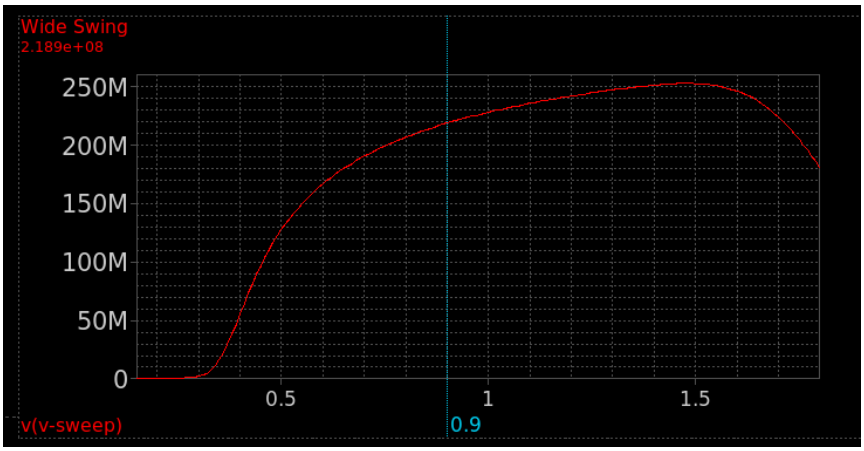


Comments:

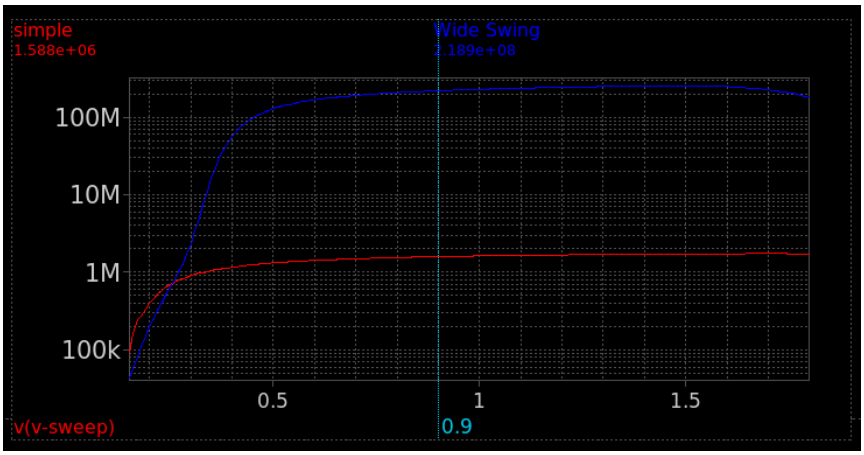
Wide swing cascode almost has no error in the operating region compared to the simple until the Vout is near the compliance voltage the error increases. For the simple there is higher error in mirroring except at the points near the VDS1.

- **Report Rout vs VOUT:**





- **Overlaid results with log Y:**



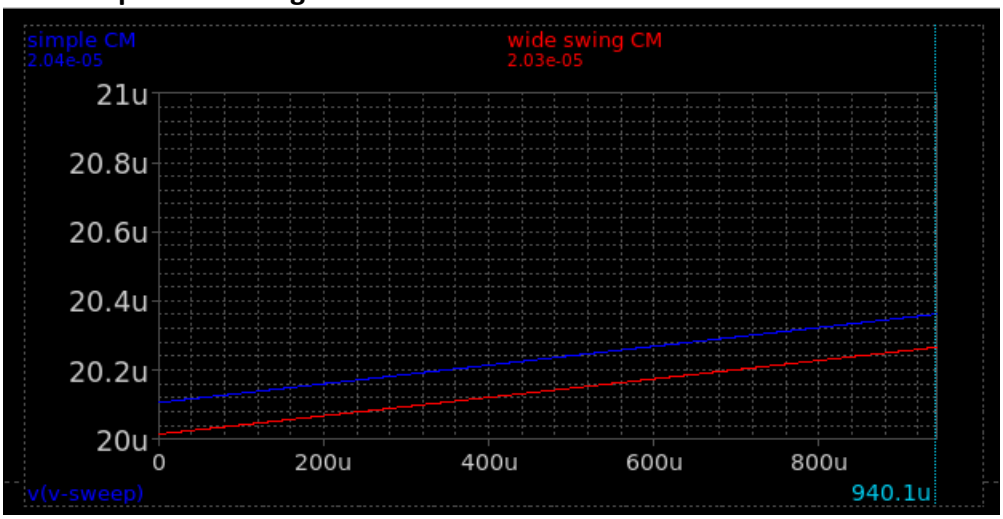
- **Overlaid results with log Y and log X:**

- **Comment on the difference between the two circuits:**
  Wide Swing CM has a lot higher Rout than simple CM which is better as it reduces the dependency of the current on VDS.
- **Does Rout change with VOUT? Why?**
  Yes, it changes as ro depends on VDS and Rout in both circuits depends on ro.
- **Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table:**
  Simple CM: $Rout = ro = 1.579M\Omega$.
  Wide Swing Cascode Rout: $Rout = ro1 + ro2 + (gm + gmb)ro1 * ro2 = 214.36M\Omega$.

	Analytical	Simulation
Simple	$1.579M\Omega$	$1.588M\Omega$
Wide Swing	$214.36M\Omega$	$218.9M\Omega$

3. Mismatch:

- **Find the percent change in $Iout$ for VMIS1:**



Simulation:

In Simple: $error = \frac{20.04-20.1}{20.1} * 100 = 1.49\%$

In wide swing: $error = \frac{20.3-20}{20} * 100 = 1.5\%$

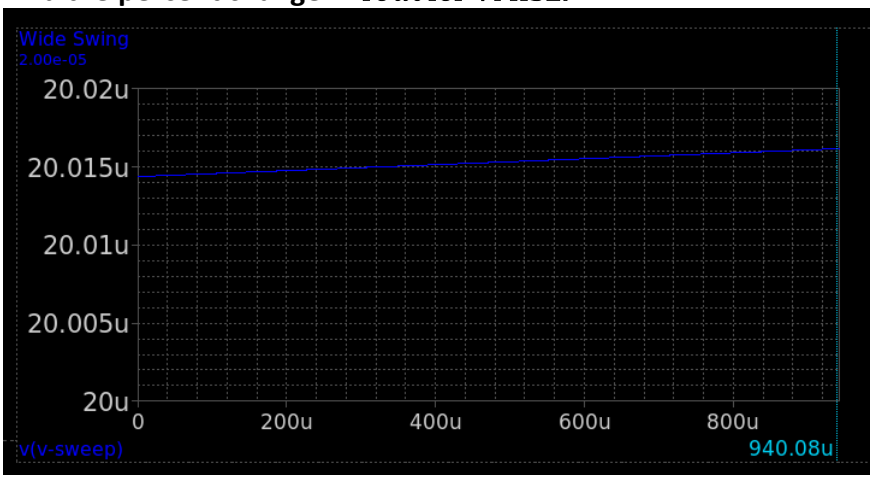
Analytically:

In Simple: $\Delta Iout = gm * Vgmis = 0.255\mu A$, $percentage = \frac{\Delta Iout}{Iout} = 1.268\%$

In wide swing: $\Delta Iout = gm * Vgmis = 0.252\mu A$, $percentage = \frac{\Delta Iout}{Iout} = 1.26\%$

	Analytical	Simulation
Simple	1.268%	1.49%
Wide Swing	1.26%	1.5%

- **Find the percent change in $Iout$ for VMIS2:**



Simulation:

$error = \frac{20.016-20.014}{20.014} * 100 = 0.01\%$

Analytically:

$\Delta Iout = Gm * Vgmis = \frac{gm}{1+gm*ro} * Vgmis = 2.43nA$ which is negligible.

$Percentage = 0.012\%$

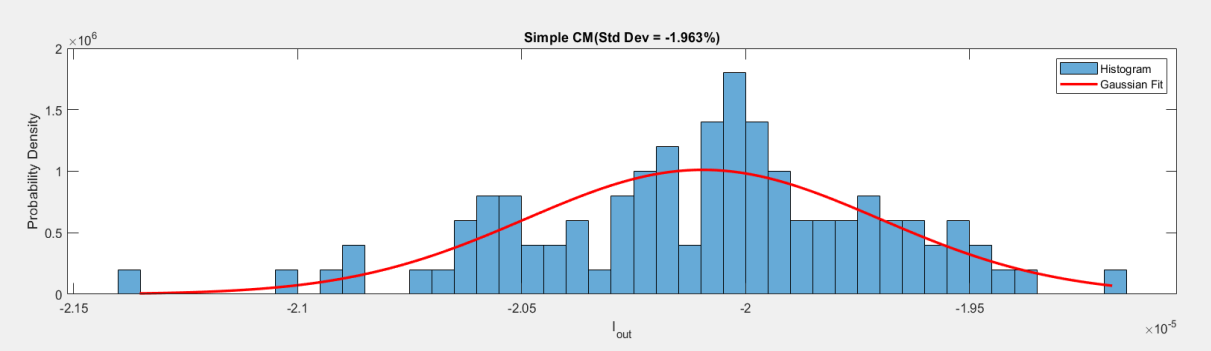
	Analytical	Simulation
Wide Swing	0.012%	0.01%

- **Which mismatch contribution is more pronounced? Why?**
  The mismatch in the mirror transistors is more pronounced as the cascode transistors' mismatch gets degeneration which reduces its effect a lot on the current but the mirror transistors has $Gm = gm$.
- **Which design decision is better: setting the same W and L for the mirror and cascode devices? Or using larger W and L for the current mirror devices? Why?**
  using larger W and L for the current mirror devices is better to reduce the mismatch error for the mirror transistors. The cascode transistors mismatch already has a small value so using large W and L for them is useless it will increase the area and cost for no benefit.

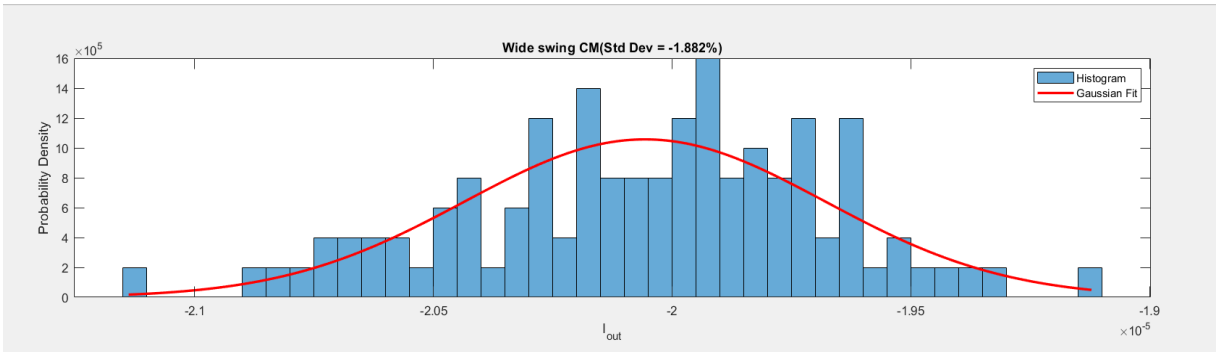
4. Monte Carlo (MC) Simulation:

- **Histogram and standard deviation:**

- Simple CM:



- Wide Swing CM:



➢ **Compare the MC simulation result to the expected analytical result:**
The expected analytical mismatch error is 2% and we can find that the Monte Carlo simulation for both circuits are very close to what we expected and they maintain the condition that $Mismatch\ error < 2\%$