

# Design Challenge 1

## PART 1:

- **From the closed loop specs, calculate the OTA open loop specs.**
  - $BW_{cl} = BW_{ol} * (1 + \beta A_{ol}) \approx BW_{ol} * \beta A_{ol} \approx \beta * GBW_{ol}$
  - We want  $BW_{cl} = 10MHz$  then worst GBW will be at the lowest  $\beta = \frac{C_f}{C_f + C_{in}} = \frac{1}{5}$  at the  $gain = 4$  then  $GBW_{ol} = 50MHz$ .
  - $\frac{g_{m-input}}{2\pi * C_c} = 50MHz$ , We will assume  $C_c$  half the worst  $C_{out}$  and worst  $C_{out}$  is at the unity gain buffer connection then  $C_{out} = C_{in} + C_f = 2.5pF$  then  $C_c = 1.25pF$  and we get  $g_{m-input} = 392.699\mu S$ .
  - $LG = \beta A_{ol} = 54dB = 501.18$  then  $A_{ol} = 2505.9$ .
  - Finally, the  $BW_{ol}$  will depend on the value of  $A_{ol}$  we get as  $GBW_{ol}$  will stay constant.
- **OTA topology selection and design steps (use ADT cockpit or the Sizing Assistant).**
  - The gain is high and we need high output swing so we will use the two-stage miller OTA. We can't use folded or telescopic as they have low output swing.
  - We will distribute the gain between the two stages  $A_1 = 38dB = 79.43$  and  $A_2 = 30dB = 31.6227$ .
  - We will start with the input pair. We will assume  $\frac{g_m}{I_D} = 16$  and then assume  $I_D = 25\mu A$  to get  $g_m = 400\mu S$ .
  - To achieve the gain spec,  $\frac{g_m}{g_{ds-input} + g_{gs-load}} \geq 79.43$  We will assume input pair and CM load have the same  $g_{ds}$  and take the first stage gain to be 90 then  $\frac{g_m}{g_{ds}} = 180$ .

Plot 1A
Plot 1B
Plot 1C
Plot 1D

Import: Plot 1B
OK
?

LUT Settings

ID 25u
gm/ID 16
gm/gds 180
VDS 0.6
VSB 0
Stack 1

Results:

	Name	TT-25.0
1	ID	25u
2	IG	0
3	L	2.12u
4	W	76.65u
5	VGS	613.6m
6	VDS	600m
7	VSB	0
8	gm/ID	15.66
9	Vstar	127.8m

Y-Expr gm/ID\*ft
Plot

Plot 1A
Plot 1B
Plot 1C
Plot 1D

Import: Plot 1B
OK
?

LUT Settings

ID 25u
gm/ID 16
gm/gds 180
VDS 0.6
VSB 0
Stack 1

Results:

	Name	TT-25.0
10	ft	102MEG
11	gm/gds	178.2
12	VA	11.38
13	ID/W	326.2m
14	gm/W	5.106
15	AREA	162.5p
16	gm	391.4u
17	gmb	106.3u
18	gds	2.196u

Y-Expr gm/ID\*ft
Plot

Plot 1A
Plot 1B
Plot 1C
Plot 1D

Import: Plot 1B
OK
?

LUT Settings

ID 25u
gm/ID 16
gm/gds 180
VDS 0.6
VSB 0
Stack 1

Results:

	Name	TT-25.0
19	ro	455.3k
20	Ron	24k
21	VTH	570.4m
22	VDSAT	88.02m
23	cgg	610.7f
24	cdd	47.01f
25	csg	469.8f
26	cdg	27.22f
27	cgd	24.68f

Y-Expr gm/ID\*ft
Plot

- Now, We will design the tail current source. To put  $V_{incm} = 1V$  then  $V_{GS1} + V_{Dsat3} \leq 1$  then  $V_{Dsat3} \leq 0.3864$ . We will choose  $V^* = 0.2V$  then  $\frac{gm}{ID} = 10$ .
- We will assume  $L = 4\mu m$  to increase  $ro$  and have less variations when  $VDS$  changes. And we know that  $ID = 50\mu A$ .

Plot 1A
Plot 1B
Plot 1C
Plot 1D

Import: Plot 1B
OK
?

LUT Settings

ID 50u
gm/ID 10
L 4u
VDS 0.6
VSB 0
Stack 1

Results:

	Name	TT-25.0
1	ID	50u
2	IG	0
3	L	4u
4	W	74.43u
5	VGS	717m
6	VDS	600m
7	VSB	0
8	gm/ID	9.89
9	Vstar	202.2m

Y-Expr gm/ID\*ft
Plot

Plot 1A
Plot 1B
Plot 1C
Plot 1D

Import: Plot 1B
OK
?

LUT Settings

ID 50u
gm/ID 10
L 4u
VDS 0.6
VSB 0
Stack 1

Results:

	Name	TT-25.0
10	ft	61.89MEG
11	gm/gds	249.4
12	VA	25.21
13	ID/W	671.8m
14	gm/W	6.644
15	AREA	297.7p
16	gm	494.5u
17	gmb	133.1u
18	gds	1.983u

Y-Expr gm/ID\*ft
Plot

Plot 1A
Plot 1B
Plot 1C
Plot 1D

Import: Plot 1B
OK
?

LUT Settings

ID 50u
gm/ID 10
L 4u
VDS 0.6
VSB 0
Stack 1

Results:

	Name	TT-25.0
19	ro	504.3k
20	Ron	12k
21	VTH	562.5m
22	VDSAT	149.5m
23	cgg	1.272p
24	cdd	49.7f
25	csg	1.028p
26	cdg	30.96f
27	cgd	25.77f

Y-Expr gm/ID\*ft
Plot

- To design the current mirror of the second stage we want it to match tail current source then  $L = 4\mu m$  and  $\frac{gm}{ID} = 10$  and we will use  $ID = 100\mu A$  as it is a reasonable when calculating the PM spec in the next step.

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 100u ?

gm/ID 10 ?

L 4u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
1 ID	100u
2 IG	0
3 L	4u
4 W	148.9u
5 VGS	717m
6 VDS	600m
7 VSB	0
8 gm/ID	9.89
9 Vstar	202.2m

Y-Expr gm/ID\*FT ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 100u ?

gm/ID 10 ?

L 4u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
10 ft	61.89MEG
11 gm/gds	249.4
12 VA	25.21
13 ID/W	671.8m
14 gm/W	6.644
15 AREA	595.4p
16 gm	989u
17 gmb	266.3u
18 gds	3.966u

Y-Expr gm/ID\*FT ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 100u ?

gm/ID 10 ?

L 4u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
19 ro	252.1k
20 Ron	6k
21 VTH	562.5m
22 VDSAT	149.5m
23 cgg	2.543p
24 cdd	99.39f
25 csg	2.056p
26 cdg	61.93f
27 cgd	51.54f

Y-Expr gm/ID\*FT ?

Plot

- $PM = 90 - \tan^{-1}\left(\frac{\omega u}{\omega p2}\right) = 60$  then  $\omega u < \frac{\sqrt{3}}{3}\omega p2$  then  $\frac{gm_{1,2}}{2\pi*Cc} < \frac{\sqrt{3}}{3} \frac{gm_4}{2\pi* Cout}$  then  $gm_4 > 2\sqrt{3}gm_{1,2}$  then  $gm_4 > 1385.64\mu S$ . We choose  $gm_4 = 1400\mu S$ .
- We may assume  $\frac{gm}{ID} = 14$  then  $ID = 100\mu A$ .
- $A2 = \frac{gm_4}{g_{ds4}+g_{ds5}} > 32$  then  $g_{ds4} < 39.784$ . We will choose  $g_{ds4} = 36\mu S$ .

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 100u ?

gm/ID 14 ?

gds 36u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
1 ID	100u
2 IG	0
3 L	340n
4 W	47.73u
5 VGS	632.3m
6 VDS	600m
7 VSB	0
8 gm/ID	13.29
9 Vstar	150.5m

Y-Expr gm/ID\*FT ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 100u ?

gm/ID 14 ?

gds 36u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
10 ft	2.878G
11 gm/gds	32.77
12 VA	2.467
13 ID/W	2.095
14 gm/W	27.83
15 AREA	16.23p
16 gm	1.329m
17 gmb	312.5u
18 gds	40.54u

Y-Expr gm/ID\*FT ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 100u ?

gm/ID 14 ?

gds 36u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
19 ro	24.67k
20 Ron	6k
21 VTH	504.7m
22 VDSAT	135m
23 cgg	73.48f
24 cdd	31.42f
25 csg	44.17f
26 cdg	18.09f
27 cgd	17.7f

Y-Expr gm/ID\*FT ?

Plot

- We will put  $V_{GS} = 632.2mV$  and we know  $I_D = 25\mu A$  and we assumed  $g_{ds} = g_{ds1,2} = 2.22\mu S$ .

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 25u ?

VGS 632.3m ?

gds 2.22u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
1 ID	24.85u
2 IG	0
3 L	720n
4 W	124.6u
5 VGS	632.3m
6 VDS	600m
7 VSB	0
8 gm/ID	17.98
9 Vstar	111.3m

Y-Expr gm/ID\*ft ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 25u ?

VGS 632.3m ?

gds 2.22u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
10 ft	223.8MEG
11 gm/gds	202.5
12 VA	11.27
13 ID/W	199.4m
14 gm/W	3.585
15 AREA	89.7p
16 gm	446.6u
17 gmb	147u
18 gds	2.205u

Y-Expr gm/ID\*ft ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

ID 25u ?

VGS 632.3m ?

gds 2.22u ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
19 ro	453.5k
20 Ron	24.15k
21 VTH	611m
22 VDSAT	78.8m
23 cgg	317.6f
24 cdd	83.86f
25 csg	180.8f
26 cdg	48.23f
27 cgd	47.98f

Y-Expr gm/ID\*ft ?

Plot

- $R_z = \frac{1}{g_{m4}} = \frac{1}{1.329 \times 10^{-3}} = 752.44$ .
- Switch design  $X_c = \frac{1}{2\pi \cdot f \cdot C} = 31830.988$  at max frequency we want at least ron less than 100 order then  $ron = 300$  and  $V_{GS} = V_{DD}$  and minimum L.

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

Ron 300 ?

VGS 2 ?

L min ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
1 ID	2.001m
2 IG	0
3 L	280n
4 W	5.78u
5 VGS	2
6 VDS	600m
7 VSB	0
8 gm/ID	616.4m
9 Vstar	3.245

Y-Expr gm/ID\*ft ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

Ron 300 ?

VGS 2 ?

L min ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

Results:

Name	TT-25.0
10 ft	19.64G
11 gm/gds	750.1m
12 VA	1.217
13 ID/W	346.2
14 gm/W	213.4
15 AREA	1.618p
16 gm	1.234m
17 gmb	206.6u
18 gds	1.645m

Y-Expr gm/ID\*ft ?

Plot

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1B OK ?

LUT Settings

Ron 300 ?

VGS 2 ?

L min ?

VDS 0.6 ?

VSB 0 ?

Stack 1 ?

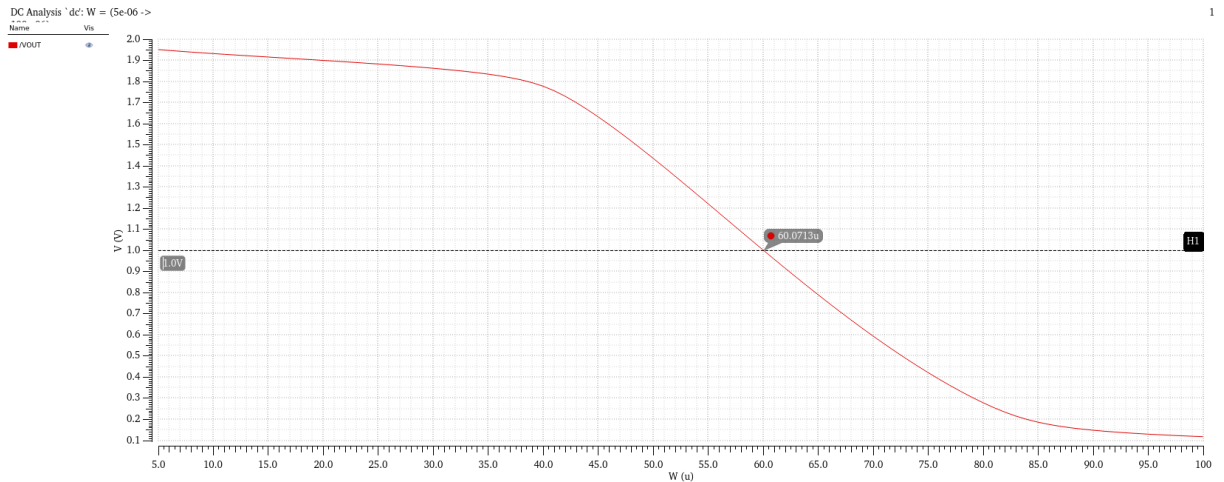
Results:

Name	TT-25.0
19 ro	608
20 Ron	299.8
21 VTH	500.3m
22 VDSAT	730.3m
23 cgg	9.999f
24 cdd	7.278f
25 csg	5.447f
26 cdg	4.098f
27 cgd	3.339f

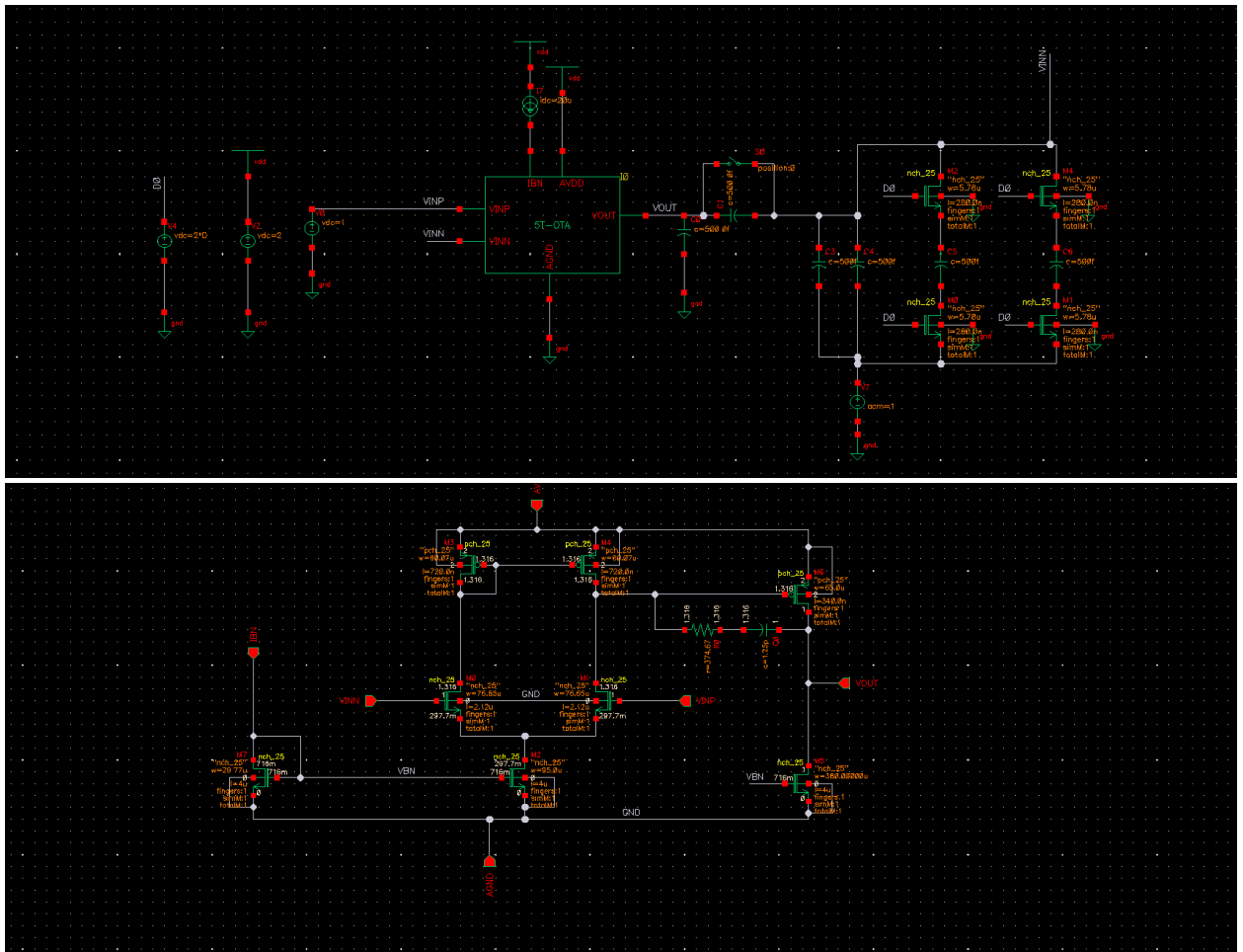
Y-Expr gm/ID\*ft ?

Plot

- We made sweep on CM width to cancel offset when we run open loop and set  $V_{out}=1$ .



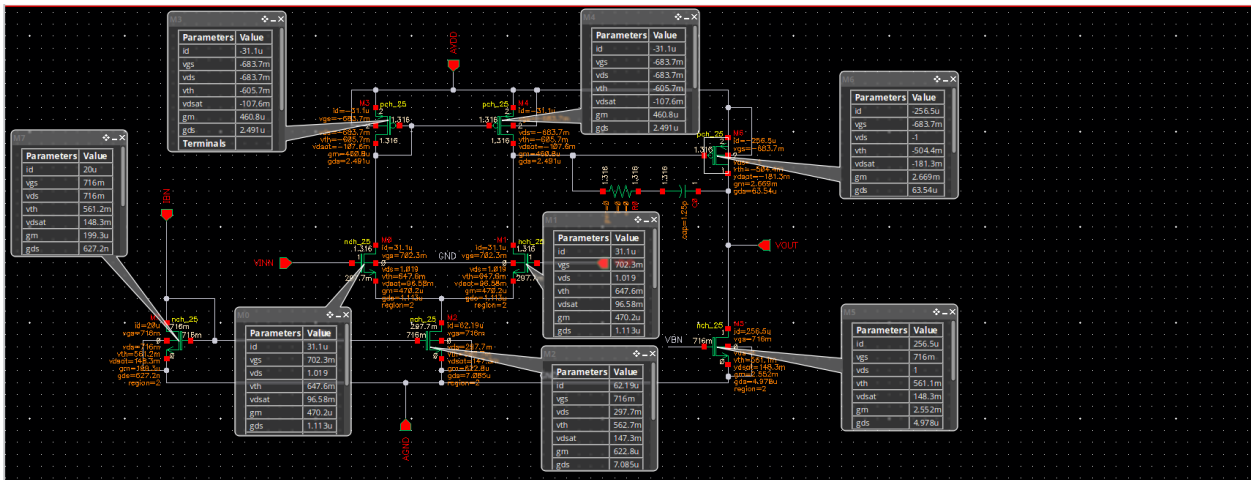
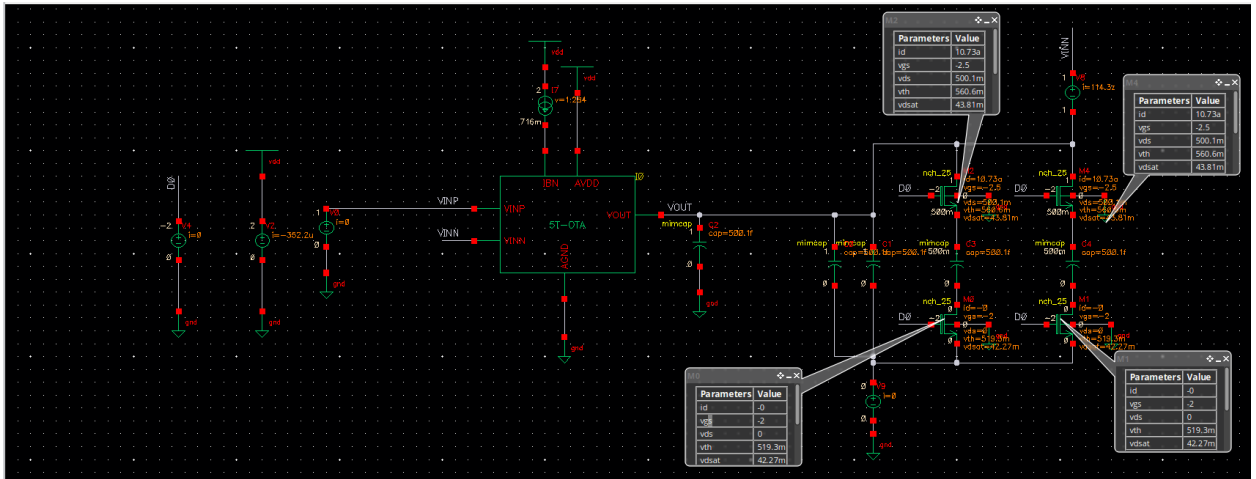
- Schematics with device sizing.



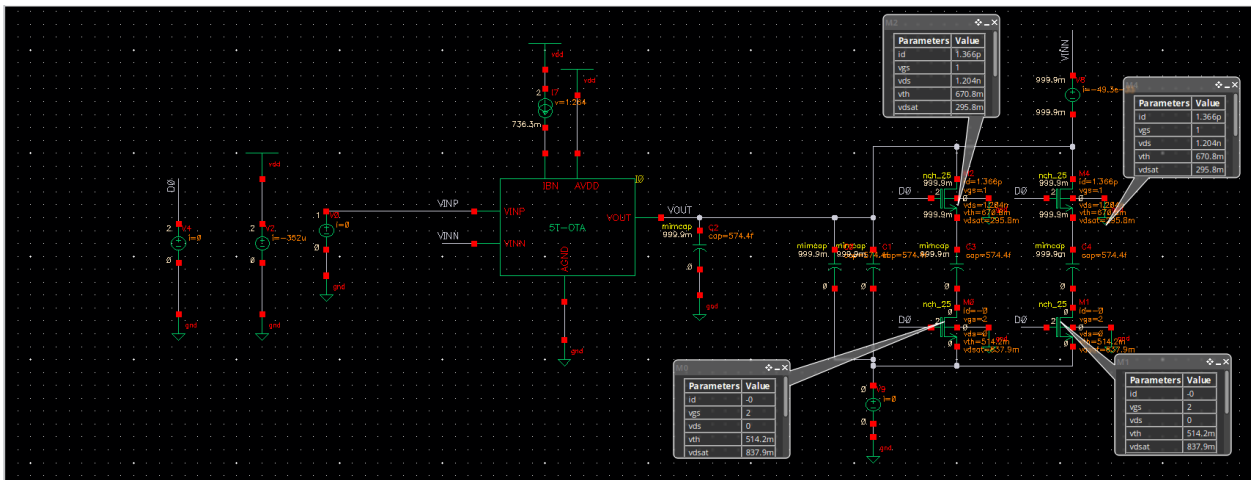
- **Note:** We put two switches to completely separate caps from the circuit and we increased the width of current sources and the second stage PMOS to satisfy the GBW and PM.

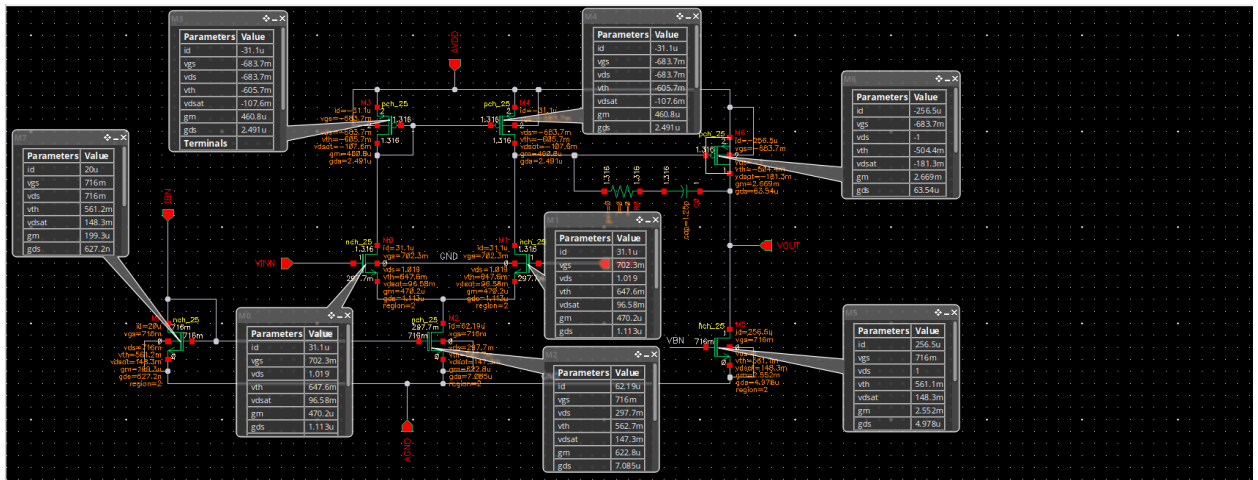
- Schematics with DC OP and node voltages annotated.

➤ For gain=2:



➤ For gain=4:





- Closed loop stb analysis results showing the amplifier closed loop specs (Closed loop gain and BW, DC LG, and PM) at the two different gain settings.

➤ Open loop:

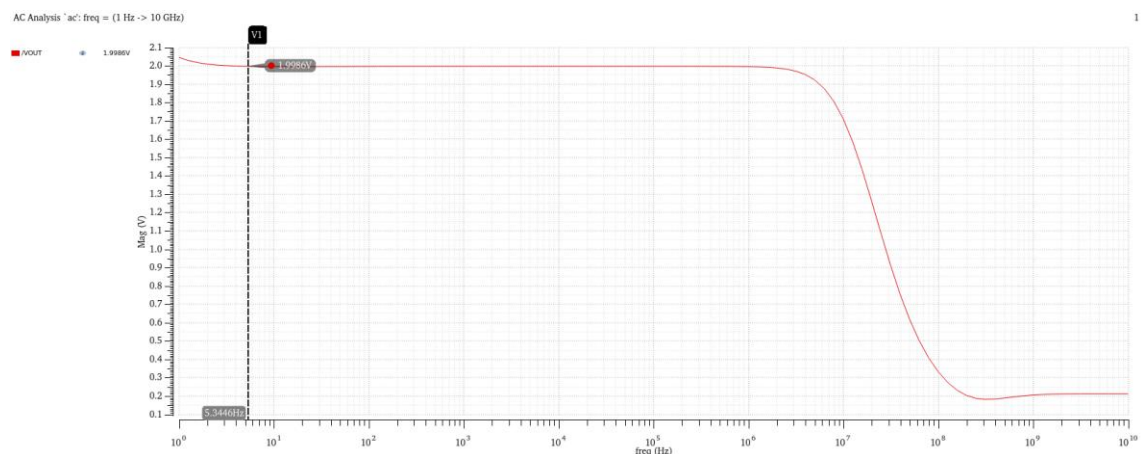
Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	y <sub>max</sub> (mag(VF"/VOUT"))	5.069k			
Design_Challenge:design1_TB:1	dB20(y <sub>max</sub> (mag(VF"/VOUT")))	74.1			
Design_Challenge:design1_TB:1	bandwidth(VF"/VOUT") 3 "low"	11.23k			
Design_Challenge:design1_TB:1	gainBwProd(VF"/VOUT")	57.04M			
Design_Challenge:design1_TB:1	unityGainFreq(VR"/VOUT")	55.74M			

Note: the open loop gain and GBW are satisfied.

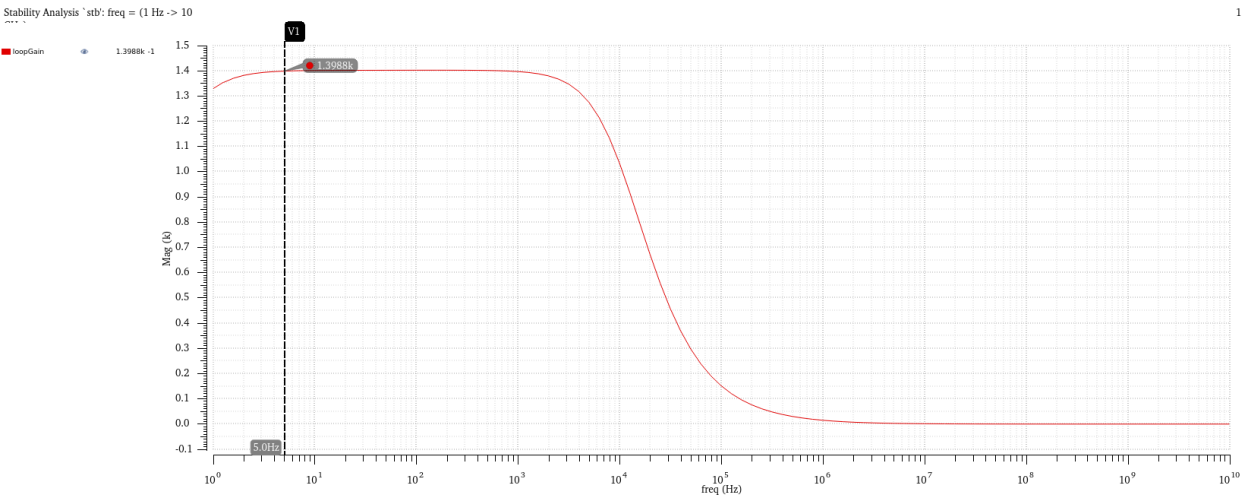
➤ Closed loop for A=2:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	y <sub>max</sub> (mag(VF"/VOUT"))	2.047			
Design_Challenge:design1_TB:1	dB20(y <sub>max</sub> (mag(VF"/VOUT")))	6.224			
Design_Challenge:design1_TB:1	bandwidth(VF"/VOUT") 3 "low"	15.55M			
Design_Challenge:design1_TB:1	gainBwProd(VF"/VOUT")	31.91M			
Design_Challenge:design1_TB:1	unityGainFreq(VR"/VOUT")	28.38M			

Closed loop gain:



DC LG:



PM at the feedback capacitor:

Design\_Challenge:design1\_TB:1 | Phase Margin | 84.52 |

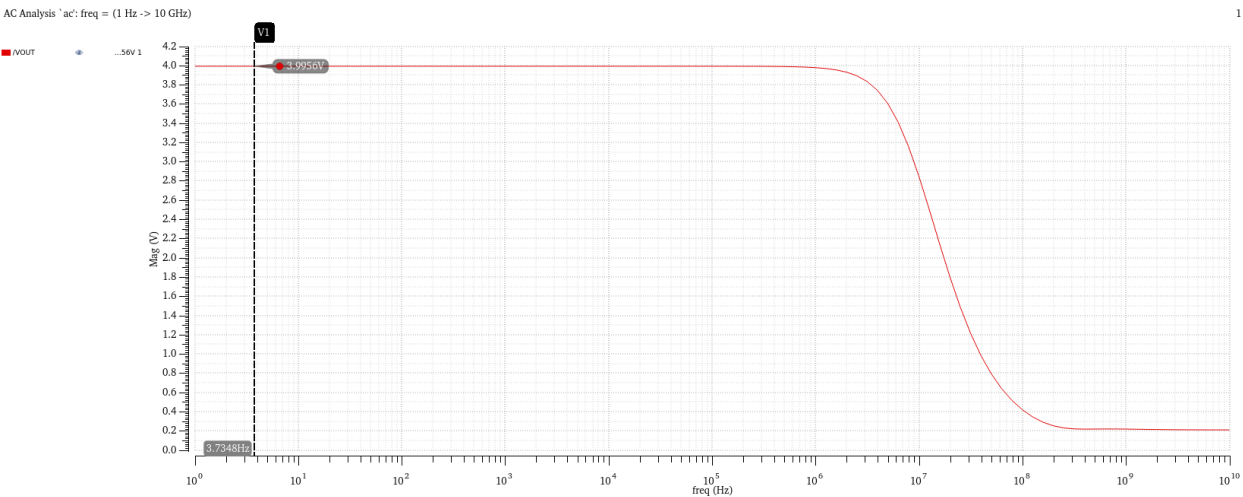
PM at unity gain buffer connection:

Design_Challenge:design1_TB:1	Phase Margin	65.41			
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➤ Closed loop for A=4:

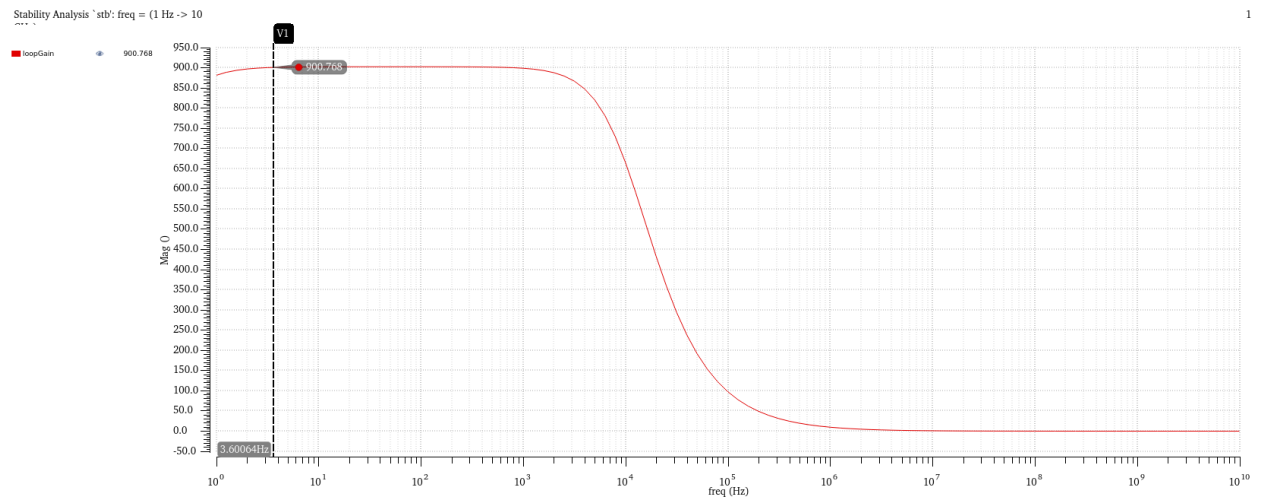
Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	y <sub>max</sub> (mag(VF"/VOUT"))	3.996			
Design_Challenge:design1_TB:1	dB20(y <sub>max</sub> (mag(VF"/VOUT")))	12.03			
Design_Challenge:design1_TB:1	bandwidth(VF"/VOUT") 3 "low"	10.5M			
Design_Challenge:design1_TB:1	gainBwProd(VF"/VOUT")	42.05M			
Design_Challenge:design1_TB:1	unityGainFreq(VR"/VOUT")	40.65M			

Closed loop gain:





## DC LG:



PM at the feedback capacitor:

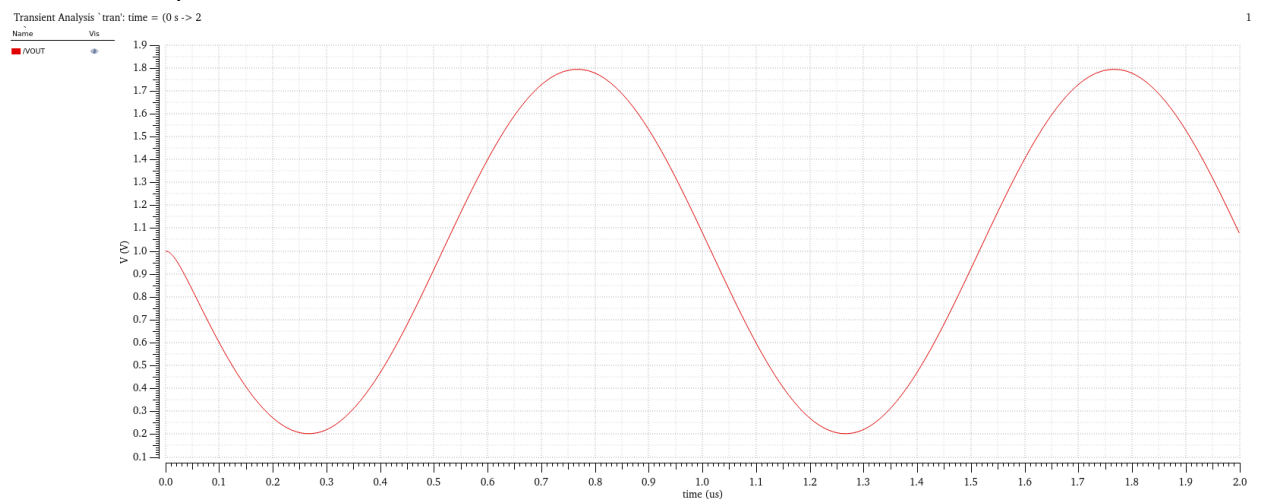
Design_Challenge:design1_TB:1	Phase Margin	86.66	
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PM at unity gain buffer connection:

Design_Challenge:design1_TB:1	Phase Margin	60.24			
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- Closed loop transient simulation results with sinusoidal input (1 MHz) at the nominal corner showing the maximum output swing at the two different gain settings.

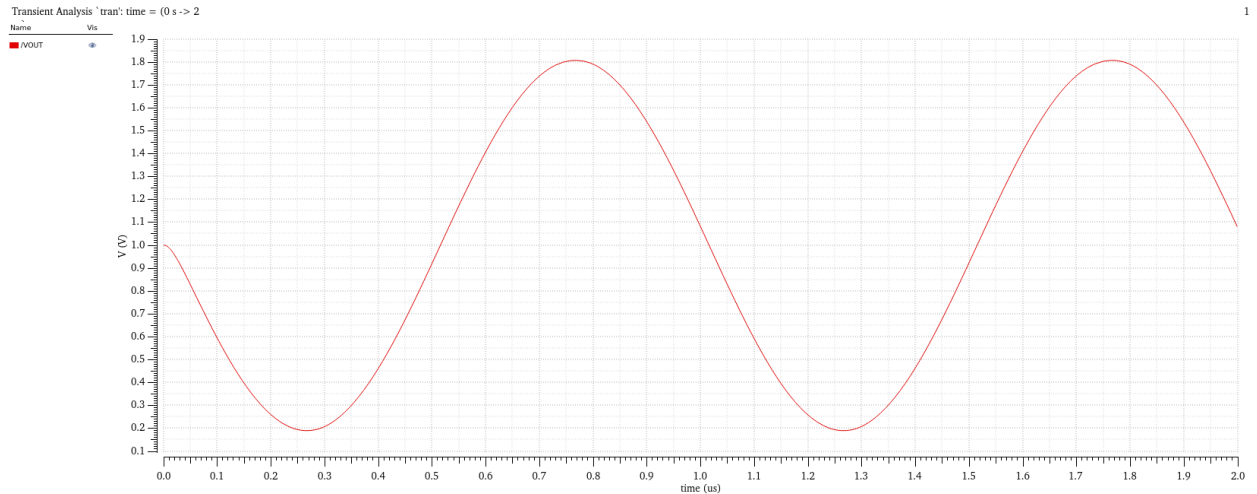
➤ Transient response at A=2:



Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(V"/VOUT" ?result"t...	1.623			

**Note:** We put input signal amplitude of 406.5mV to have this response. The signal has 180 degree shift as we use inverting topology. We notice that the swing spec is satisfied. And this is the max symmetrical swing as  $swing = 2 - 2 * V_{Dsat} = 1.638$  almost the same here.

➤ Transient response at A=4:



Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(V("VOUT" ?result "t...	1.618			

**Note:** We put input signal amplitude of 203.5mV to have this response. The signal has 180 degree shift as we use inverting topology. We notice that the swing spec is satisfied.

## PART 2:

- Use the THD function in the calculator to calculate the output distortion.

➤ For A=2:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(V("VOUT" ?result "t...	1.624			
Design_Challenge:design1_TB:1	thd(VT("VOUT") 1e-06 2e-06 51...	83.57m			

➤ For A=4:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(V("VOUT" ?result "t...	1.619			
Design_Challenge:design1_TB:1	thd(VT("VOUT") 1e-06 2e-06 51...	98.05m			

- Report the simulation results across corners

➤ A=2:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	y <sub>max</sub> (mag(VF("/VOUT")))	2.047				2.02	2.064	2.02	2.064
Design_Challenge:design1_TB:1	dB20(y <sub>max</sub> (mag(VF("/VOUT"))))	6.224				6.106	6.293	6.106	6.293
Design_Challenge:design1_TB:1	bandwidth(VF("/VOUT") 3 "low")	15.55M				12.25M	20.82M	12.25M	20.82M
Design_Challenge:design1_TB:1	gainBwProd(VF("/VOUT"))	31.91M				24.81M	43.09M	24.81M	43.09M
Design_Challenge:design1_TB:1	unityGainFreq(VR("/VOUT"))	28.38M				21.84M	38.21M	21.84M	38.21M
Design_Challenge:design1_TB:1	Phase Margin	84.52				83.2	85.64	85.64	83.2
Design_Challenge:design1_TB:1	y <sub>max</sub> (mag(getData("loopGain" ?...	1.403k				1.359k	1.454k	1.454k	1.359k

We notice that in FF corner at T=-40 the current increased so gm input pair increased and GBW and BW increased and the current in the second branch didn't increase with the same ratio so PM reduced and vice versa in SS at T=100 corner.

PM at unity gain connection:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	Phase Margin	65.45				59.92	69.76	69.76	59.92

➤ A=4:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	y <sub>max</sub> (mag(VF("/VOUT")))	3.995				3.995	3.995	3.995	3.995
Design_Challenge:design1_TB:1	dB20(y <sub>max</sub> (mag(VF("/VOUT"))))	12.03				12.03	12.03	12.03	12.03
Design_Challenge:design1_TB:1	bandwidth(VF("/VOUT") 3 "low")	10.18M				7.72M	14.07M	7.72M	14.07M
Design_Challenge:design1_TB:1	gainBwProd(VF("/VOUT"))	40.79M				30.92M	56.35M	30.92M	56.35M
Design_Challenge:design1_TB:1	unityGainFreq(VR("/VOUT"))	39.36M				30.24M	54.04M	30.24M	54.04M
Design_Challenge:design1_TB:1	Phase Margin	86.66				85.51	87.68	87.68	85.51
Design_Challenge:design1_TB:1	y <sub>max</sub> (mag(getData("loopGain" ?...	902.6				887.8	925.7	925.7	887.8

PM at unity gain connection:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	Phase Margin	60.63				55.19	64.96	64.96	55.19