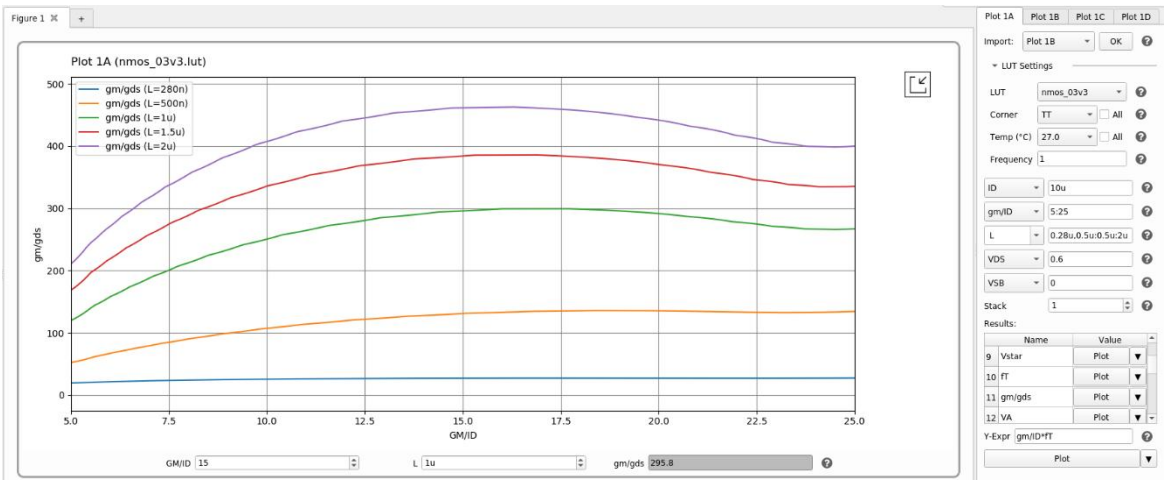
# Lab 09

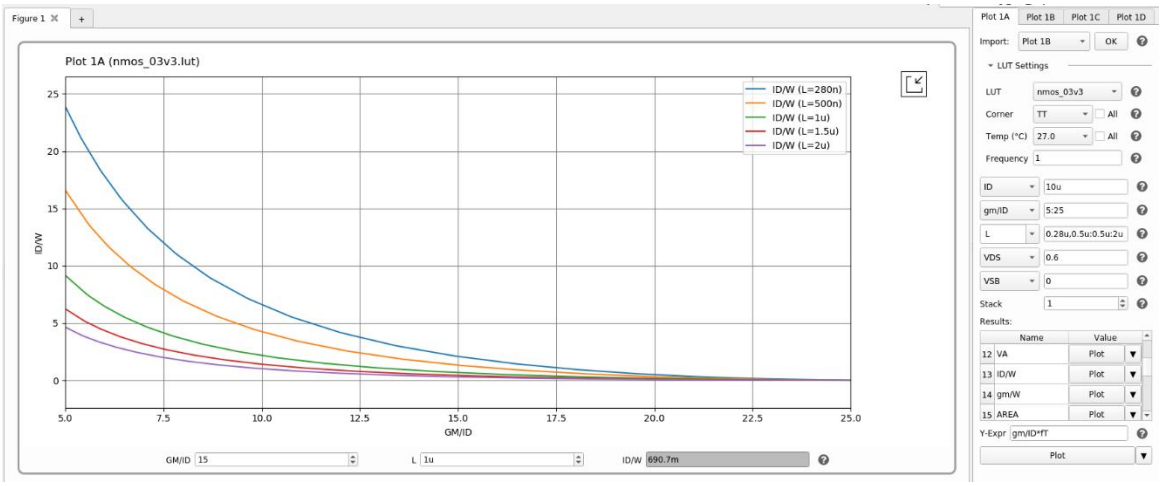
## PART 1: gm/ID Design Charts:

- NMOS:

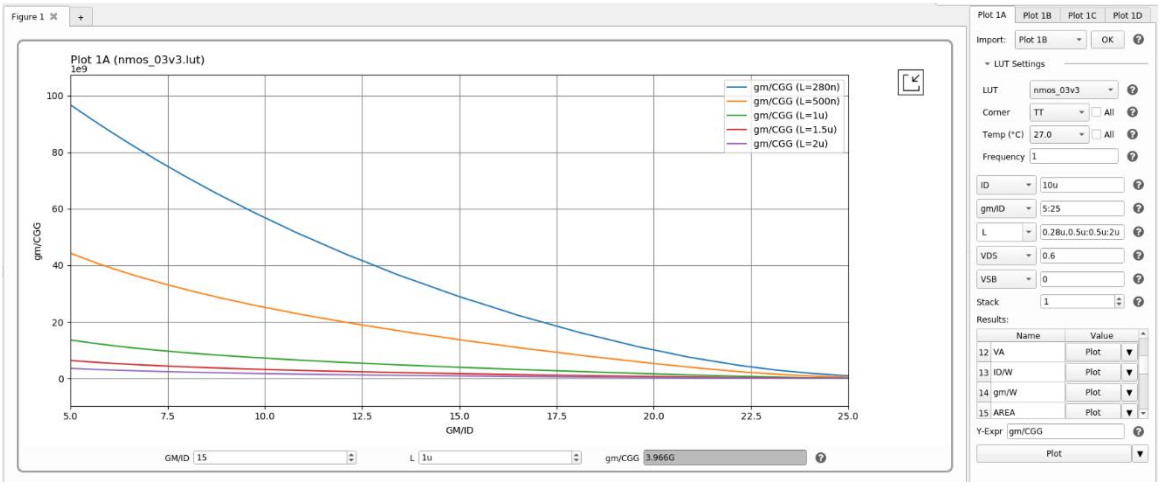
➢ gm/gds:



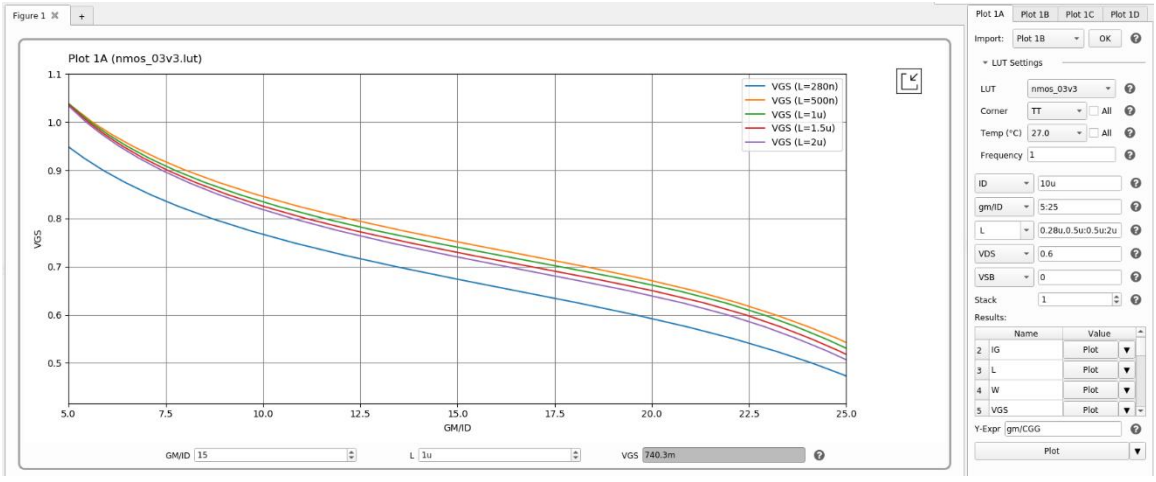

➢ ID/W:



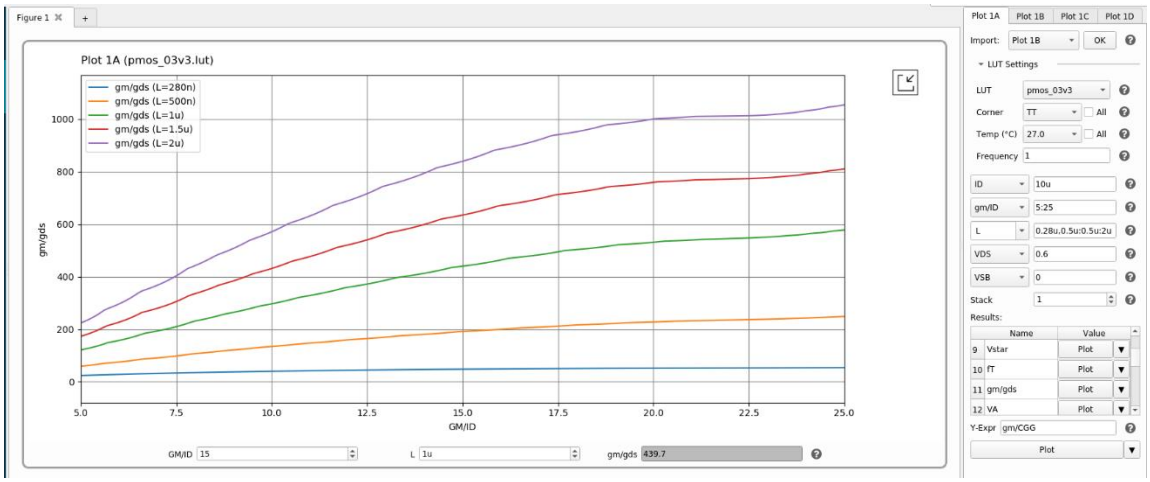
- gm/cgg:



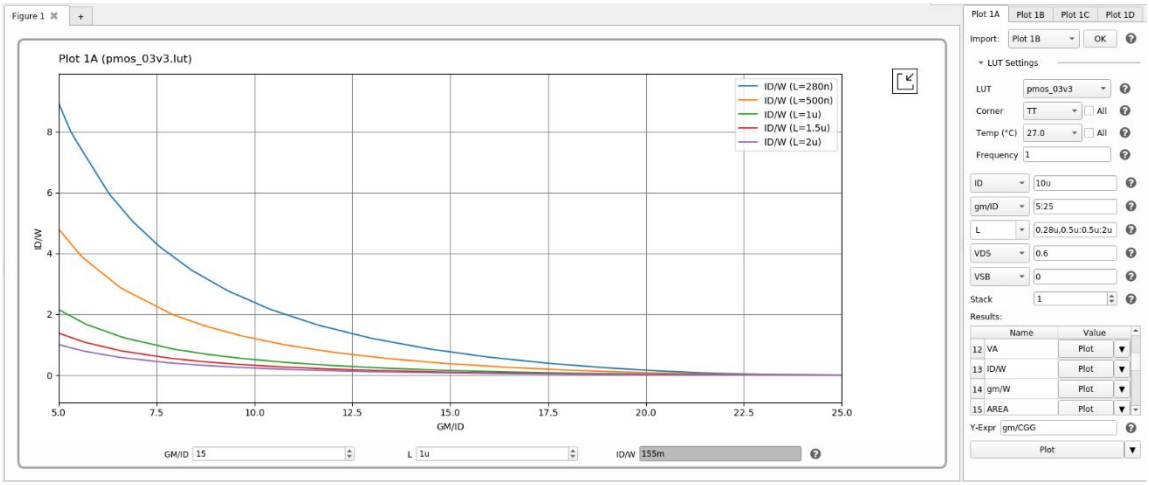

- VGS:



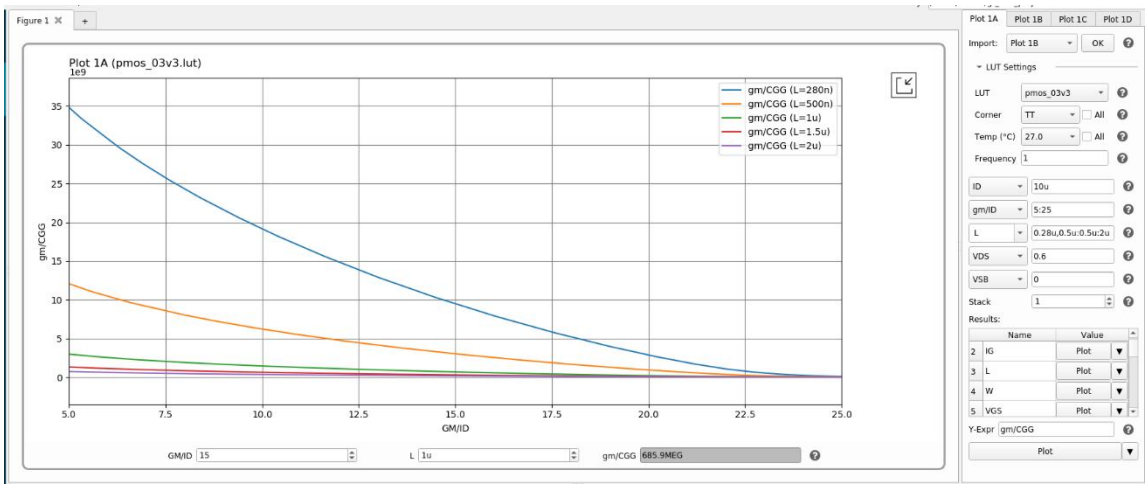

- PMOS:
- gm/gds:



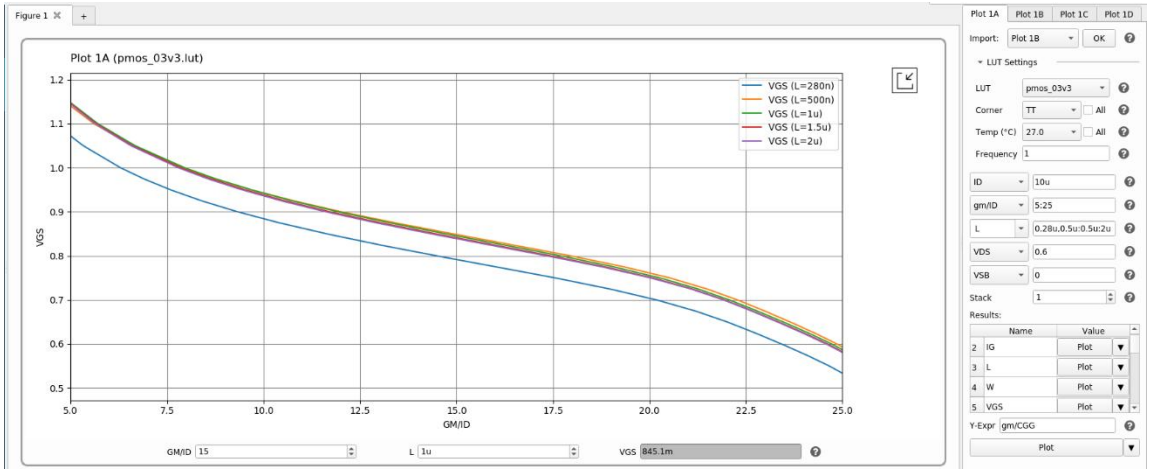
- ID/W:




- gm/cgg:




- VGS:



# PART 2: OTA Design:

- **Specs:**

| | Specs |
|---|---|
| Supply Voltage | $1.8V$ |
| Static gain error | $\leq 0.05\%$ |
| CMRR @ DC | $\geq 74dB$ |
| Phase margin | $\geq 70°$ |
| current consumption | $\leq 60\mu A$ |
| CMIR – high | $\geq 0.8V$ |
| CMIR – low | $\leq 0.2V$ |
| Output swing | $0.2: 1.6$ |
| Buffer closed loop rise time | $\leq 70nS$ |
| Slew rate | $5V/\mu s$ |

**Q) Detailed design procedure and hand analysis. Justify why you used NMOS or PMOS input pair for each stage.**

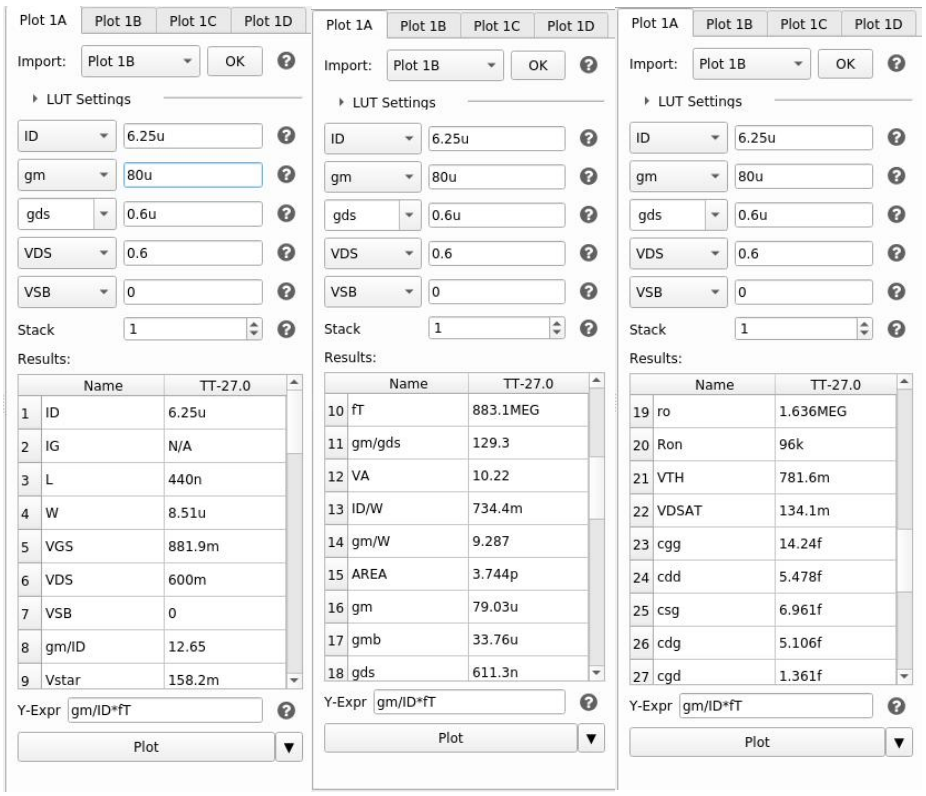
## Design Procedure:

We chose the Miller two stage OTA as We will need high gain of 66dB which we can't achieve by one stage and we need high output swing so we can't use telescopic or folded cascode. We will choose the input pair to be PMOS as the input is closer to ground.

1. Input pair design (M1 &M2):

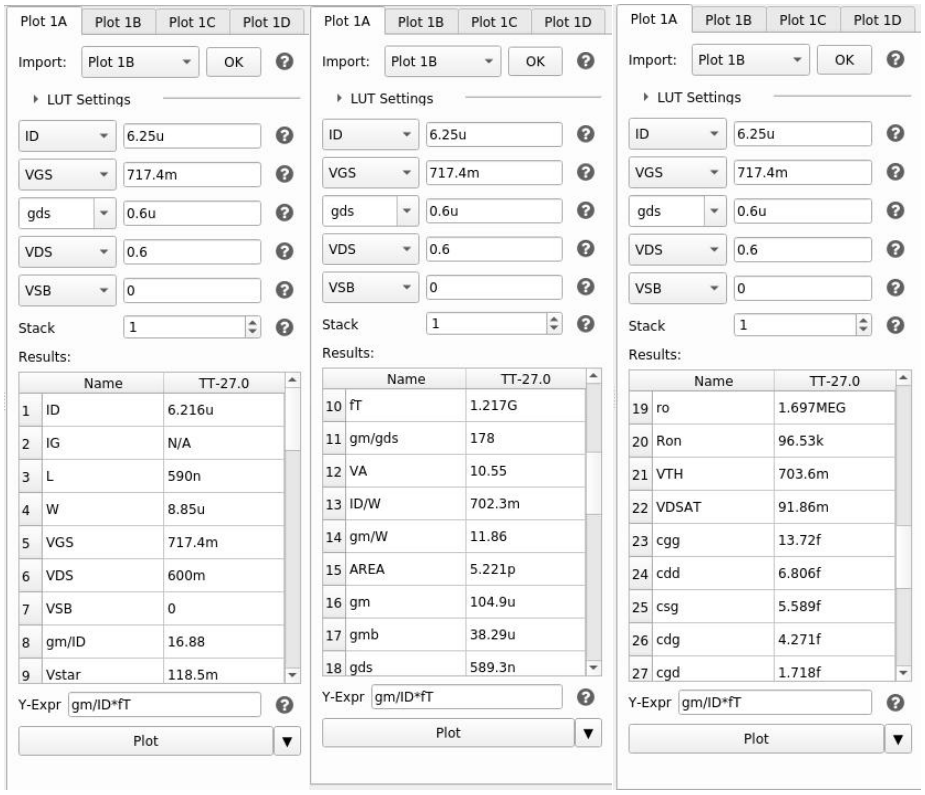
- We want $Trise \leq 70nS$ then $\tau = \frac{Trise}{2.2}$ $so\ \tau \leq 31.82nS$. We know that $\tau = \frac{1}{2\pi\omega cl}$ and this is a buffer connection so $ACL = 1$ so $\omega cl = \omega u$ so We get $\omega u \geq 5MHz$.
- Then $\frac{gm1,2}{2\pi Cc} \geq 5MHz$. We will assume that $Cc = 0.5CL = 2.5pF$ then $gm1,2 \geq 78.54\mu S$. We will choose $gm1,2 = 80\mu S$.

- We need $\varepsilon_s \leq 0.05\%$ and $\varepsilon_s = \frac{1}{\beta Aol}$ and $\beta = 1$ so $Aol \geq 2000$ which is 66dB. We will distribute the gain to be 36dB in the first stage and 30dB for the second stage as the first stage is an OTA which give higher gain and the first stage improves the CMRR.
- We will assume the Current mirror load and input pair to have the same gds then $A_{OTA} = \frac{gm1,2}{2gds} = 63.1$ then $gds = 0.6339\mu S$ We will choose $gds = 0.6\mu S$ which even gives higher gain to the first stage which will approximately equal 66.67.
- From the slew rate condition $SR = \frac{ISS1}{Cc} = 5$ then $Iss1 = 12.5\mu A$ and $ID = 6.25\mu A$. then We get $\frac{gm}{ID} = 12.8$.



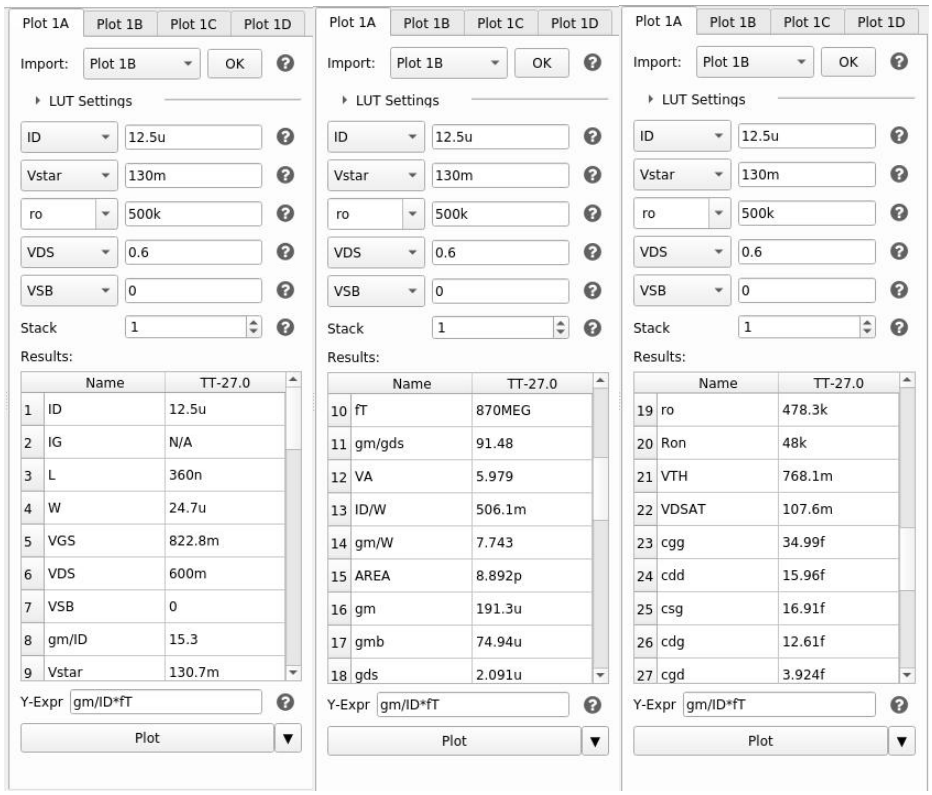

2. Current Mirror load (M3 & M4):

- We got from the first part $ID = 6.25\mu A$ and $gds3,4 = 0.6\ \mu S$.
- From the CMIR-Low condition: $V_{incm} =- |VGS1,2| + |Vdsat1,2| + VGS3,4 \leq 0.2$ $VGS3,4 \leq 0.9478$ We will Choose $VGS3,4 = 717.4mV$ which is the VGS we got to the NMOS of the second stage to try eliminate the offset.
- Then We can calculate gm/ID for current mirror load to be 16.88



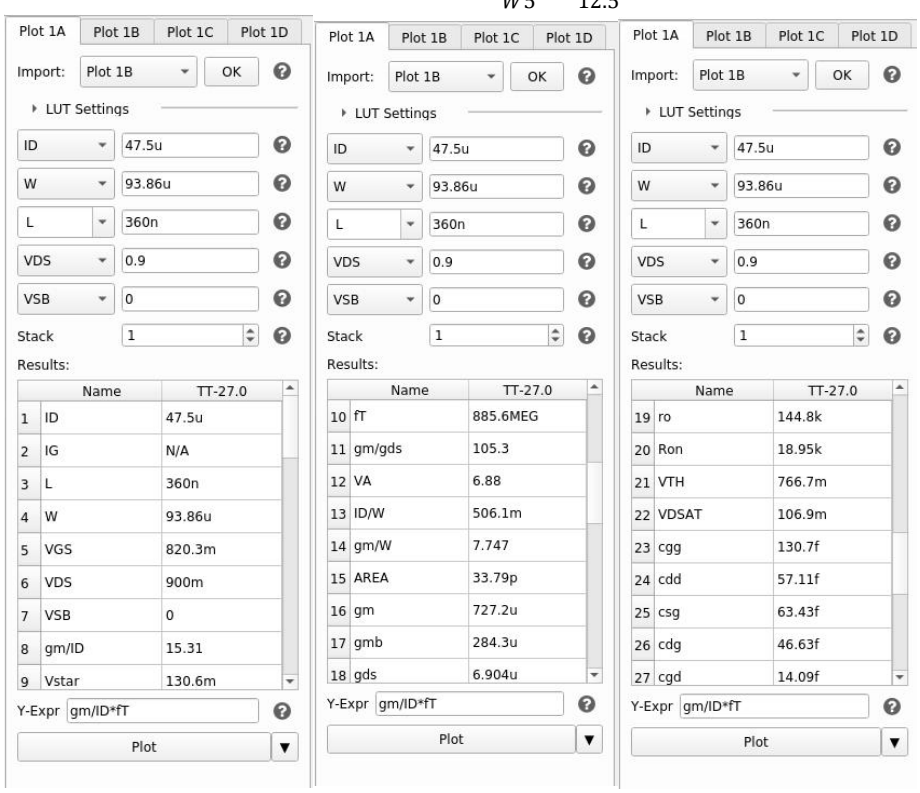

3. Tail current source (M5):

- We got the Bias current $ISS1 = 12.5\mu A$ which is ID for this transistor.
- $CMRR = Adiff - Acm \leq 74dB$ then $Acm \leq -38dB$ which is equivalent to 0.012589 so $\frac{1}{2gm3,4*ro5} \leq 0.012589$ then $ro5 \geq 378619\Omega$ We will choose $ro5 = 500K\Omega$ to reduce dependence on VDS.
- Now, we will use the CMIR-high condition to get $V^*$
  $Vcm = -|VGS1,2| - |Vdsat5| + VDD \leq 0.8$ then $|Vdsat5| \leq 0.1181V$
  We will choose $V^* = 130mV$ and make sure that the Vdsat condition is achieved.



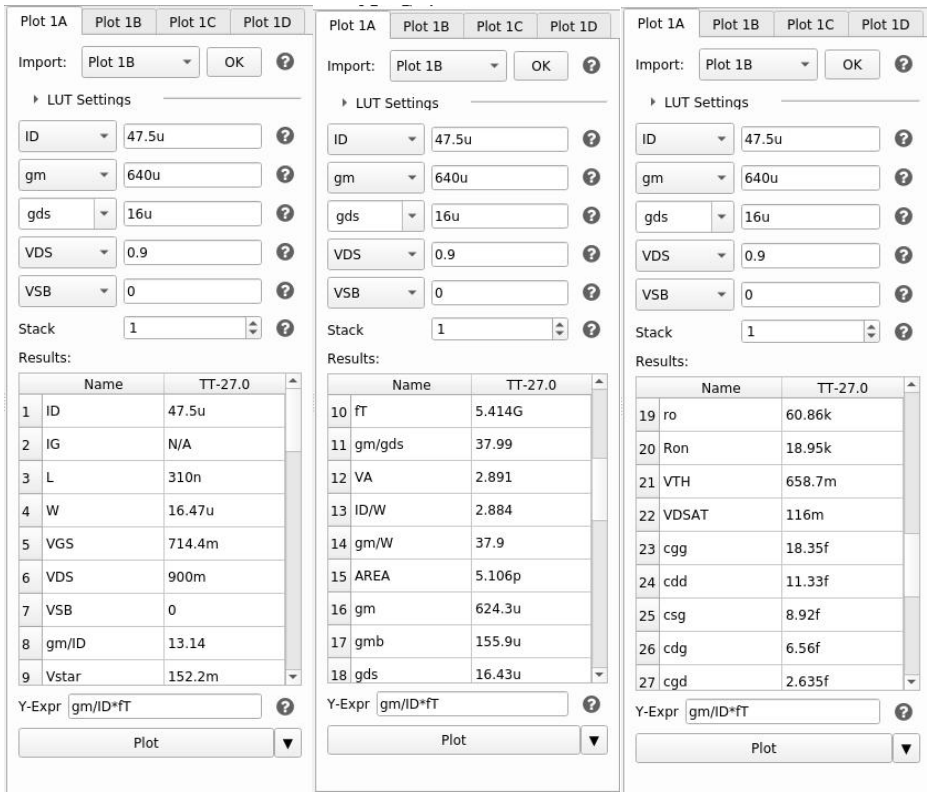

4. Mirroring transistors M7:

- From current consumption We get $Iss2 = 47.5\mu A$ and for matching we will choose $L7 = L5 = 360nm$. From mirror ratio $\frac{W7}{W5} = \frac{47.5}{12.5}$ $then\ W7 = 93.86\mu m$.



5. Second stage common source NMOS amplifier (M6):

- We got $Iss2 = 47.5\mu A$.
- To achieve the phase margin condition, we need $\omega p2 > 4\omega u$ then $\frac{gm6}{2\pi Cl} \geq \frac{gn1,2}{2\pi Cc}$ then $gm6 \geq 8gm1,2$ so $gm6 \geq 640\mu S$ and we will choose it to equal $640\mu S$.
- To achieve the gain spec we need $A2 \geq 26.667\ so \frac{gm6}{gds6+gds7} \geq 26.667$ so $gds \leq 20.09566\mu S$ we will choose it to equal 16 $\mu S$




6. Mirror device (M8):

- Finally, the mirror device will have $L8 = L5 = 360nm$ and it has $ID = 10\mu A$ so it will has $W8 = 19.76\mu m$.

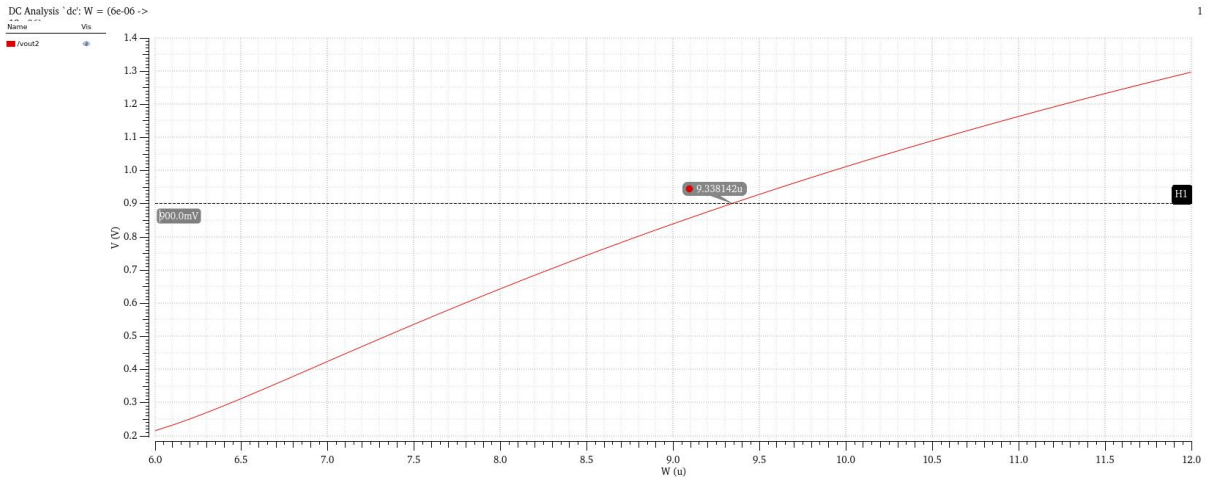
7. Choosing RZ:

$Rz = \frac{1}{gm6} = \frac{1}{640*10^{-6}} = 1562\Omega$.

8. Verify that your gm/ID choices do not violate the CMIR and the peak-to-peak output swing:

$CMIR_{low} =- |VGS1,2| + |Vdsat1,2| + VGS3,4 =- 0.033 < 0.2\ (achieved)$
$CMIR_{high} =- |VGS1,2| - |Vdsat5| + VDD = 0.8105 > 0.8\ (achieved)$
$output\ swing_{low} = Vdsat6 = 0.116 < 0.2\ (achieved)$
$output\ swing_{high} = VDD - Vdsat7 = 1.6931 > 1.6\ (achieved)$

9. In order to eliminate systematic offset between M6 and M3&4, We will sweep W of M3,4 and get the point at which $vout = 0.9V$. We got $W = 9.33\mu m$.




**Q) A table showing W, L, $gm$,$ID$, $gm/ID$, $vdsat$, $Vov$ = $VGS - VTH$, and $V* =$ $2ID/gm$ of all transistors (as calculated from gm/ID curves).**

| | M1,2 | M3,4 | M5 | M6 | M7 | M8 |
|---|---|---|---|---|---|---|
| W | $8.51\mu m$ | $8.85\mu m$ | $24.7\mu m$ | $16.47\mu m$ | $93.86\mu m$ | $19.76\mu m$ |
| L | $440nm$ | $590nm$ | $360nm$ | $310nm$ | $360nm$ | $360nm$ |
| gm | $79.03\mu S$ | $104.9\mu S$ | $191.3\mu S$ | $624.3\mu S$ | $727.2\mu S$ | $153.04\mu S$ |
| ID | $6.25\mu A$ | $6.216\mu A$ | $12.5\mu A$ | $47.5\mu A$ | $47.5\mu A$ | $10\mu A$ |
| gm/ID | 12.65 | 16.88 | 15.3 | 13.14 | 15.31 | 15.3 |
| Vdsat | $134.1mV$ | $91.86mV$ | $107.6mV$ | $116mV$ | $106.9mV$ | $107.6mV$ |
| Vov | $100.3mV$ | $13.8mV$ | $54.7mV$ | $55.7mV$ | $53.6mV$ | $54.7mV$ |
| $\boldsymbol{V}^*$ | $158.2mV$ | $118.5mV$ | $130.7mV$ | $152.2mV$ | $130.6mV$ | $130.7mV$ |

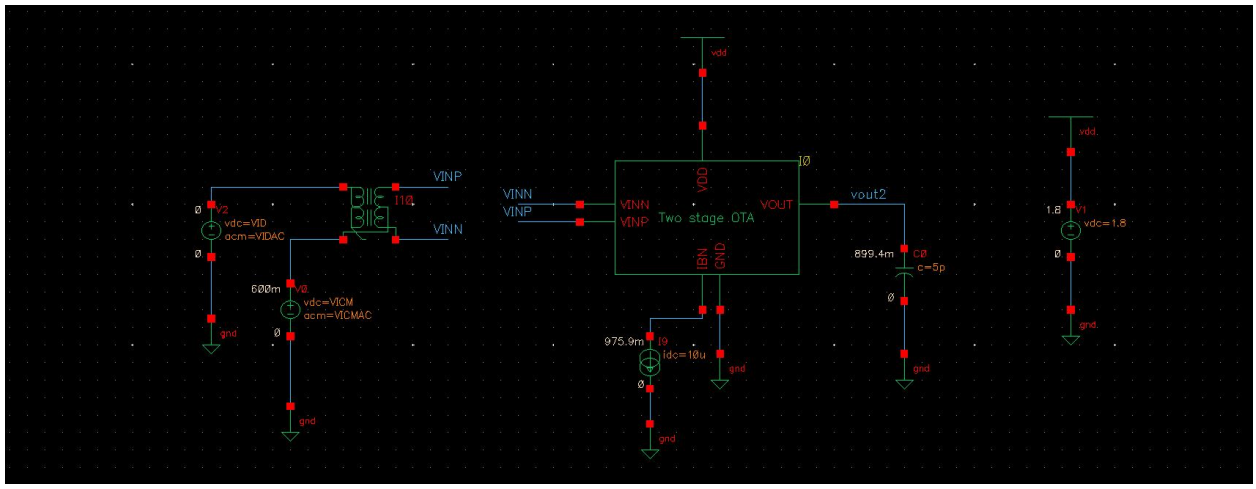
**Note:**

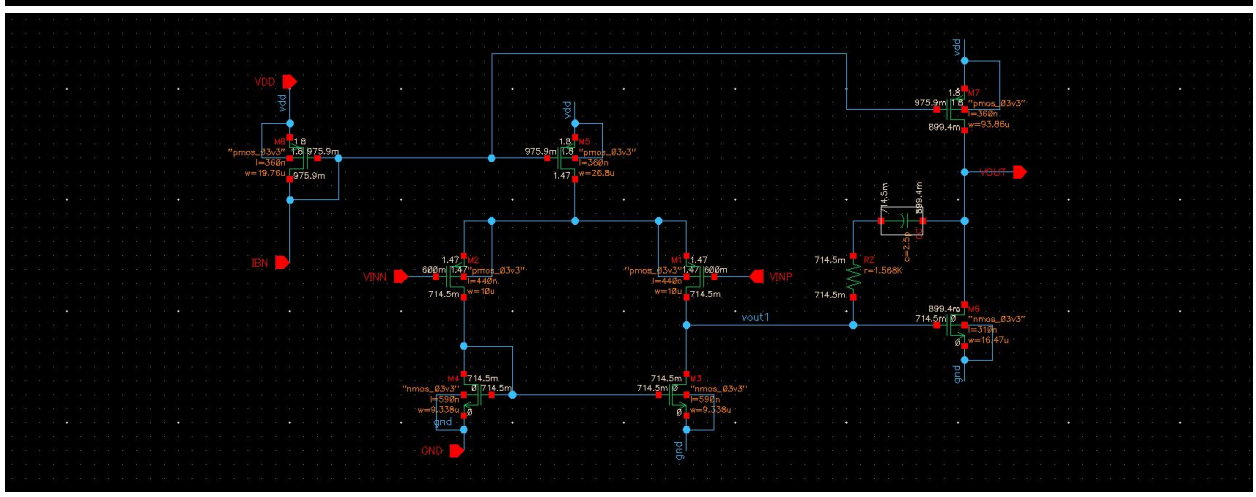
The values in the table are the values from sizing assistant there may be slight error like in ID of M3,4 or gm6 but in actual simulation they will be more accurate.

Also, W3,4 changed to get to set $Vout_{DC} = 0.9V$.

# PART 3: Open-Loop OTA Simulation:

1) **Schematic of the OTA and bias circuit with DC node voltages clearly annotated.**




**Note:**

- We increased W5 to increase the current as $VDS5 < VDS8$ so the mirroring wasn't accurate and the current was less than 12.5$\mu A$.
- We increase W1,2 to improve gm by increasing gm/ID to achieve GBW condition.

**Q) Is the current (and gm) in the input pair exactly equal?**

| | Name | Value |
|---|---|---|
| 1 | I0.M1.m0:id | -6.233E-6 |
| 2 | I0.M1.m0:gm | 84.71E-6 |
| 3 | I0.M2.m0:id | -6.233E-6 |
| 4 | I0.M2.m0:gm | 84.71E-6 |

The current and gm are exactly equal as they have the same bias and sizing.

**Q) What is DC voltage at the output of the first stage? Why?**

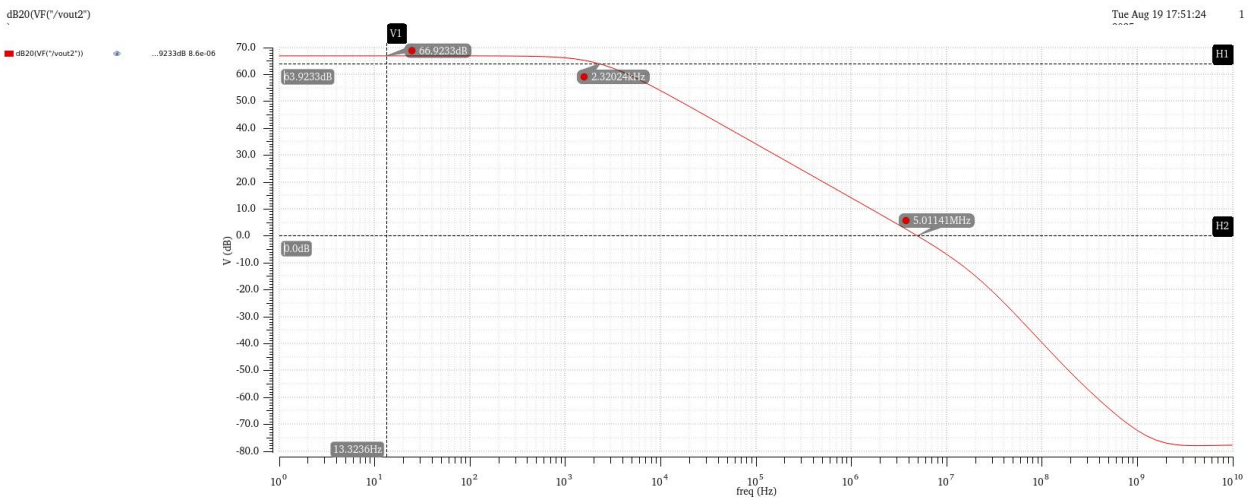
$vout1 = 714.5mV$ as in open loop the Vout1 node will follow the mirror node and the mirror node here is the VGS3,4 of the current mirror load which we designed it to take this value.

**Q) What is DC voltage at the output of the second stage? Why?**

$Vout2 = 899.4mV \approx 900mV$ and that's because we swept W3,4 to get Vout=900mV and we chose this value as it is approximately in the middle of the output swing so that we can benefit from all the output swing.

**2) Diff small signal ccs:**

**Q) Plot diff gain (in dB) vs frequency**




**Q) Compare simulation results with hand calculations in a table**

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| ITI_labs:Lab_09_TB:1 | Ao | 2.219k | | | |
| ITI_labs:Lab_09_TB:1 | Ao_dB | 66.92 | | | |
| ITI_labs:Lab_09_TB:1 | BW | 2.327k | | | |
| ITI_labs:Lab_09_TB:1 | fu | 5.011M | | | |
| ITI_labs:Lab_09_TB:1 | GBW | 5.163M | | | |
| ITI_labs:Lab_09_TB:1 | Ao_first_stage | 78.89 | | | |
| ITI_labs:Lab_09_TB:1 | dB20(VF("/vout2")) | | | | |

$$A1 = \frac{gm1,2}{gds1,2+gds3,4} = 78.97 = 37.95dB \text{ , } A2 = \frac{gm6}{gds6+gds7} = 28.127 = 28.98dB$$

$$A = A1 + A2 = 37.95 + 28.98 = 66.932dB = 2221$$

$$BW = \frac{1}{2\pi Cc*\left(1+\frac{gm6}{gds6+gds7}\right)*\frac{1}{gds1,2+gds3,4}} = 2346Hz$$

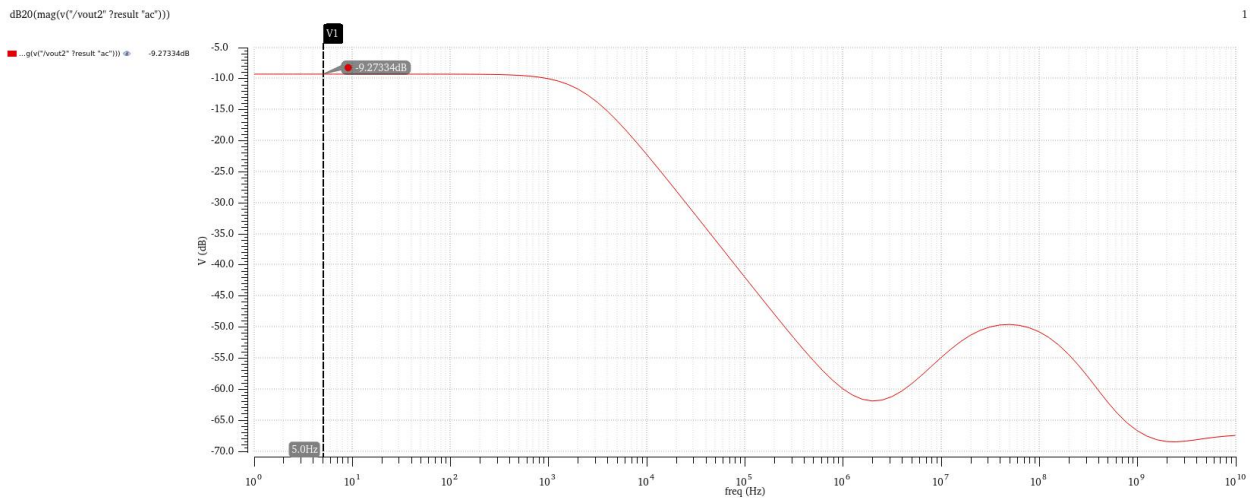
$$GBW = A * BW = 5.21MHz$$

| | I0.M1.m0:gm | I0.M1.m0:gds | I0.M3.m0:gds | I0.M6.m0:gm | I0.M6.m0:gds | I0.M7.m0:gds |
|---|---|---|---|---|---|---|
| 1 | 84.72E-6 | 535.7E-9 | 537.7E-9 | 637.5E-6 | 15.89E-6 | 6.775E-6 |

| | Hand analysis | Simulation |
|---|---|---|
| Gain | 2221 | 2219 |
| BW | $2346Hz$ | $2327Hz$ |
| GBW | $5.21MHz$ | $5.16MHz$ |

**3) CM small signal ccs:**

**Q) Plot CM gain in dB vs frequency**




**Q) Compare simulation results with hand calculations in a table**

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| ITI_labs:Lab_09_TB:1 | Ao | 343.8m | | | |
| ITI_labs:Lab_09_TB:1 | Ao_dB | -9.273 | | | |
| ITI_labs:Lab_09_TB:1 | BW | 2.325k | | | |

$$A1 = \frac{gds5}{2gm3,4} = 0.01256 =- 38.02dB \text{ , } A2 = \frac{gm6}{gds6+gds7} = 28.127 = 28.98dB$$

$$A = A1 + A2 =- 38.02 + 28.98 =- 9.0395dB = 0.3532$$

$$BW = \frac{1}{2\pi Cc*\left(1+\frac{gm6}{gds6+gds7}\right)*\frac{1}{gds1,2+gds3,4}} = 2346Hz$$

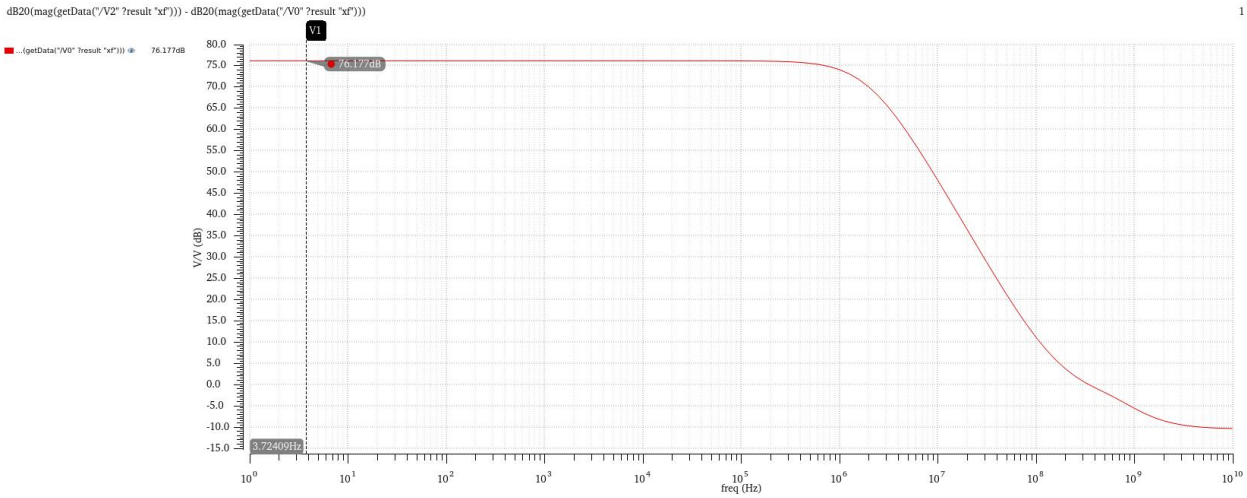
There is no UGF here and GBW is meaningless.

| | I0.M6.m0:gm | I0.M6.m0:gds | I0.M7.m0:gds | I0.M3.m0:gm | I0.M5.m0:gds |
|---|---|---|---|---|---|
| 1 | 637.5E-6 | 15.89E-6 | 6.775E-6 | 106.6E-6 | 2.678E-6 |

| | Hand analysis | Simulation |
|---|---|---|
| Gain | $353.2mV$ | $343.8mV$ |
| BW | $2346Hz$ | $2325Hz$ |

## 4) CMRR:

### Q) Plot CMRR in dB vs frequency



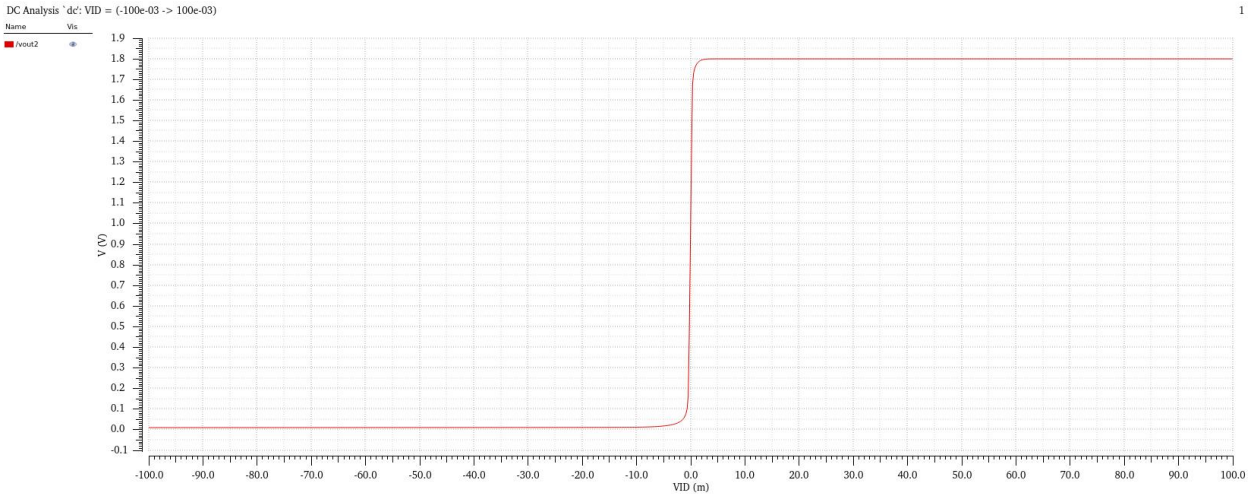

### Q) Compare simulation results with hand calculations in a table

$CMRR = Adiff - Acm = 37.95 - (-38.02) = 76.15dB$

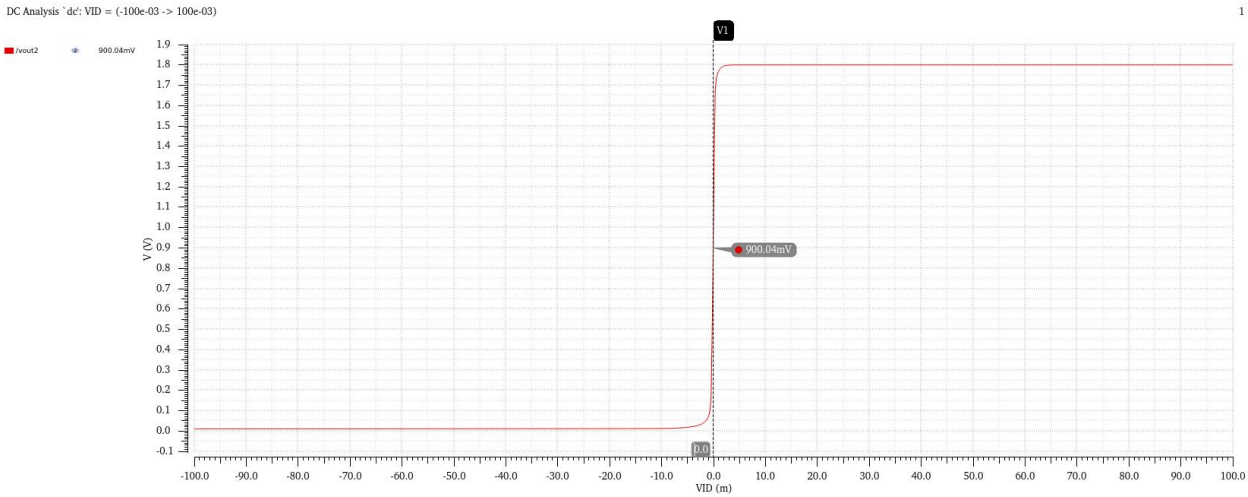
| | Hand analysis | Simulation |
|---|---|---|
| CMRR | $76.15dB$ | $76.177dB$ |

## 5) Diff large signal ccs:

### Q) Plot VOUT vs VID

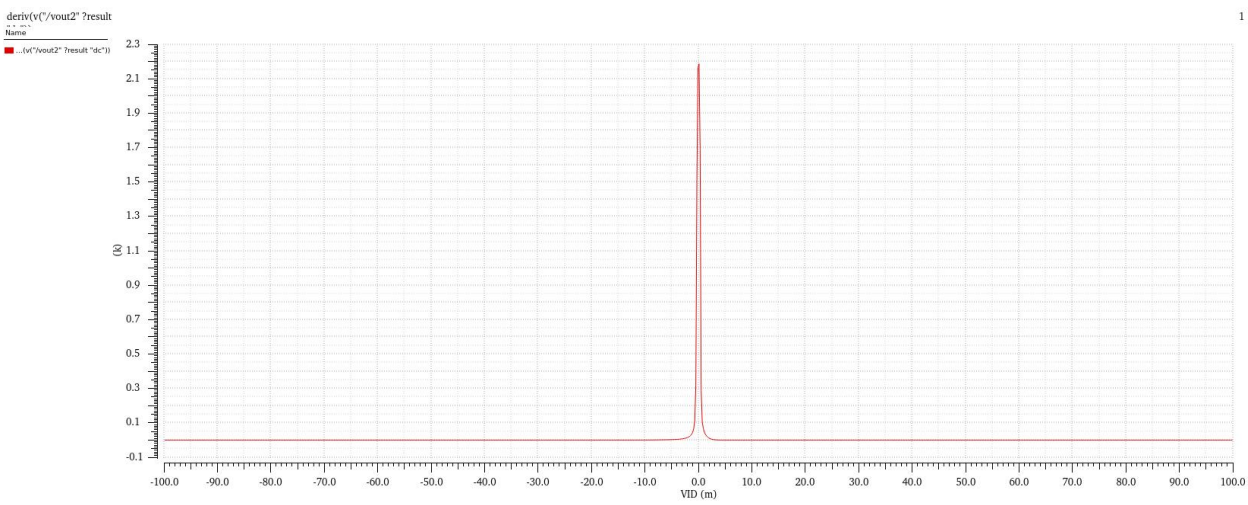


**Q) From the plot, what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP**




Vout at VID = 0 equals 900.04mV which approximately equals Vout at DCOP (899.4mV) as at VID=0 this is common mode bias which is the DCOP at which we use the OTA as an amplifier.

**Q) Plot the derivative of VOUT vs VID. Is the peak less than the value of Avd obtained from ac analysis? Why?**

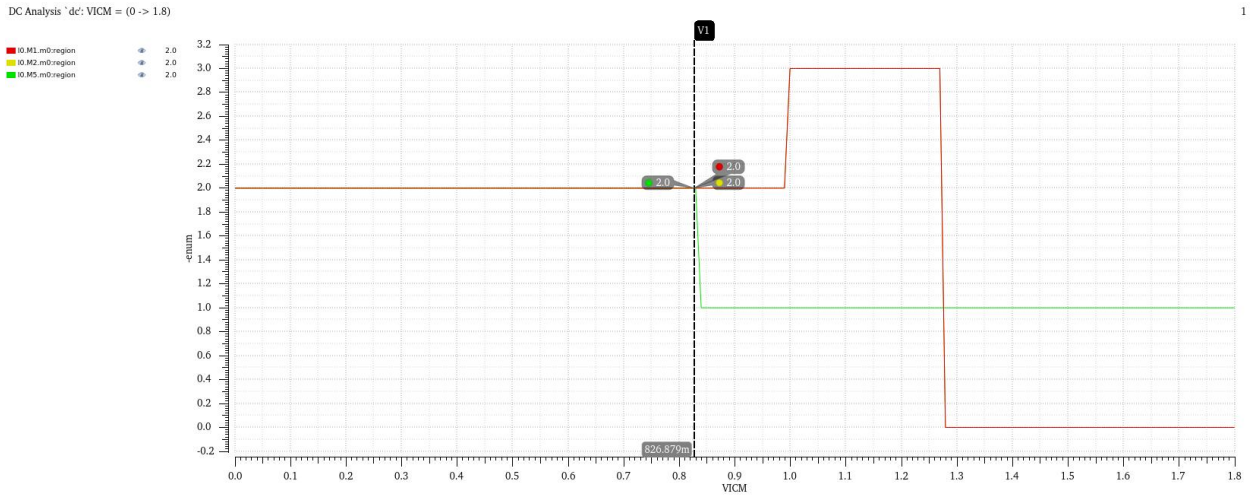



| | Expression | Value |
|---|---|---|
| 1 | ymax(deriv(v("/vout2" ?result "dc"))) | 2.186E3 |

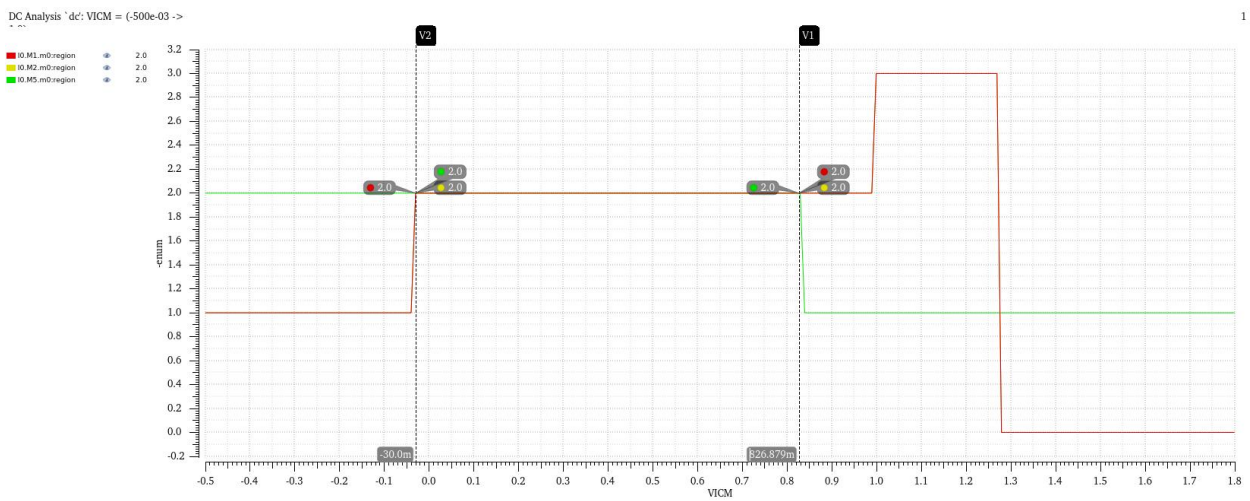
Yes, The peak is 2186 which is less than the actual gain from ac analysis as we use a large step compared to the very narrow region of gain not that we used step= $0.2mV$ instead of $1mV$ to increase the accuracy.

## 6) CM large signal ccs (region vs VICM):

### Q) Plot "region" OP parameter vs VICM for the input pair and the tail current source




### Q) Find the CM input range (CMIR). Compare with hand analysis in a table




Hand Analysis:

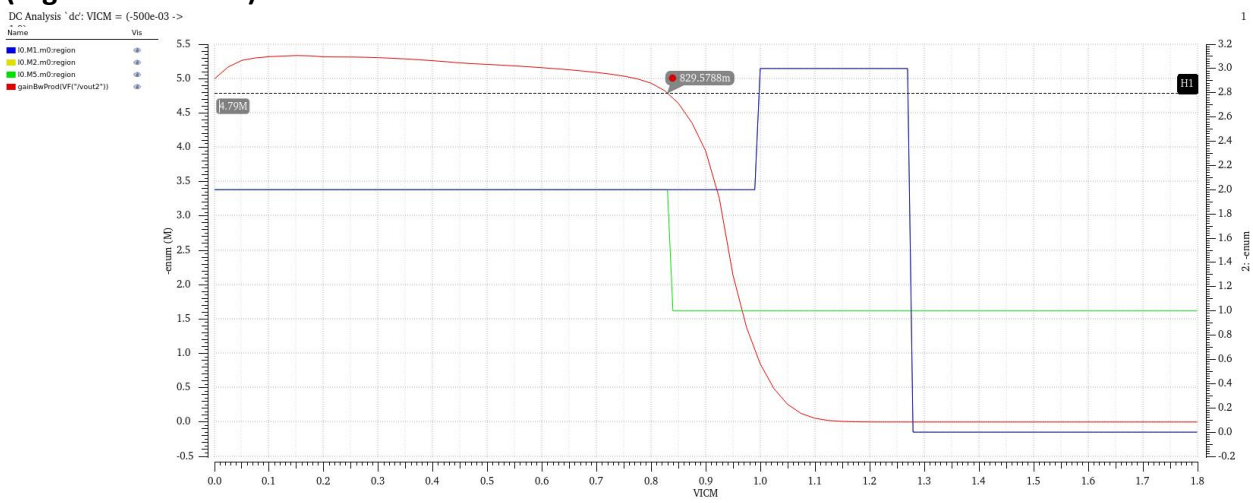
$$CMIR_{low} =- |VGS1,2| + |Vdsat1,2| + VGS3,4 =- 32.4mV$$
$$CMIR_{high} =- |VGS1,2| - |Vdsat5| + VDD = 825.6mV$$

| | Name | Value |
|---|---|---|
| 1 | I0.M1.m0:vgs | -870.0E-3 |
| 2 | I0.M1.m0:vdsat | -123.2E-3 |
| 3 | I0.M3.m0:vgs | 714.4E-3 |
| 4 | I0.M5.m0:vdsat | -104.4E-3 |

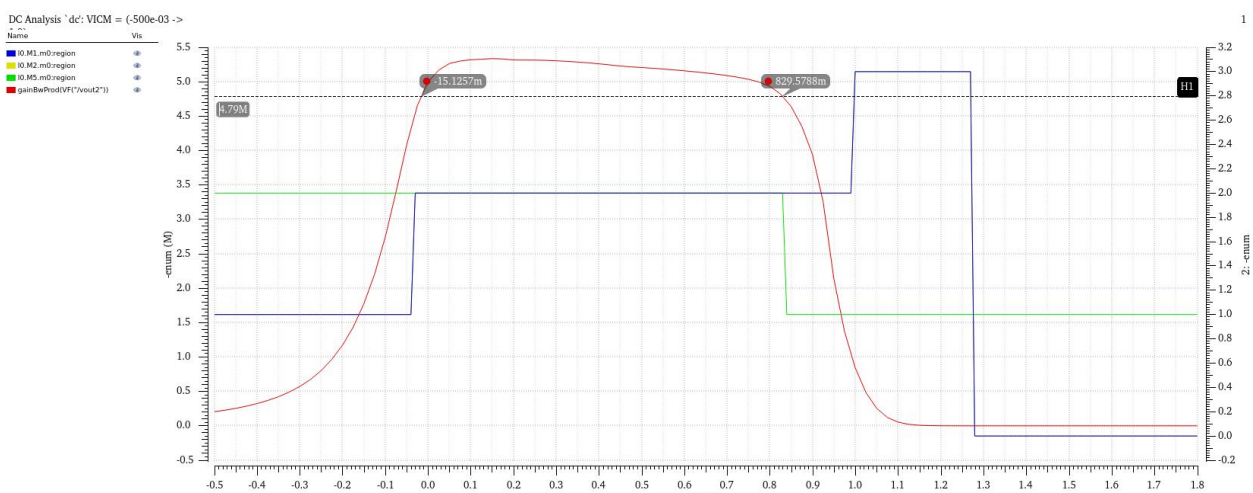
| | Hand analysis | Simulation |
|---|---|---|
| $\boldsymbol{CMIR_{low}}$ | $-32.4mV$ | $-30mV$ |
| $\boldsymbol{CMIR_{high}}$ | $825.6mV$ | $826.88mV$ |

## 7) CM large signal ccs (GBW vs VICM):

**Q) Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region Parameter)**



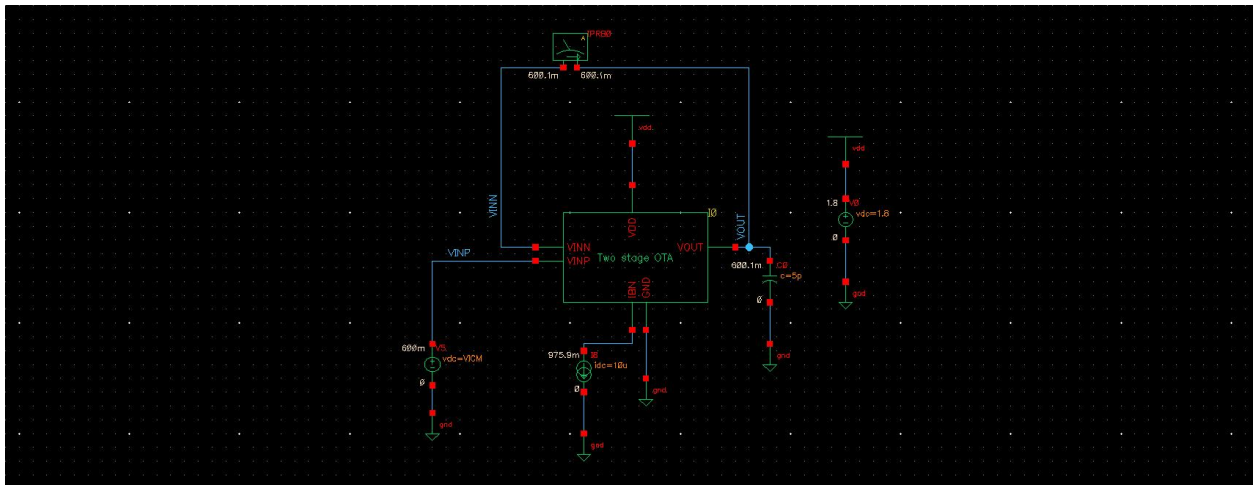

**Q) Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW**

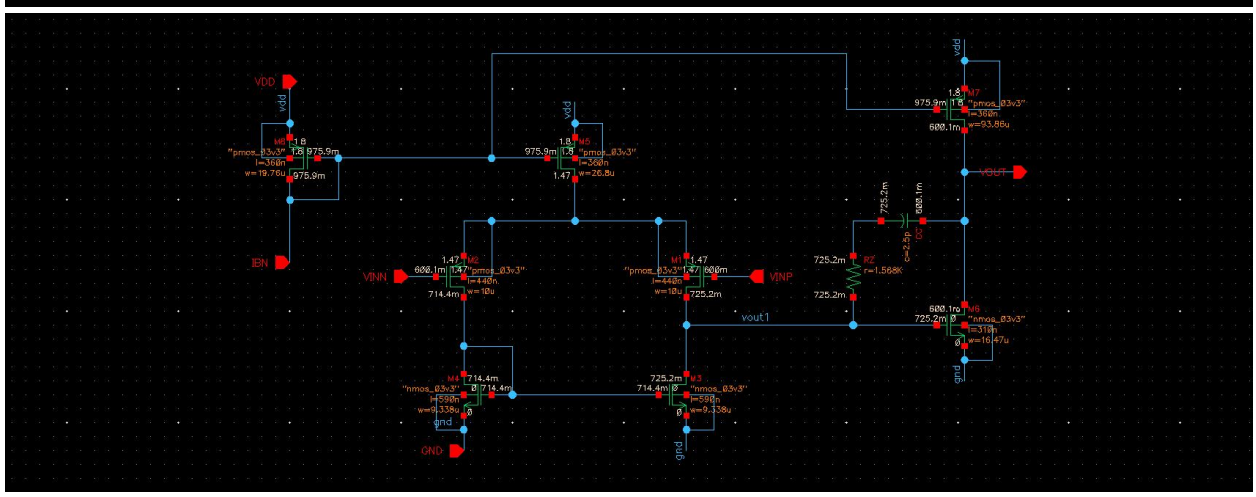



CMIR over which GBW is within 90% is from -15.1257mV TO 829.5788mV.

# PART 4: Closed-Loop OTA Simulation:

**1) Schematic of the OTA and the bias circuit with DC OP**




**Q) Are the DC voltages at the input terminals of the op-amp exactly equal? Why?**

No, they aren't equal as VGS6 will dominate and $Vout1 = \text{VGS6}$ then there is offset at vout1 and it will be $725.2 - 714.4 = 10.8mV$ and we know that

$Verr = \frac{Vout1}{AOL1} = \frac{10.8}{78.97} = 0.136mV$ and then $Verr = VINN - VINP$ then VINN= $600.1mV$.

Note that VINN is the positive terminal if we consider the first stage only so the expression of Verr was like that.

**Q) Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?**

No, as here VGS6 dominates the node Vout1 and it is set by it but in the open loop Vout1 follows mirror node so it was 714.5mV.

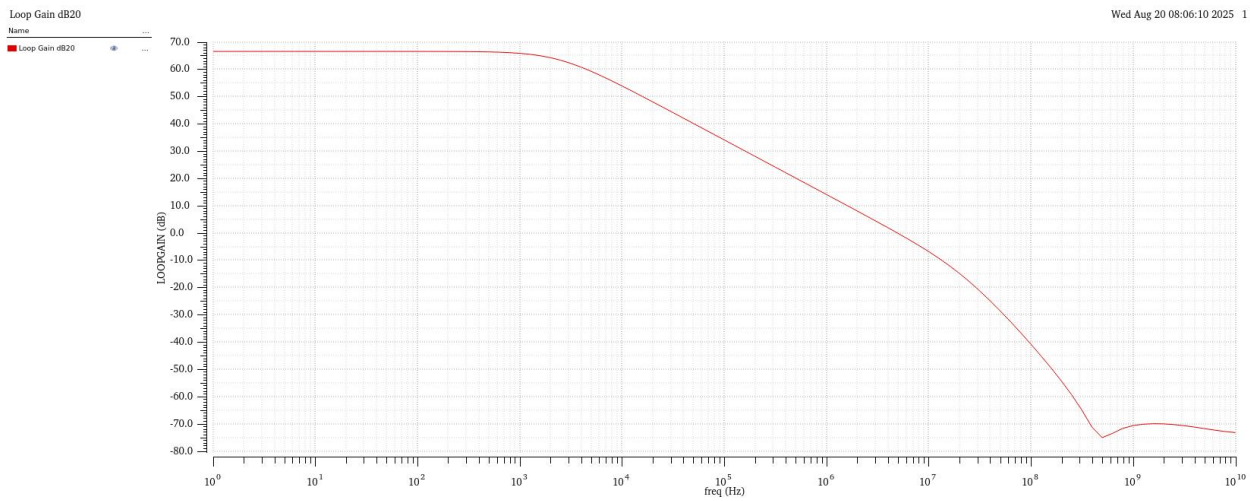
**Q) Is the current (and gm) in the input pair exactly equal? Why?**

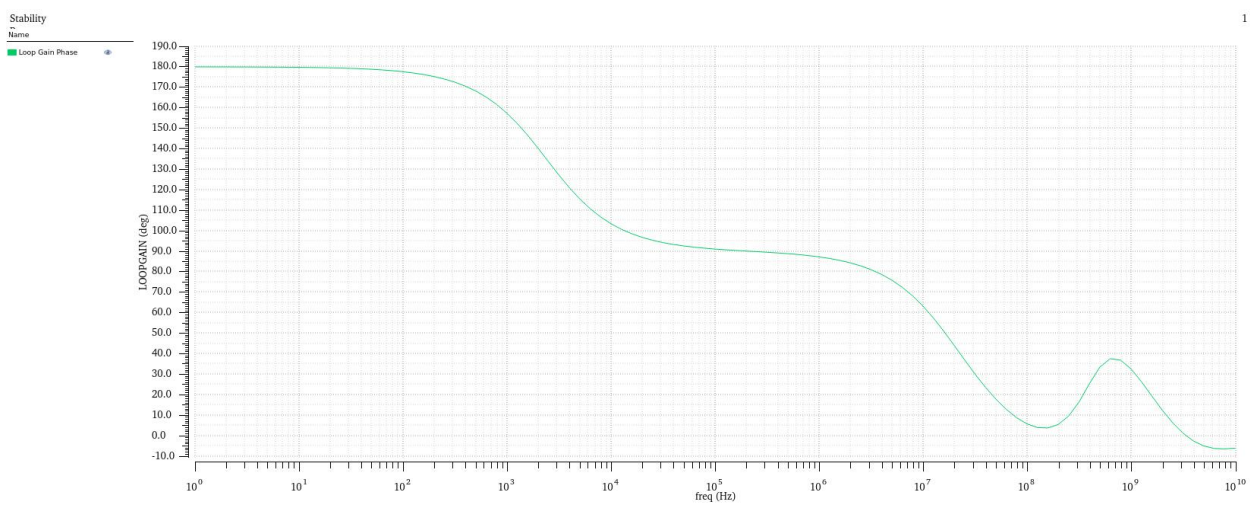
| I0.M1.m0:id | I0.M2.m0:id | I0.M1.m0:gm | I0.M2.m0:gm |
|---|---|---|---|
| -6.235E-6 | -6.230E-6 | 84.73E-6 | 84.69E-6 |

No, they are not exactly equal as the bias voltage of each transistor of the input pair is slightly changed ($VGS1 \neq VGS2$) which makes a small change in current and gm and M1 current and gm are higher as VGS1 is higher than VGS2.

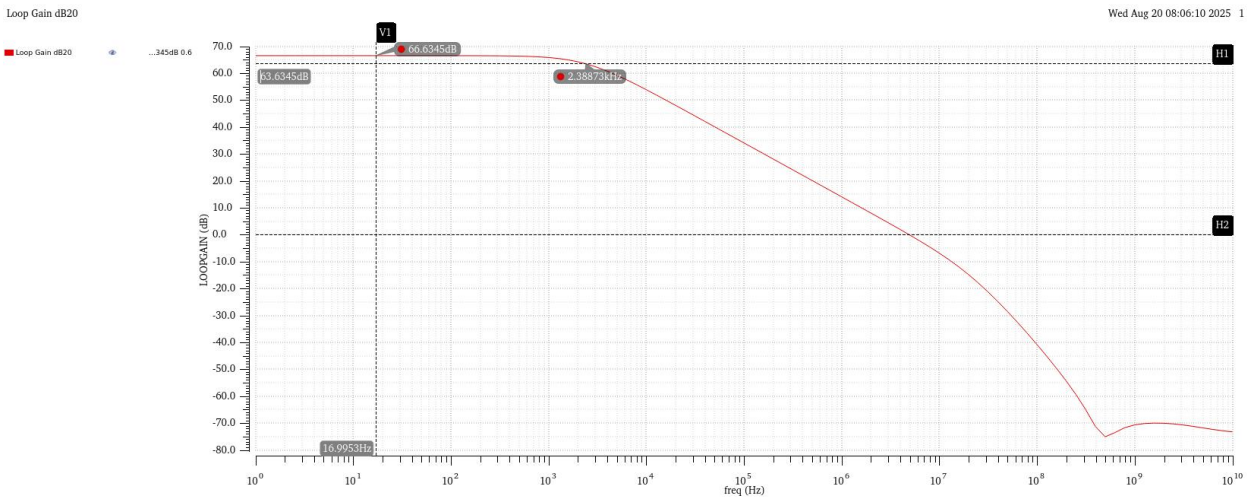
## 2) Loop gain:

**Q) Plot loop gain in dB and phase vs frequency**



**Q) Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment**



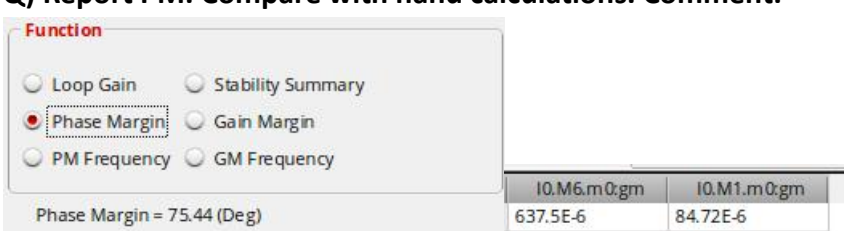

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| ITI_labs:Lab_09_TB2:1 | Loop Gain Phase | | | | |
| ITI_labs:Lab_09_TB2:1 | Loop Gain dB20 | | | | |
| ITI_labs:Lab_09_TB2:1 | Phase Margin | 75.44 | | | |
| ITI_labs:Lab_09_TB2:1 | gainBwProd(mag(getData("loop... | 5.15M | | | |
| ITI_labs:Lab_09_TB2:1 | unityGainFreq(mag(getData("lo... | 4.999M | | | |
| ITI_labs:Lab_09_TB2:1 | ymax(mag(getData("loopGain" ?... | 2.147k | | | |

| | Loop gain | Open loop |
|---|---|---|
| Gain | 2147 | 2219 |
| UGF | $4.999MHz$ | $5.011Hz$ |
| GBW | $5.15MHz$ | $5.163MHz$ |

**Comment:**

As expected, the results for loop gain are approximately the same as open loop gain as $LG = \beta * Aol$ and $\beta = 1$ as it is in a buffer connection.

**Q) Report PM. Compare with hand calculations. Comment.**




$$PM = 90 - tan^{-1}\left(\frac{\omega u}{\omega p2}\right) = 90 - tan^{-1}\left(\frac{gm1,2}{gm6} * \frac{Cl}{Cc}\right) = 75.11°$$

| | Hand analysis | Simulation |
|---|---|---|
| PM | 75.11° | 75.44° |

**Comment:**

As We made gm6 high enough we made the non-dominant pole further which increased phase margin there is almost no overshoot as $PM \approx 76°$ but as it is slightly less thanit there will be a very small overshoot but there is no peaking or ringing.

**Q) Compare simulation results with hand calculations in a table**

$A1 = \frac{gm1,2}{gds1,2+gds3,4} = 78.97 = 37.95dB$ , $A2 = \frac{gm6}{gds6+gds7} = 28.127 = 28.98dB$

$A = A1 + A2 = 37.95 + 28.98 = 66.932dB = 2221$

$BW = \frac{1}{2\pi Cc*\left(1+\frac{gm6}{gds6+gds7}\right)*\frac{1}{gds1,2+gds3,4}} = 2346Hz$

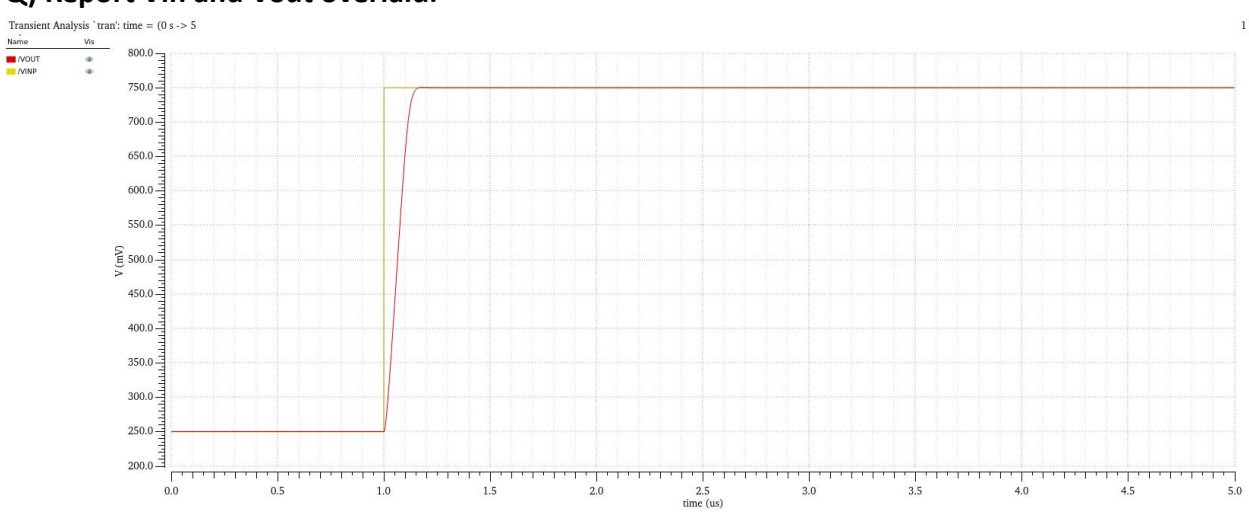
$GBW = A * BW = 5.21MHz$ and $UGF \approx GBW$ for first order systems.

| | I0.M1.m0:gm | I0.M1.m0:gds | I0.M3.m0:gds | I0.M6.m0:gm | I0.M6.m0:gds | I0.M7.m0:gds |
|---|---|---|---|---|---|---|
| 1 | 84.72E-6 | 535.7E-9 | 537.7E-9 | 637.5E-6 | 15.89E-6 | 6.775E-6 |

| | Hand analysis | Simulation |
|---|---|---|
| Gain | 2221 | 2147 |
| UGF | 5.21MHz | $4.999MHz$ |
| GBW | 5.21MHz | $5.15MHz$ |
| PM | 75.11° | 75.44° |

**3) Slew rate:**

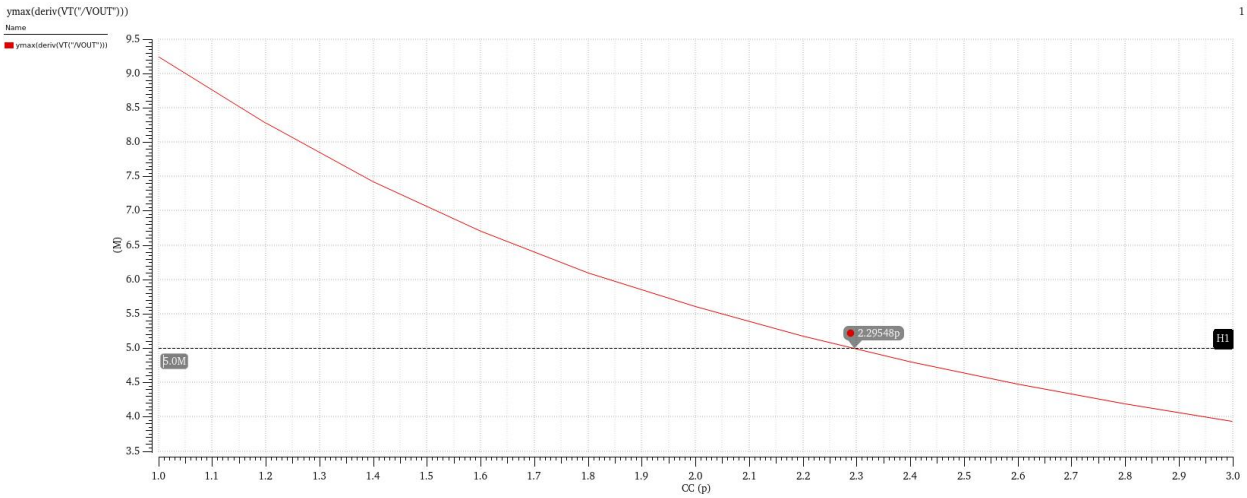
**Q) Report Vin and Vout overlaid:**



**Q) Report the slew rate:**

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| ITI_labs:Lab_09_TB2:1 | ymax(deriv(VT("/VOUT"))) | 4.637M | | | |

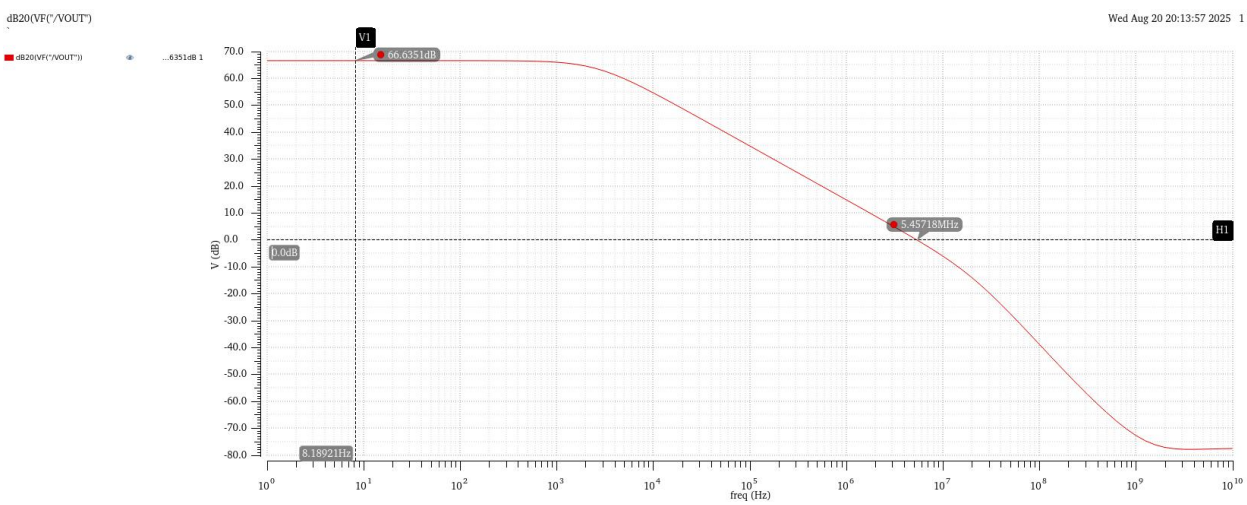
The SR wasn't achieved so we will change Cc to achieve it




But this reduced PM and became 74.27 but still achieves the condition

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| ITI_labs:Lab_09_TB2:1 | Phase Margin | 74.27 | | | |

and it increased the GBW but it is better.




Now the new slew rate became 5.002V/$\mu s$

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| ITI_labs:Lab_09_TB2:1 | ymax(deriv(VT("/VOUT"))) | 5.002M | | | |

**Q) Compare simulation results with hand calculations in a table**

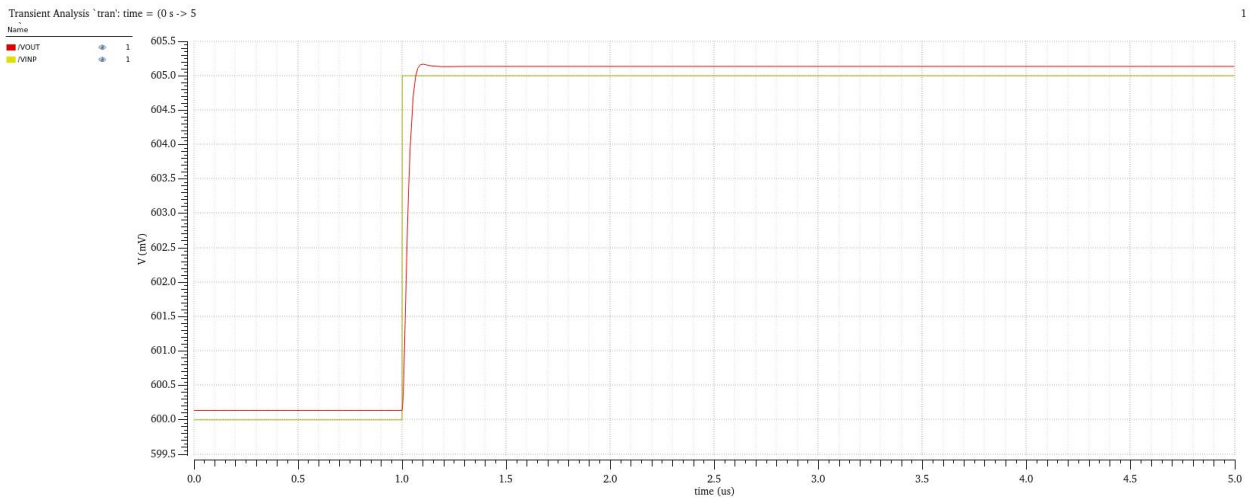
$$SR = \frac{ISS1}{Cc} = \frac{12.5}{2.29} = 5.45V/\mu s$$

| | Hand analysis | Simulation |
|---|---|---|
| SR | $5.45V/\mu s$ | $5.002V/\mu s$ |

4) **Settling time:**

**Q) Calculate the output rise time from simulation**

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| ITI_labs:Lab_09_TB 2:1 | riseTime(VT("/VOUT") 0.6001369... | 44.05n | | | |




**Q) Compare simulation results with hand calculations in a table**

$\tau = \frac{1}{2\pi\omega cl}$ $and\ \omega cl = \omega u\ then\ \tau = \frac{1}{2\pi\omega u} = 29.165ns$ then $trise = 2.2\tau = 64.16ns$

| | Hand analysis | Simulation |
|---|---|---|
| Rise time | 64.16 | $44.05ns$ |

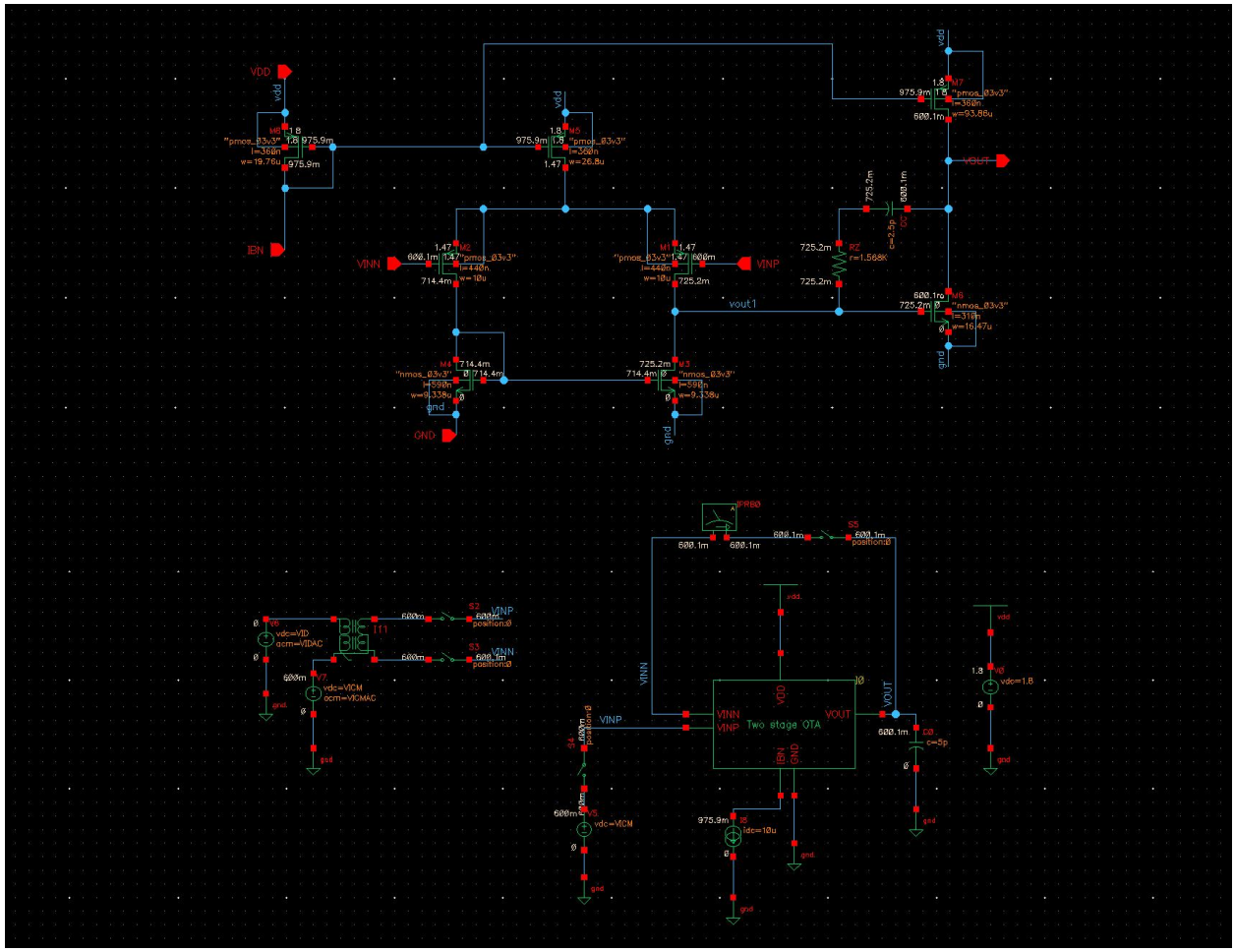
The simulation is a lot better as in hand analysis we used $trise = 2.2\tau$ but this relation is from first order system and can't be applied for second order systems and second order systems are faster than first order.

**Q) Do you see any ringing? Why?**

No, there is no ringing as $PM = 74.27 > 65.5$ so there is no ringing but there is a slight overshoot as $PM < 76$

# Part 5 (optional): DC Closed Loop AC Open-Loop OTA Simulation:

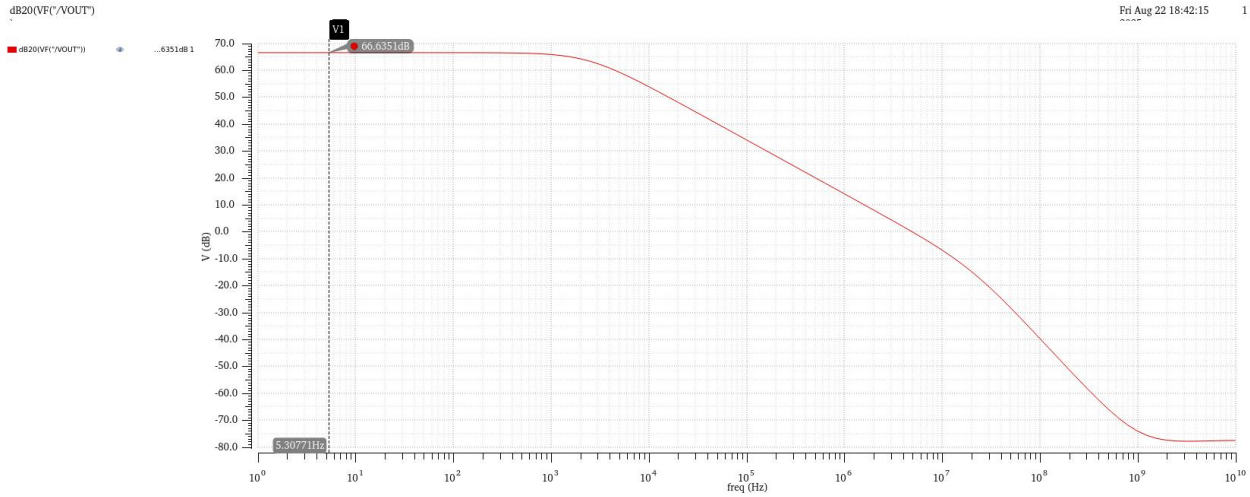
1) **Schematic and DCOP:**



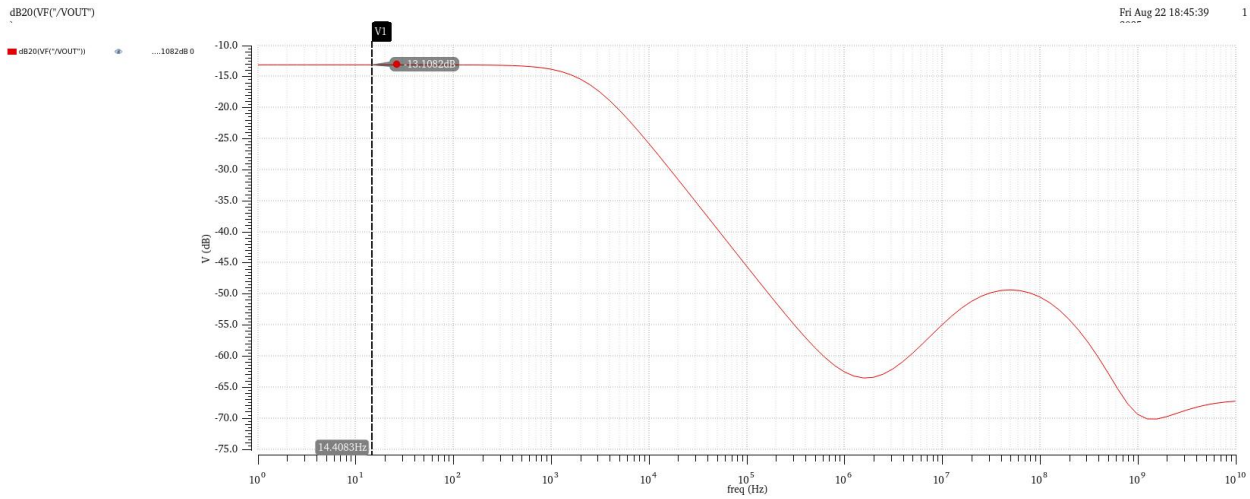

**Comment:**

We notice that DCOP is the same as closed loop simulation as at DC the switches S4 and S5 are on and S2 and S3 are off so it is the same as unity gain buffer simulation.

## 2) Diff Analysis:




## 3) CM Analysis:




- We notice that the simulations are the same as loop gain simulation we have done in part 4. We can also notice that the Acm has a large difference as there is a mismatch in gm due to the slight change in biasing which led to mismatch in gm.

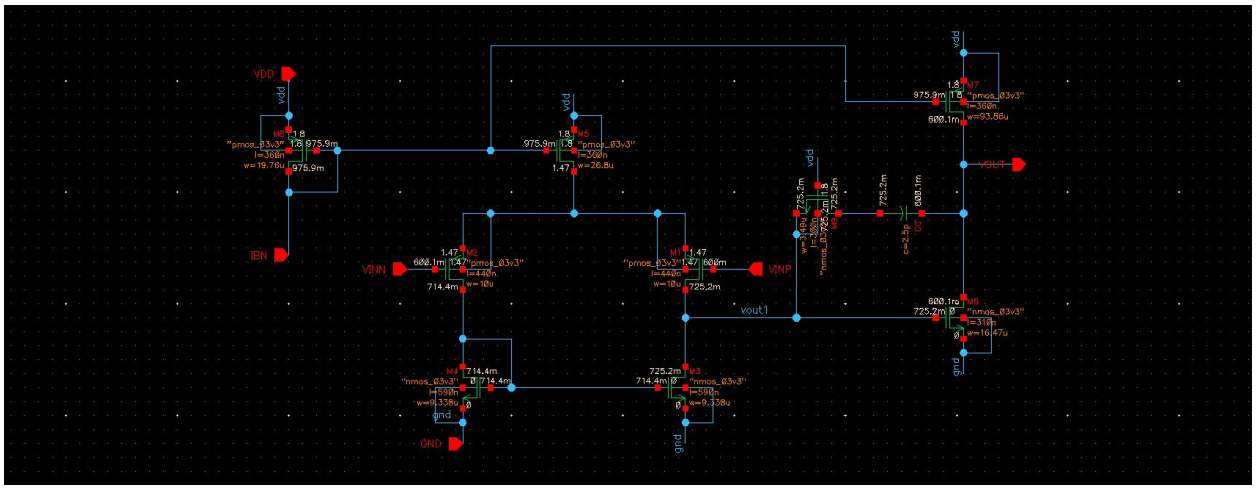
## Specs comparison:

| | Required Specs | **Achieved Specs** |
|---|---|---|
| Static gain error | $\leq 0.05\%$ | $0.045\%$ |
| CMRR @ DC | $\geq 74dB$ | $76.177dB$ |
| Phase margin | $\geq 70°$ | $74.27°$ |
| current consumption | $\leq 60\mu A$ | $60\mu A$ |
| CMIR – high | $\geq 0.8V$ | $0.82688V$ |
| CMIR – low | $\leq 0.2V$ | $-0.03V$ |
| Output swing | $0.2: 1.6$ | 0.116:1.693 |
| Buffer closed loop rise time | $\leq 70nS$ | $44.05ns$ |
| Slew rate | $5V/\mu s$ | $5.002V/\mu s$ |

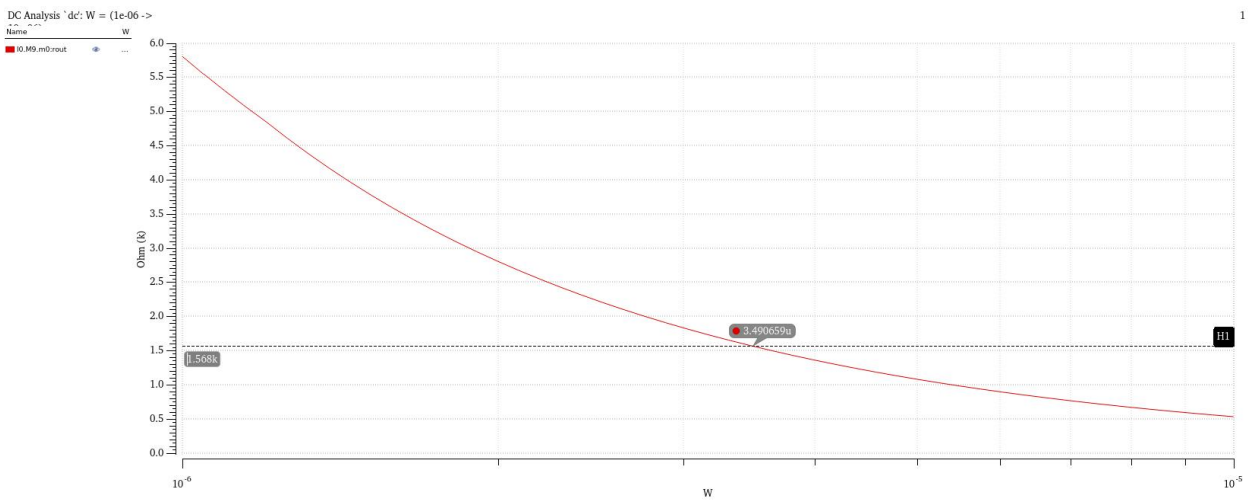
# Bonus Section:

- **Implement Rz with a transistor:**

  **Schematic:**



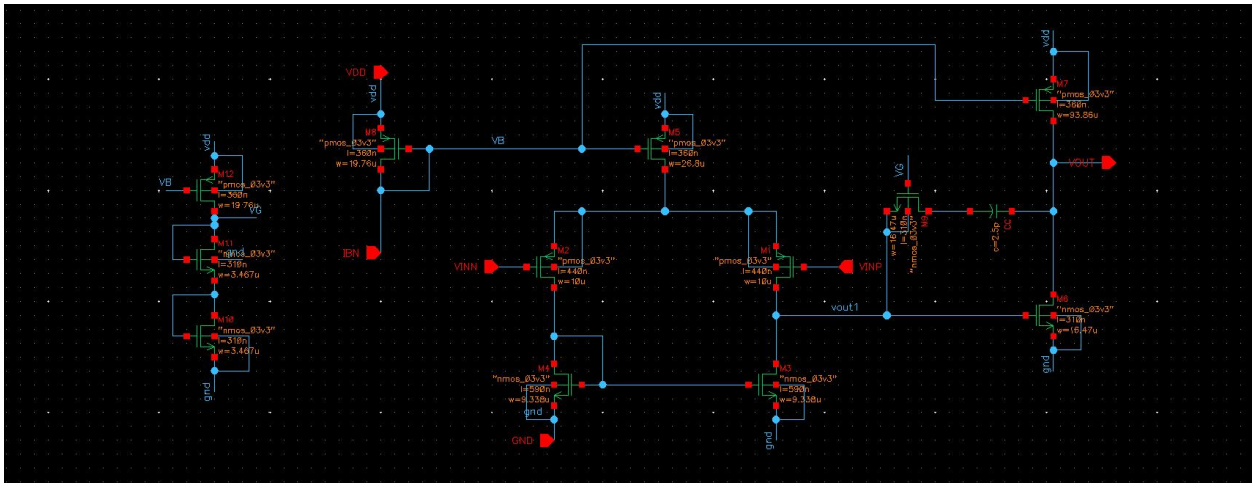

We assumed L= $300nm$ then We will sweep W to get $Rout = \frac{1}{gm6} = 1568\Omega$




Finally, we check on PM and it is achieved.

We notice that M9 works in deep triode as a Voltage controlled resistance.

But this method is for this gm6 only if it changed this will be wrong so to track gm6 we need a bias circuit to control gate of M9 to do that




First, We want M6 to match M10 to have the same bias point ($V^*$) so We need

$\frac{Iout2}{IB} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_{10}}$ and we know from the current mirror ratio that $\frac{Iout2}{IB} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_{12}}$

If We assume that $IB = 10\mu A$ then $\left(\frac{W}{L}\right)_{10} = \frac{3.467u}{310n}$ and $\left(\frac{W}{L}\right)_{12} = \frac{19.76u}{360n}$

Now, if we use square law as a simple analytical method, We find that

$Rz = \frac{1}{k' * \left(\frac{W}{L}\right)_9 * Vov9}$ and we want it to match $\frac{1}{gm6} = \frac{1}{k' * \left(\frac{W}{L}\right)_6 * vov6}$

Now, M9 and M12 are matched so they have the same Vov

$$\frac{Vov13}{Vov12} = \frac{\left(\frac{2I}{k' * \left(\frac{W}{L}\right)_{13}}\right)^{0.5}}{\left(\frac{2I}{k' * \left(\frac{W}{L}\right)_{12}}\right)^{0.5}} = \sqrt{\frac{\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_{13}}} = \frac{Vov6}{Vov9}$$

$Rz * gm6 = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_9} \sqrt{\frac{\left(\frac{W}{L}\right)_{12}}{\left(\frac{W}{L}\right)_{13}}}$ so from here we can use $\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_9 and \left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{13}$

PM will stay at 72.18 even if bias point changed and PM isn't best as we used square law we can do a sweep and draw PM and choose the PM we want and this PM will never change with the change in gm6.