

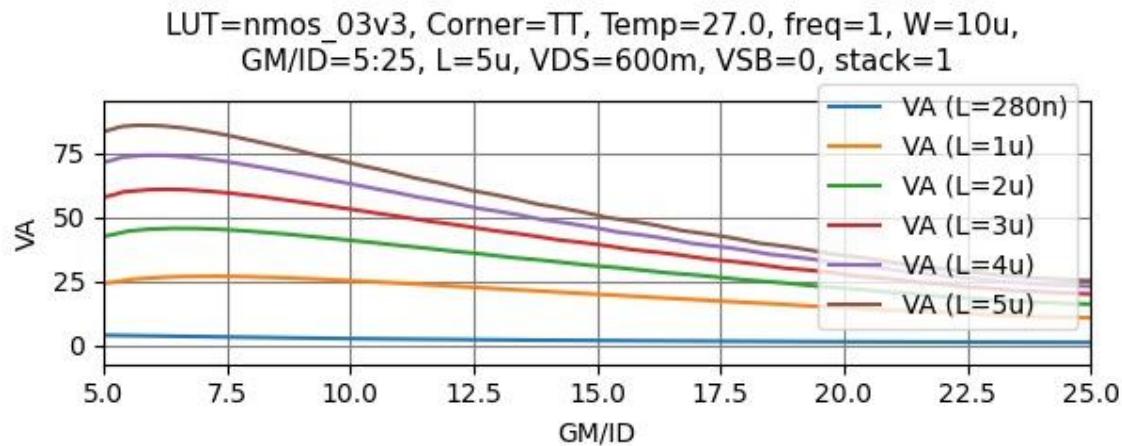
# Lab 11

## PART 1: gm/ID Design Charts:

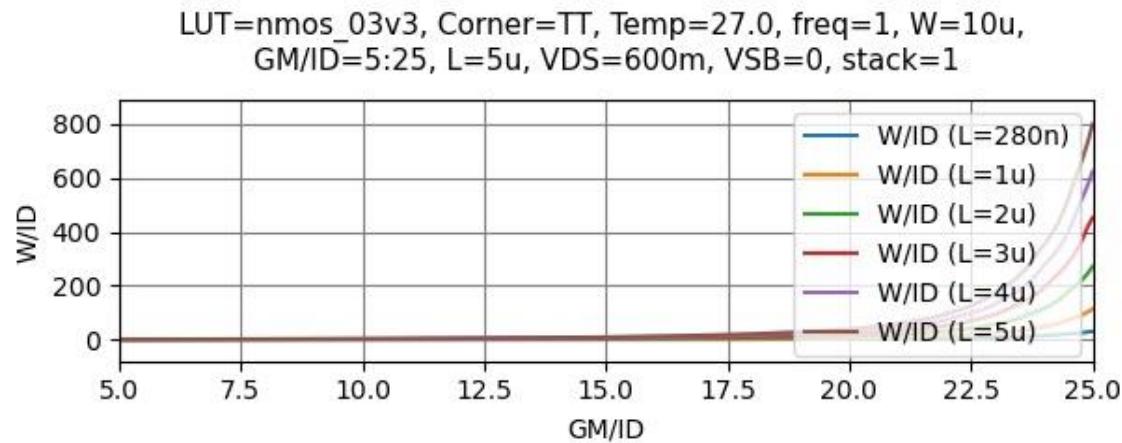
Using ADT Sizing Assistant, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS to a reasonable value and L = min,1u:1u:5u.

- NMOS:

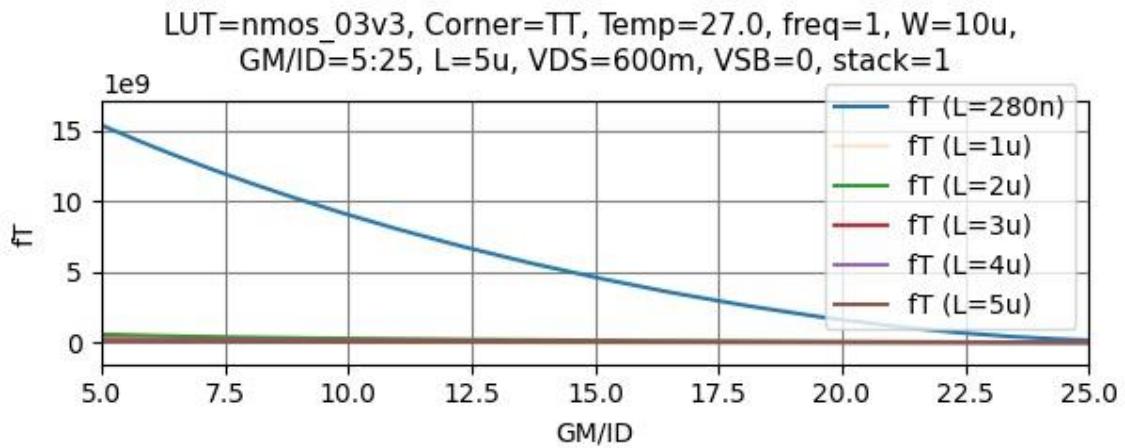
- 1) VA:



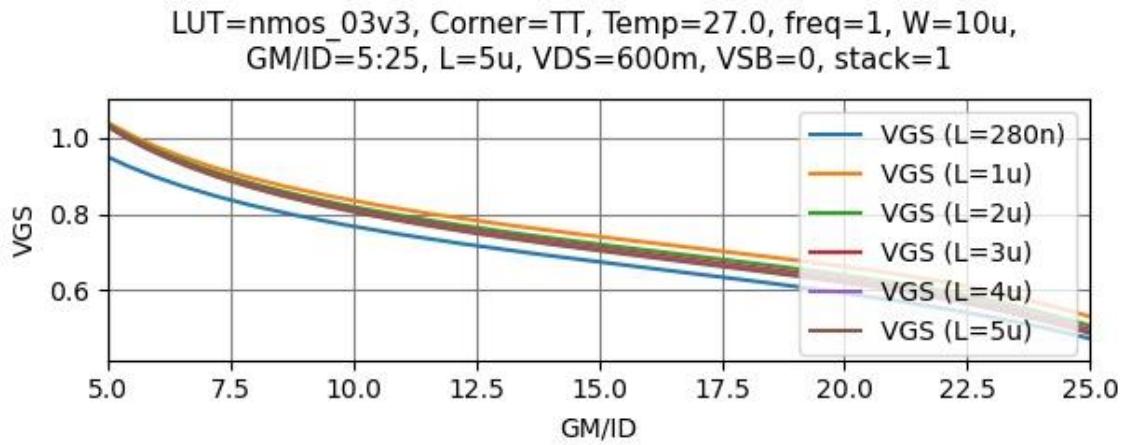
- 2) W/ID:



3) fT:

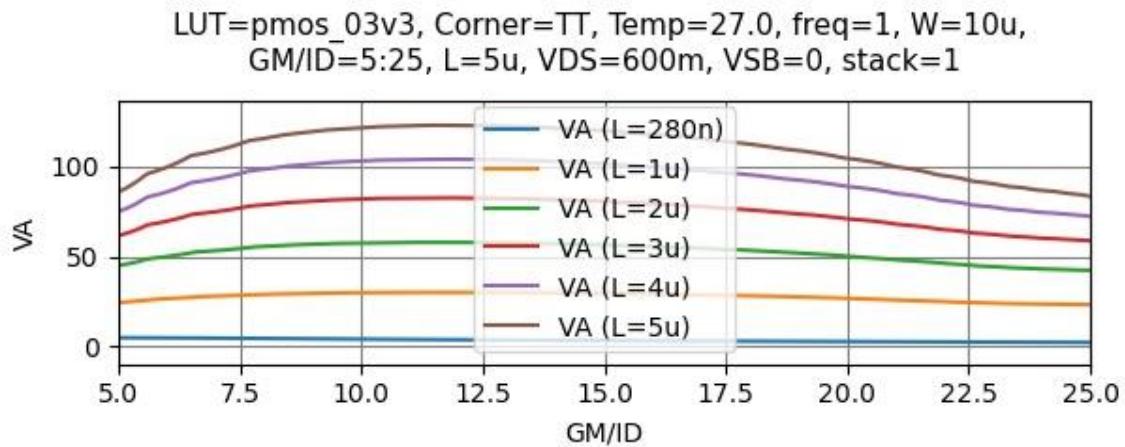


4) VGS:

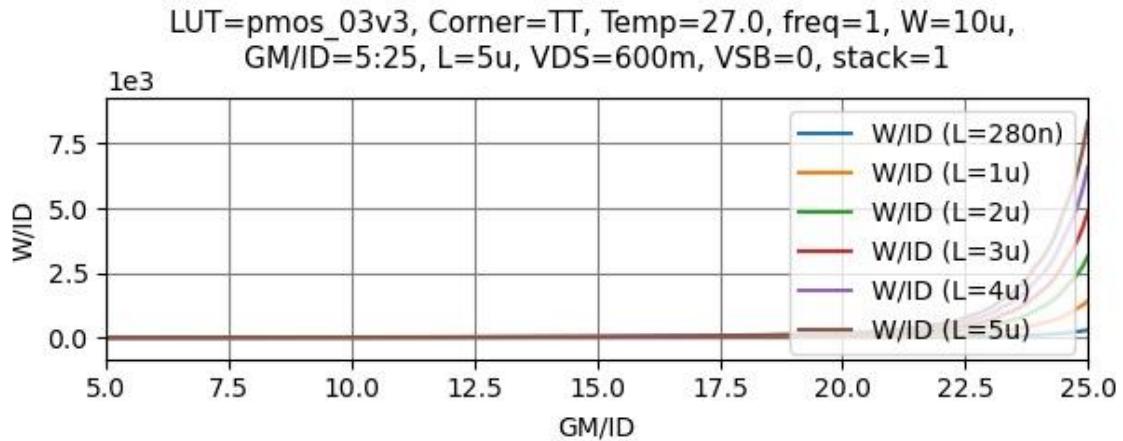


- PMOS:

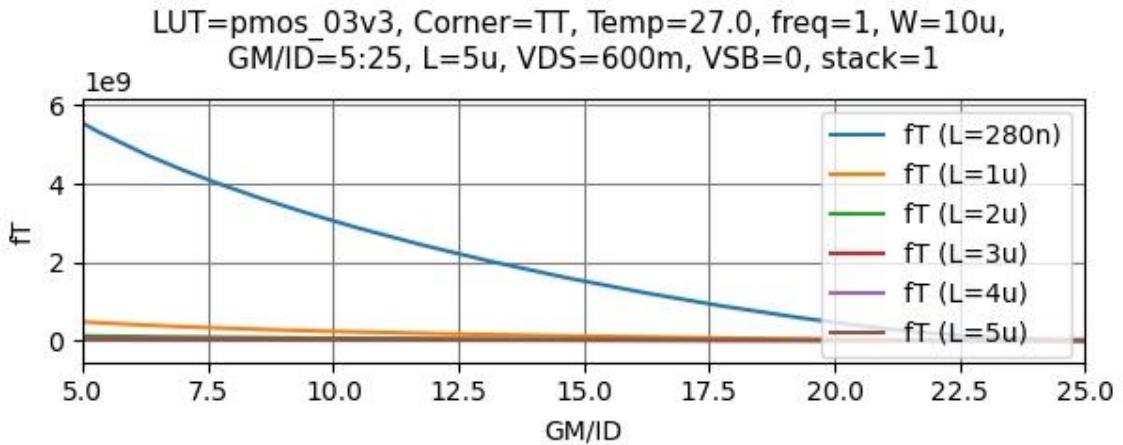
1) VA:



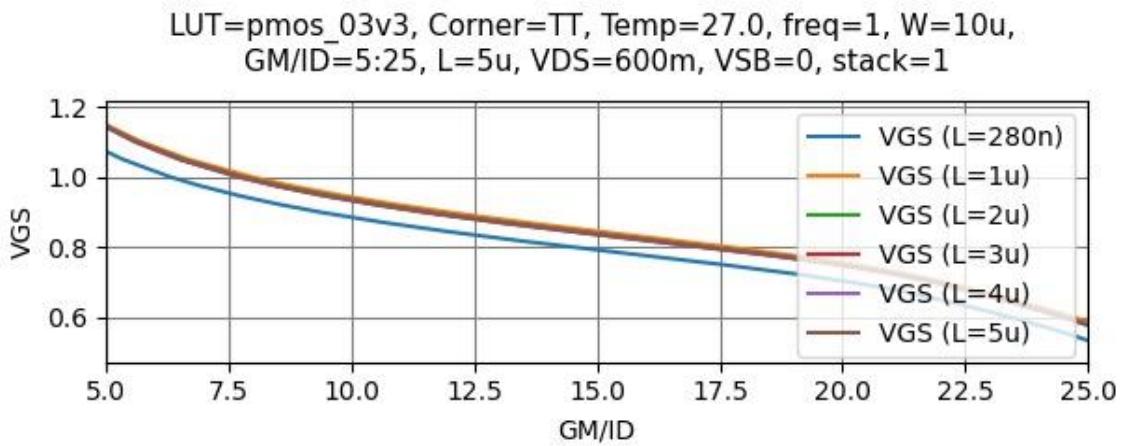
2) W/ID:



3) fT:



4) VGS:

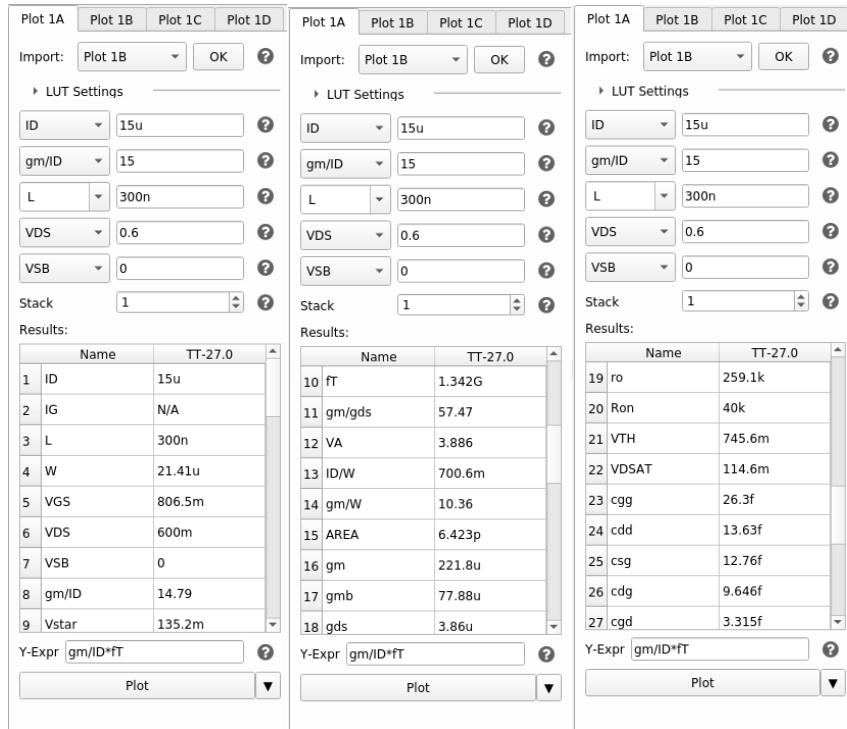


## PART 2: OTA Design:

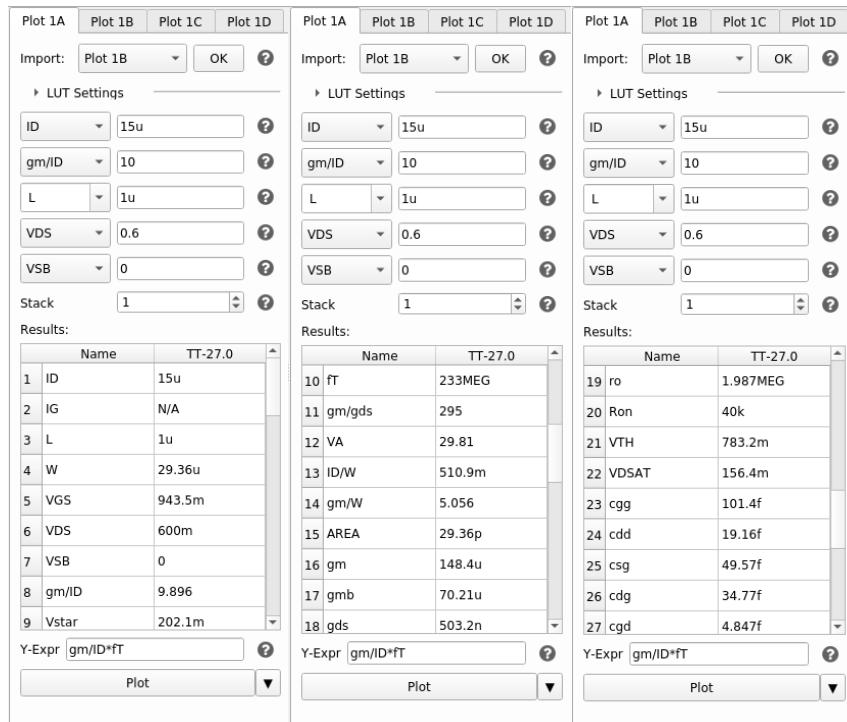
Specifications	
Closed loop gain	2
Phase margin	$\geq 70^\circ$
CM input range low	$\leq 0$
CM input range high	$\geq 1V$
Differential output swing	$1.2V \text{ pk to pk}$
DC loop gain	$60dB$
CL settling time for 1% error	$100ns$

### Design procedure:

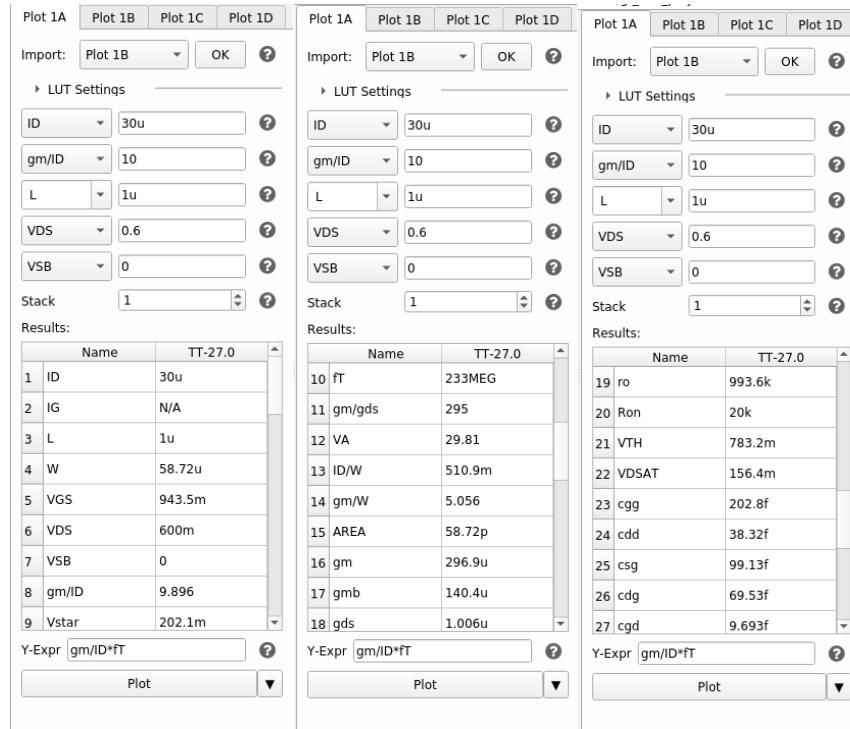
- We see that the input range is closer to ground so we will use the input pair to be PMOS.
- For the input pair (M1&M2) we assume  $L = 300nm$  to not get very high W which increases capacitances and we will assume  $\frac{gm}{ID} = 15$  to get high gm and then increase the speed by increasing GBW.
- We want  $LG = 1000$  and we have  $\beta_v = \frac{1}{3}$  so we get  $A_{ol} = 3000$ .
- We want the error  $\leq 1\%$  in less than  $100ns$  so  $e^{\frac{-t}{\tau}} \leq 0.01$  then  $\tau \leq 21.7147ns$  and we know  $\tau = \frac{1}{2\pi * BW_{cl}}$  so  $BW_{cl} \geq 7.329MHz$  then  $GBW = \frac{BW_{cl}}{\beta} = 21.987MHz$ .
- $\frac{gm_{1,2}}{2\pi * (CL + CF)} \geq 21.987MHz$  so  $gm_{1,2} \geq 207.22\mu S$  then  $ID \geq 13.8\mu A$  then we choose  $ID = 15\mu A$ .



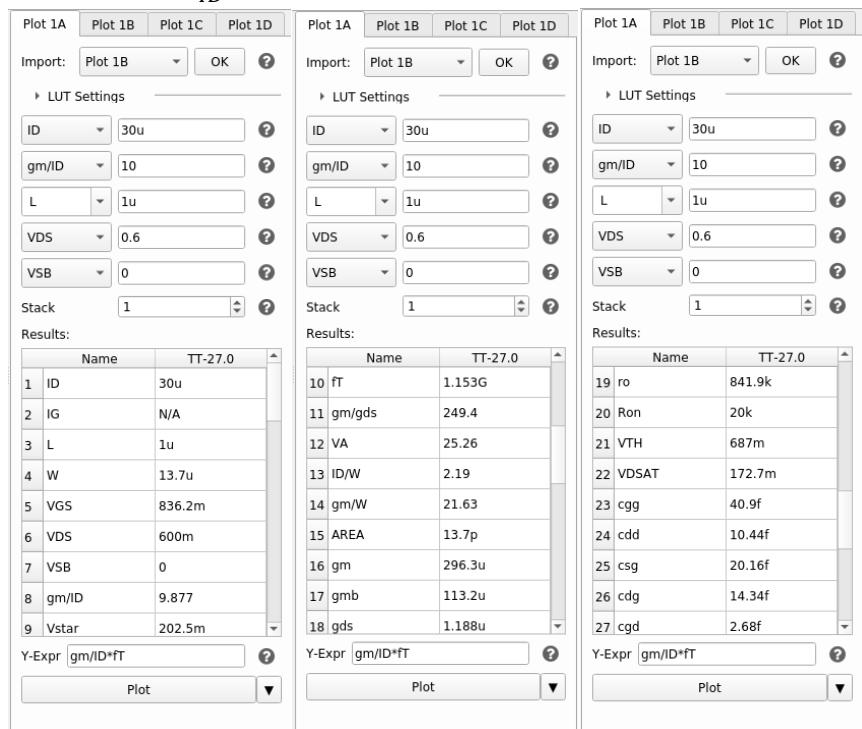
- For current mirror PMOS transistors (M10&M12) that carry  $15\mu A$  we will assume  $L = 1\mu m$  to get high  $ro$  and be less affected by  $VDS$  variations and assume  $\frac{gm}{ID} = 10$  to get lower  $gm$  to decrease input noise and input offset.



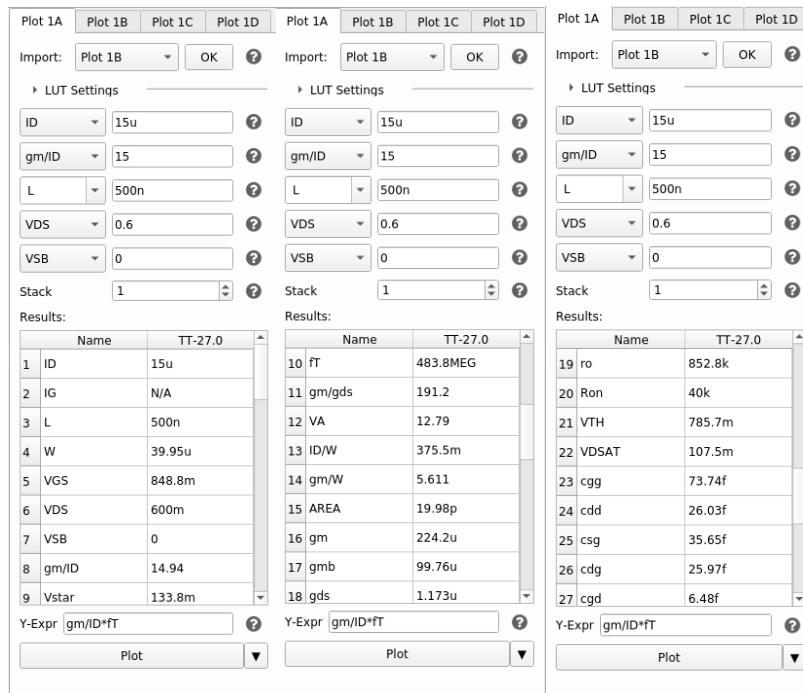
- For tail current source and other PMOS Current mirrors (M3&M4&M13), we will make the same assumptions of  $L = 1\mu m$  and  $\frac{gm}{ID} = 10$  but  $ID = 30\mu A$  and for M4  $ID = 10\mu A$ .



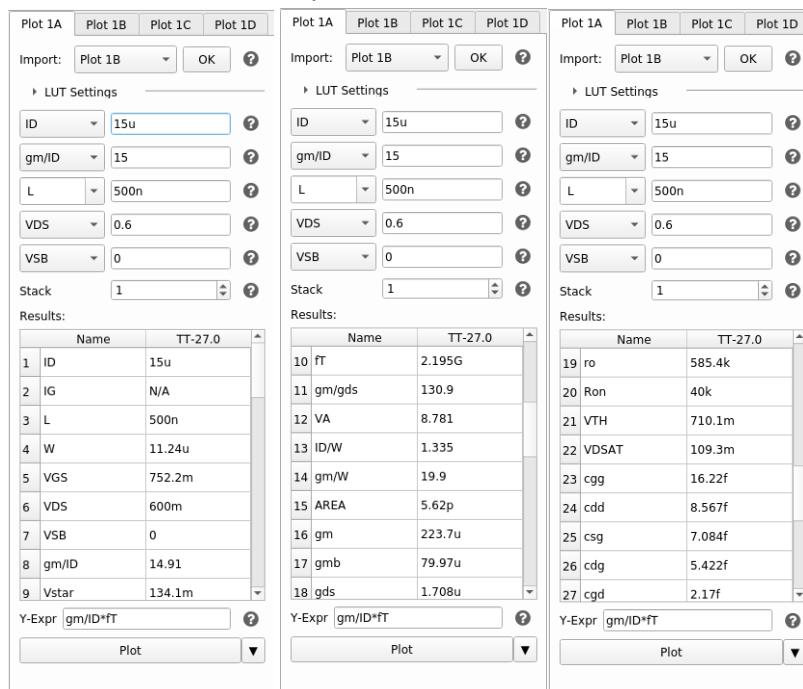
- For the NMOS mirror devices (M5&M6&M14) that sink the current We will also assume  $L = 1\mu m$  and  $\frac{gm}{ID} = 10$  and they will carry  $ID = 30\mu A$ .



- For cascode PMOS devices (M9&M11) we will assume a quite large L,  $L = 500nm$  to increase  $ro$  as it contributes to the gain and we will assume  $\frac{gm}{ID} = 15$  to improve gm which also contributes to the gain and cascode devices have low effect on input noise as its gain is degenerated so we don't fear from the high gm. Finally, we know the current in the branch  $ID = 15\mu A$ .

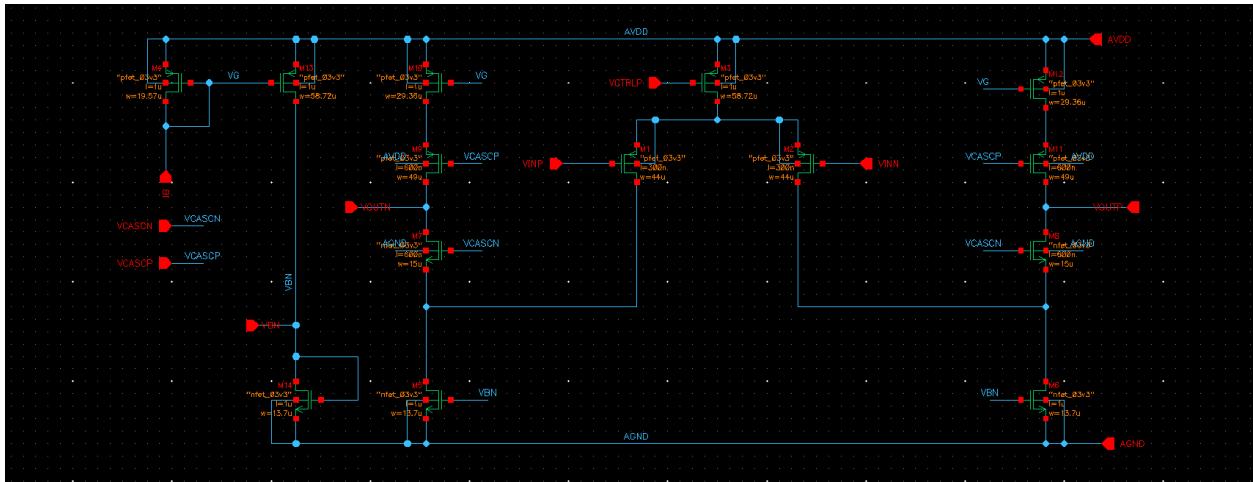


- For cascode NMOS devices (M7&M8) We will assume  $L = 500nm$  and  $\frac{gm}{ID} = 15$  and the branch carries  $ID = 15\mu A$ .



- $V_{cascn} = VGS_{7,8} + V^*_{5,6} = 954.7mV$
- $V_{cascp} = VDD - |VGS_{9,11}| - V^*_{10,12} = 1.449V$ .

### Final Schematic:

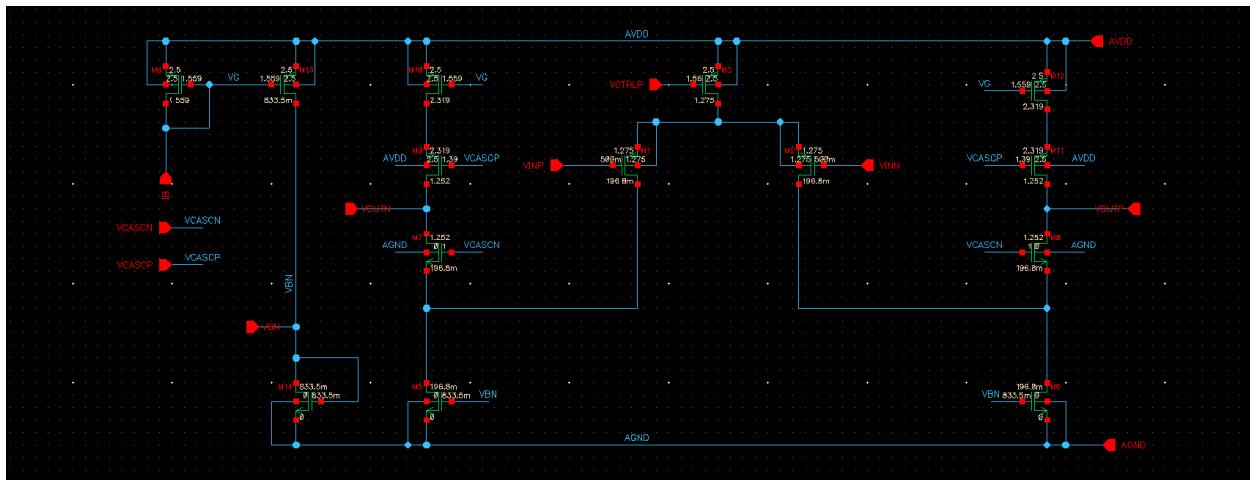


- We increased the input pair width to  $44\mu m$  to achieve the GBW specification and we increase the length of cascode device to  $L = 600nm$  maintaining the same aspect ratio to increase the  $ro$  and  $gm$  which increased the gain and achieved the specification.
- We also put  $V_{cascn} = 1$  and  $V_{cascp} = 1.4$  as the devices were in triode.

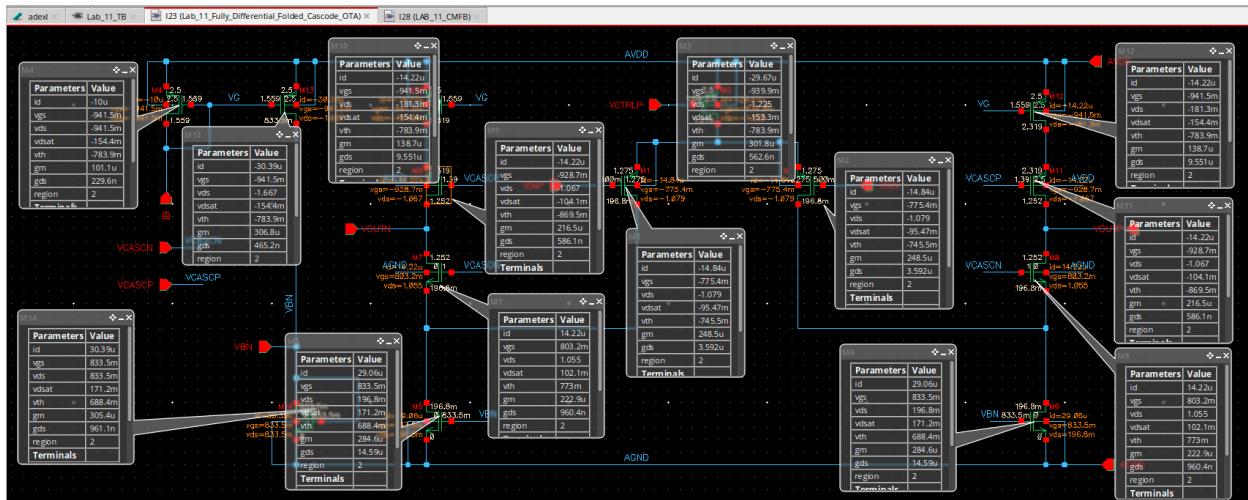
## PART 3: Open-Loop OTA Simulation (Behavioral CMFB):

### 1) Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.

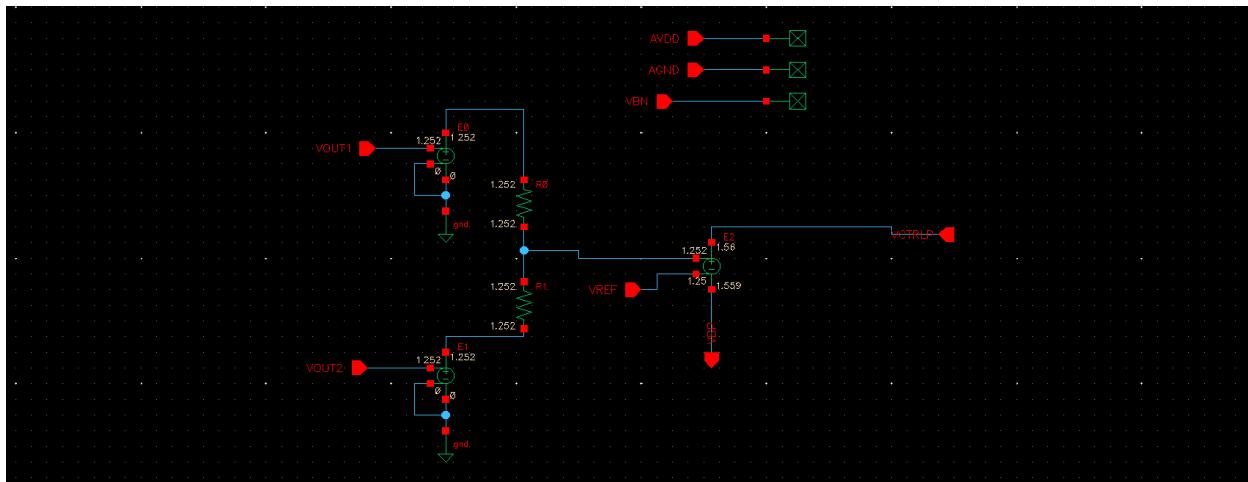
Schematic of the OTA with DC node voltages:



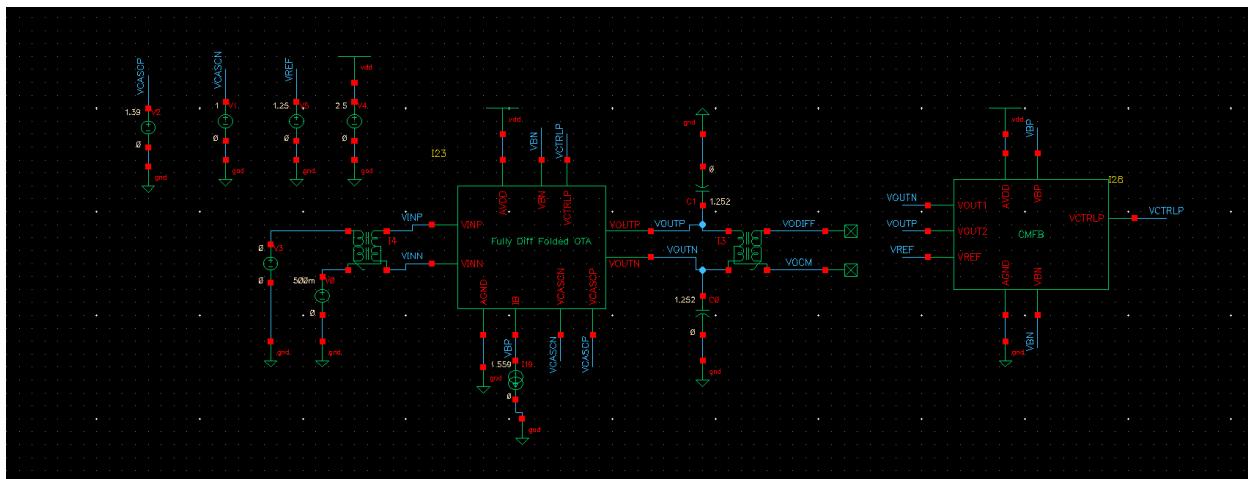
## Schematic of the OTA with transistors OP:



Schematic of CMFB with DC node voltages annotated:



Schematic of TB with DC node voltages annotated:



➤ **What is the CM level at the OTA output?**

The CM level at the OTA output is 1.252V which is very close from the Vref which was 1.25V.

➤ **What are the differential input and output voltages of the error amplifier? What is the relation between them?**

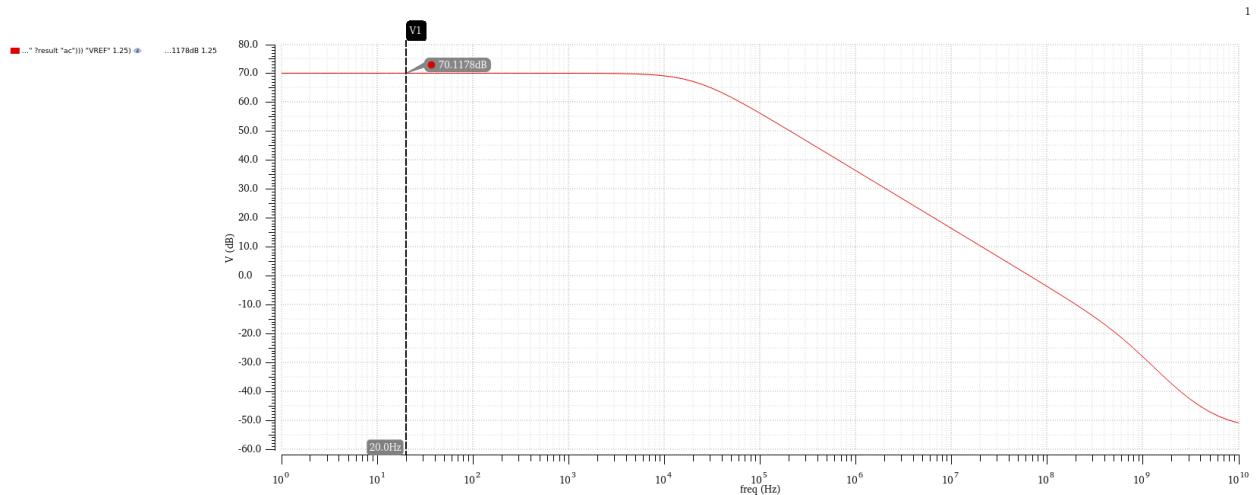
ITI_labs:Lab_11_TB1	(VDC("VCTRLP") - VDC("VBP"))	1.607m
ITI_labs:Lab_11_TB1	(VDC("I28/net21") - VDC("VREF"))	1.607m

*The differential input = The differential output = 1.607mV and the relation between them is 1 which is the gain of the error amplifier.*

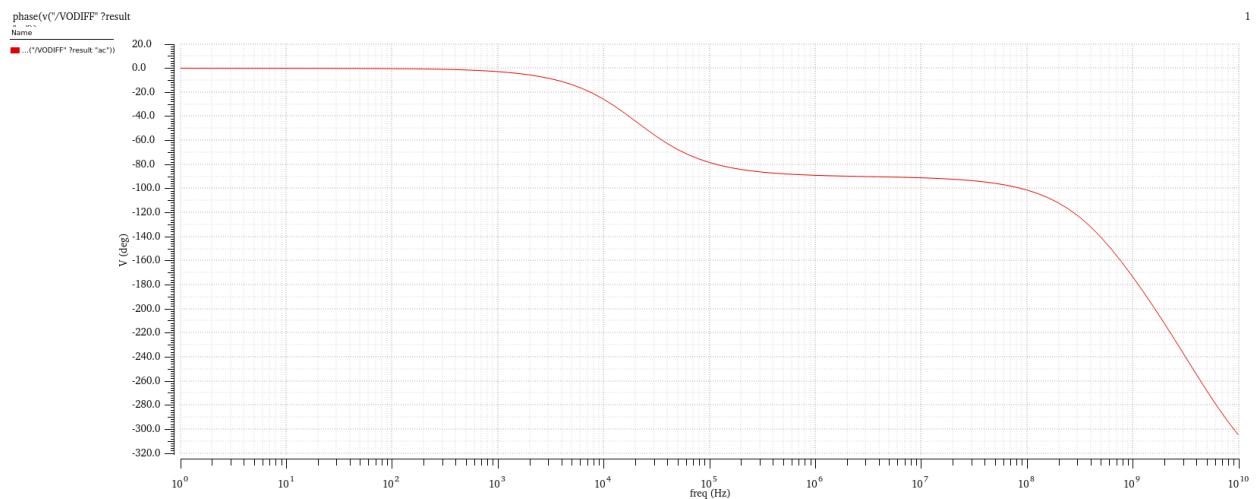
## 2) Diff small signal ccs:

➤ **Plot diff gain (magnitude in dB and phase) vs frequency.**

Magnitude:



Phase:

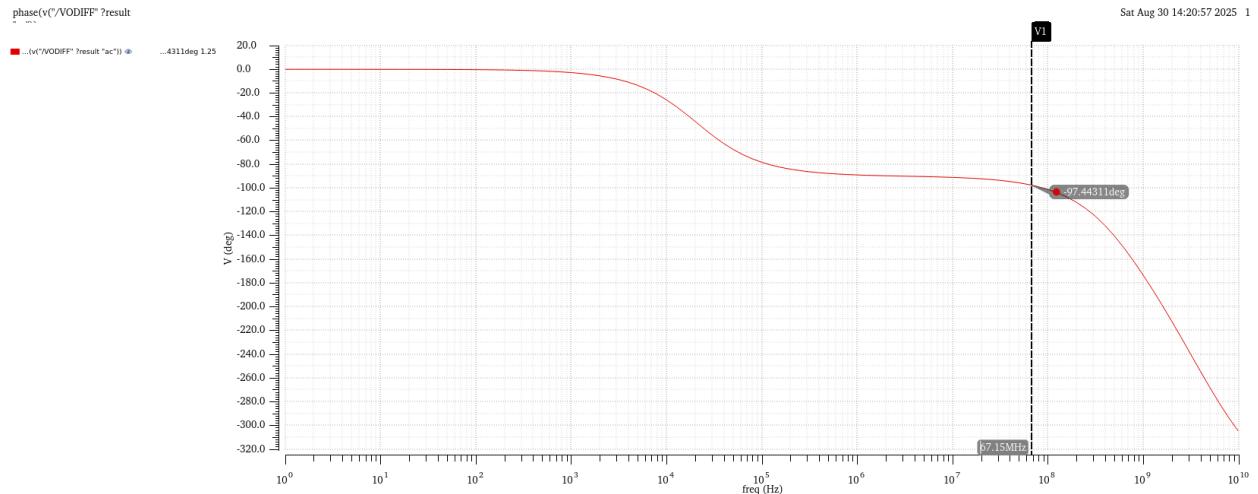


➤ Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

ITI_labs:Lab_11_TB:1	Ao	3.205k
ITI_labs:Lab_11_TB:1	Ao_dB	70.12
ITI_labs:Lab_11_TB:1	BW	20.83k
ITI_labs:Lab_11_TB:1	UGF	67.15M
ITI_labs:Lab_11_TB:1	GBW	66.77M

To calculate PM we got the phase at the gain cross over frequency then

$$PM = 180 - 97.44 = 82.56^\circ$$



➤ Compare simulation results with hand calculations in a table (use SS parameters from OP simulation in your hand analysis).

$$A = g_{m1,2} * Rout = 3218.45 = 70.15dB$$

$$Rout = (g_{m11} + g_{mb11})r_{o11}r_{o12} / (g_{m8} + g_{mb8})(r_{o6} / r_{o2})r_{o8} = 12.9515M\Omega$$

$$BW = \frac{1}{2\pi * Rout * (CL + C_{gd11} + C_{gd8} + C_{db8} + C_{db11})} = 23.464KHz$$

$$GBW = A * BW = 75.5MHz$$

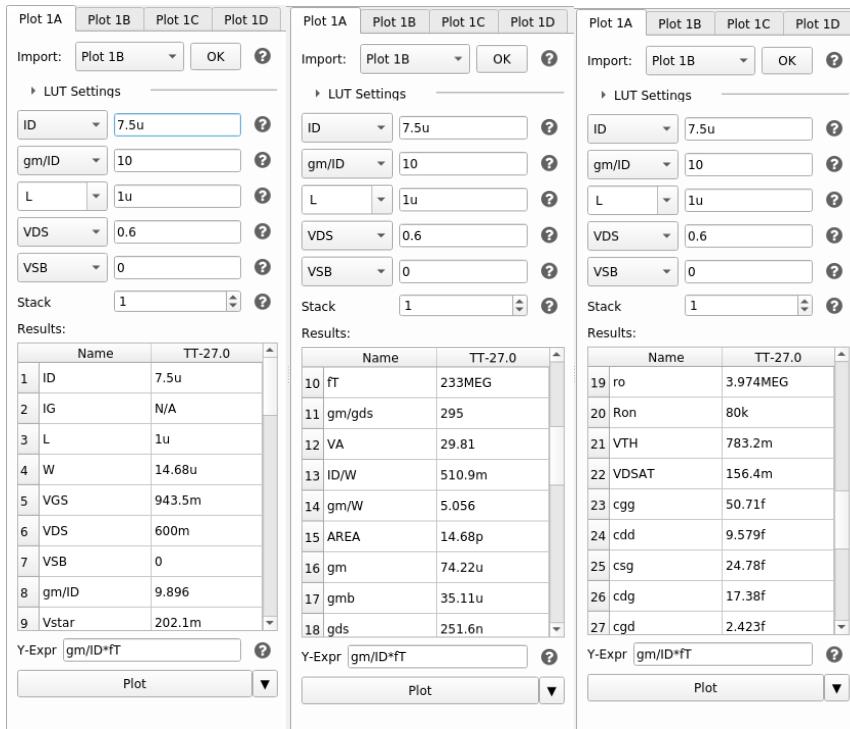
$UGF \approx GBW = 75.5MHz$  as it is approximately a first order system.

$PM \approx 90^\circ$  it approximately has one dominant pole for more accurate result we should calculate the nondominant pole which is usually at drain of M6.

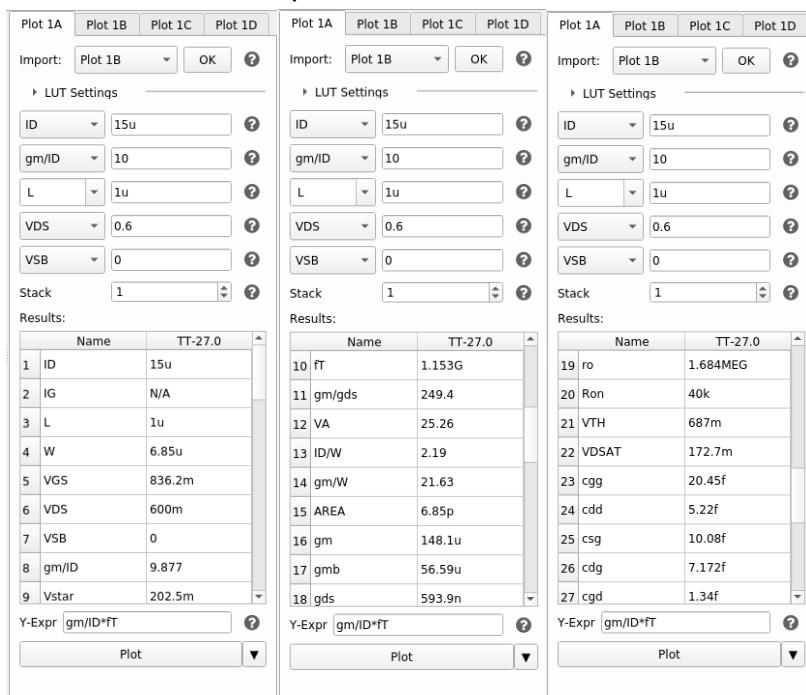
	Hand analysis	Simulation
gain	3218	3205
BW	23.464KHz	20.83KHz
GBW	75.5MHz	66.77MHz
UGF	75.5MHz	67.15MHz
Phase margin	90°	82.56°

## PART 4: Open-Loop OTA Simulation (Actual CMFB):

- M0 & M1 & M2 & M3 should be matched to the tail current source so  $L = 1\mu m$  and  $\frac{gm}{ID} = 10$  and we want  $ID = 7.5\mu A$ .



- M8 should be matched to the NMOS current mirror devices so  $L = 1\mu m$  and  $\frac{gm}{ID} = 10$  and we want  $ID = 15\mu A$ .



- M5 & M6 & M10: We will assume  $L = 1\mu m$  and  $\frac{gm}{ID} = 15$  and we want  $ID = 7.5\mu A$ .

Name	TT-27.0
1 ID	7.5u
2 IG	N/A
3 L	1u
4 W	48.39u
5 VGS	846.5m
6 VDS	600m
7 VSB	0
8 gm/ID	14.86
9 Vstar	134.6m

Name	TT-27.0
10 fT	110.6MEG
11 gm/gds	438.3
12 VA	29.5
13 ID/W	155m
14 gm/W	2.303
15 AREA	48.39p
16 gm	111.4u
17 gmb	52.91u
18 gds	254.3n

Name	TT-27.0
19 ro	3.933MEG
20 Ron	80k
21 VTH	783.2m
22 VDSAT	95.82m
23 cg	160.3f
24 cdd	31.26f
25 csg	76.63f
26 cdg	53.8f
27 cgd	7.839f

- To choose best Vref we will calculate the swing *lower end*  $\approx VCASC - VTH = 0.2$  *higher end*  $= 2.5 - 0.8465 - 0.2 = 1.6535$  then  $Vref = 0.827V$  is at the middle of the range. We will use the same CD for vref to get the same DC shift. Note that the swing condition is achieved.
- To calculate sensing resistance  $R = \frac{V_{ptp}}{ID} = \frac{1.2}{7.5 \times 10^{-6}} = 160K\Omega$ .
- For M7 & M9 We will assume  $L = 1\mu m$  and  $\frac{gm}{ID} = 15$  and we want  $ID = 7.5\mu A$ .

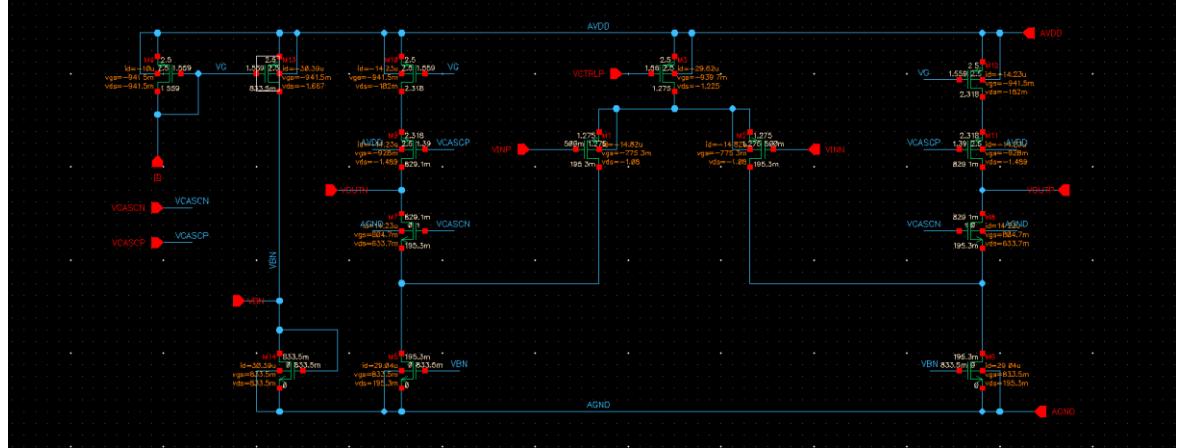
Name	TT-27.0
19 ro	2.671MEG
20 Ron	80k
21 VTH	687m
22 VDSAT	109.2m
23 cg	27.4f
24 cdd	8.118f
25 csg	12.03f
26 cdg	8.689f
27 cgd	2.061f

Name	TT-27.0
10 fT	642.3MEG
11 gm/gds	295.4
12 VA	20.03
13 ID/W	690.6m
14 gm/W	10.18
15 AREA	10.86p
16 gm	110.6u
17 gmb	42.3u
18 gds	374.4n

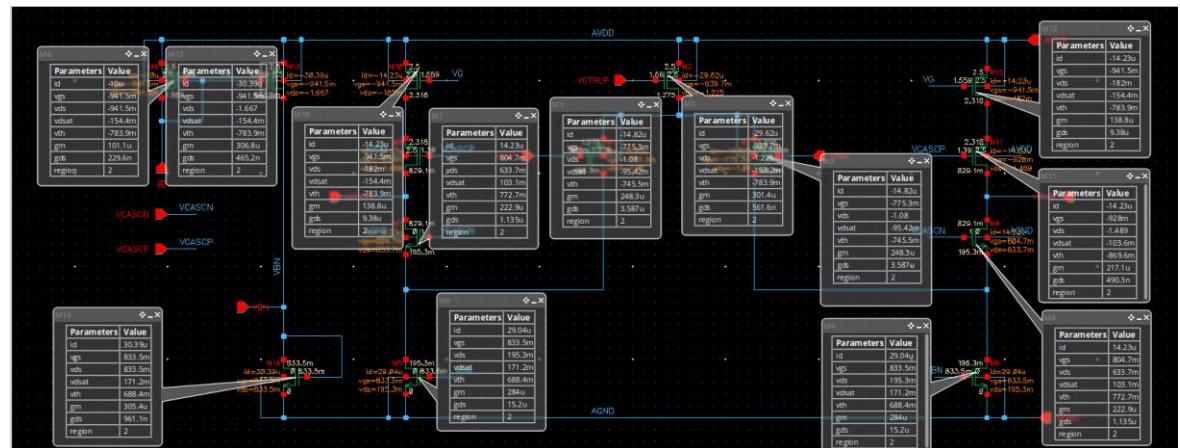
Name	TT-27.0
1 ID	7.5u
2 IG	N/A
3 L	1u
4 W	10.86u
5 VGS	742.4m
6 VDS	600m
7 VSB	0
8 gm/ID	14.75
9 Vstar	135.6m

**1) Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.**

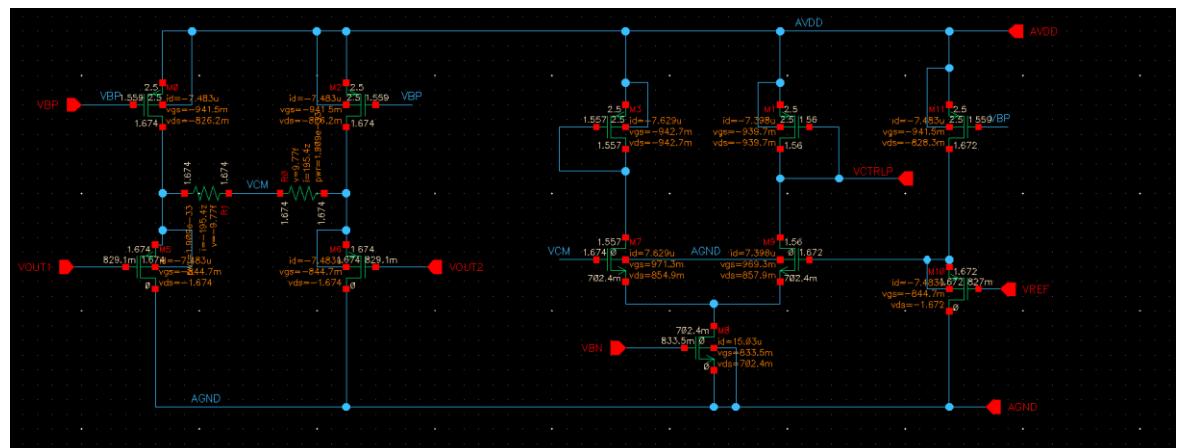
Schematic of OTA with DC node voltages:



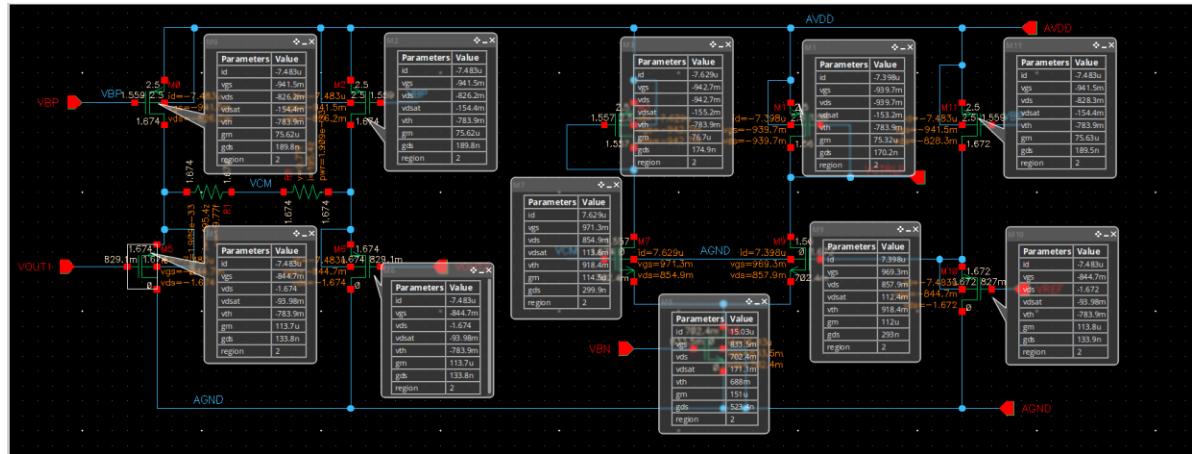
Schematic of OTA with transistors DC OP:



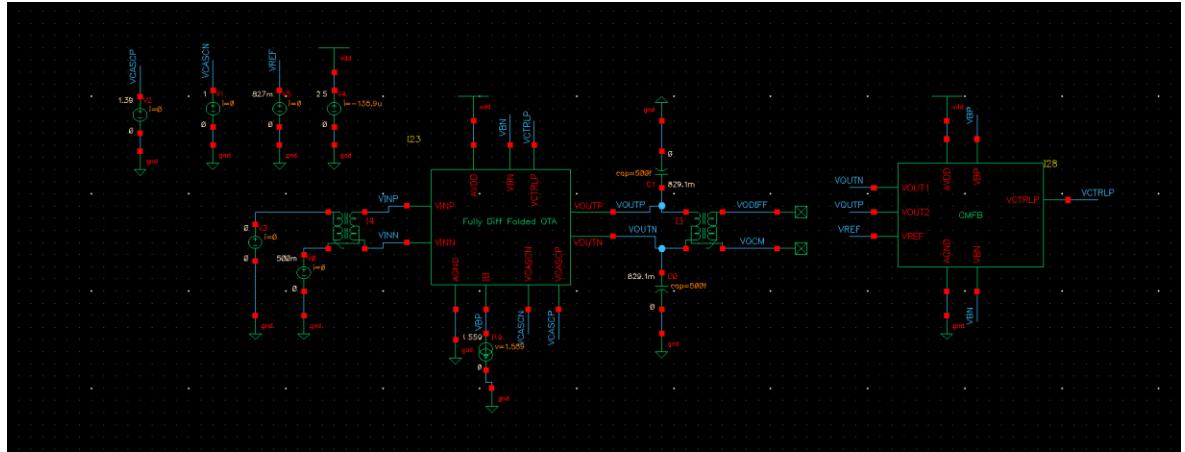
Schematic of CMFB with DC node voltages:



## Schematic of CMFB with transistors DC OP:



### Schematic of TB with DC node voltages:



- ## ➤ What is the CM level at the OTA output? Why?

the CM level at the OTA output is 829.1mV which is very close from  $V_{ref}=827\text{mV}$  and this error is because the error amplifier doesn't have high gain and we chose this CM value to be in the middle of the range of the output swing.

- What are the differential input and output voltages of the error amplifier? What is the relation between them?

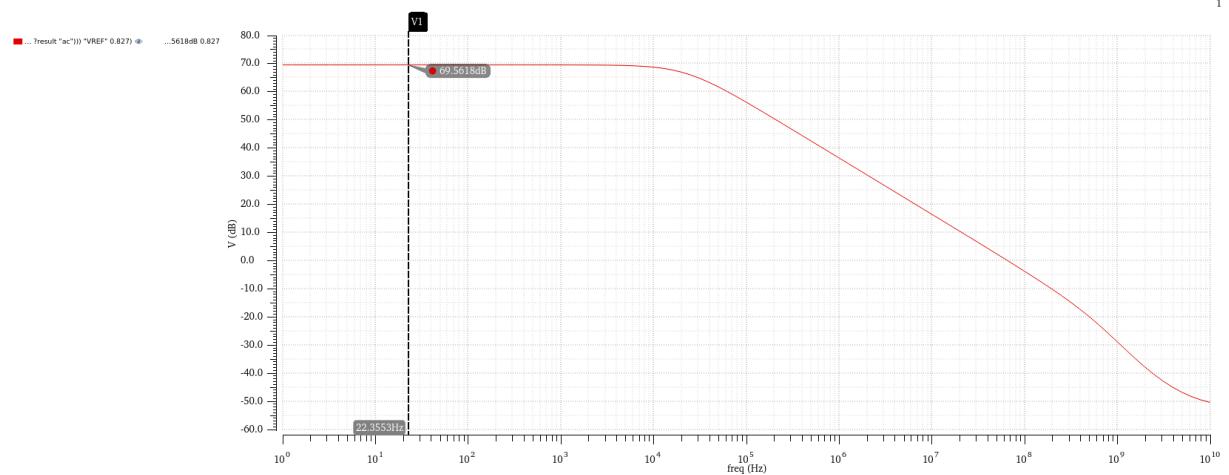
Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_labs:Lab_11_TB:1	(VDC("/VCTRLP") - VDC("/I28/net...")	3.033m			
ITI_labs:Lab_11_TB:1	(VDC("/I28/VCM") - VDC("/I28/ne...")	2.049m			

differential input = 2.049mV and differential output = 3.033mV and the relation between them is  $\frac{V_{out}}{V_{in}} = 1.48$  which equals the gain of error amplifier which is  $A = \frac{g_{m7,9}}{g_{m1,3}} = 1.487$ .

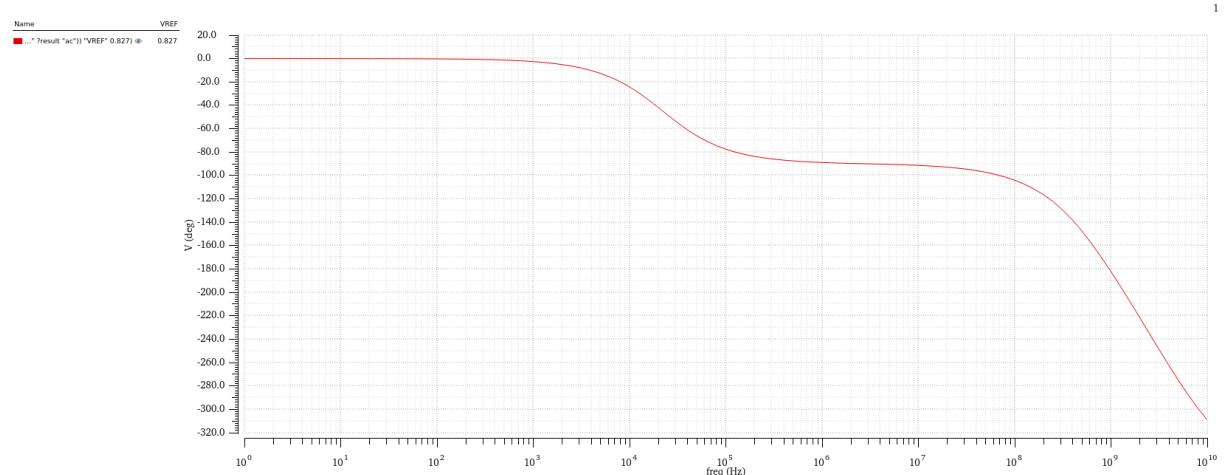
## 2) Diff small signal ccs:

- Plot diff gain (magnitude in dB and phase) vs frequency.

Magnitude:



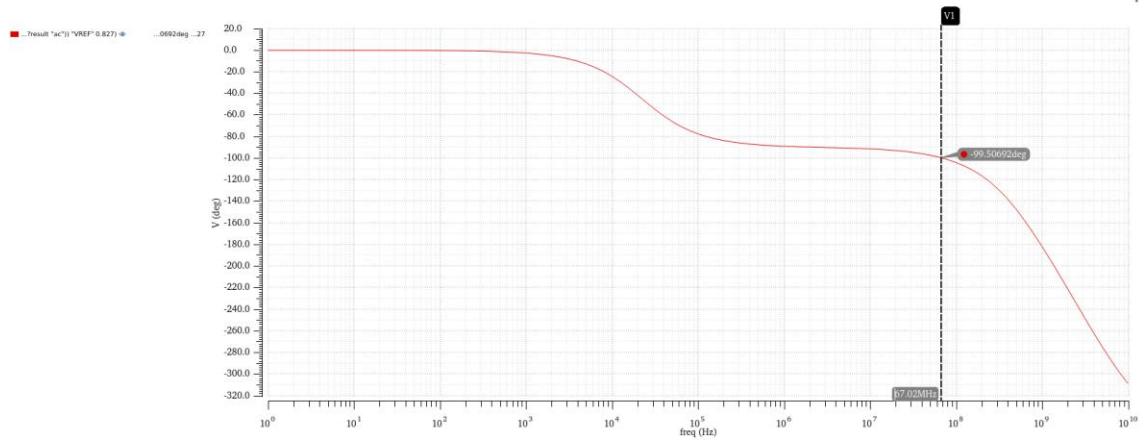
Phase:



- Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_labs:Lab_11_TB:1	Ao	3.007k			
ITI_labs:Lab_11_TB:1	Ao_dB	69.56			
ITI_labs:Lab_11_TB:1	BW	22.39k			
ITI_labs:Lab_11_TB:1	UGF	67.02M			
ITI_labs:Lab_11_TB:1	GBW	67.49M			

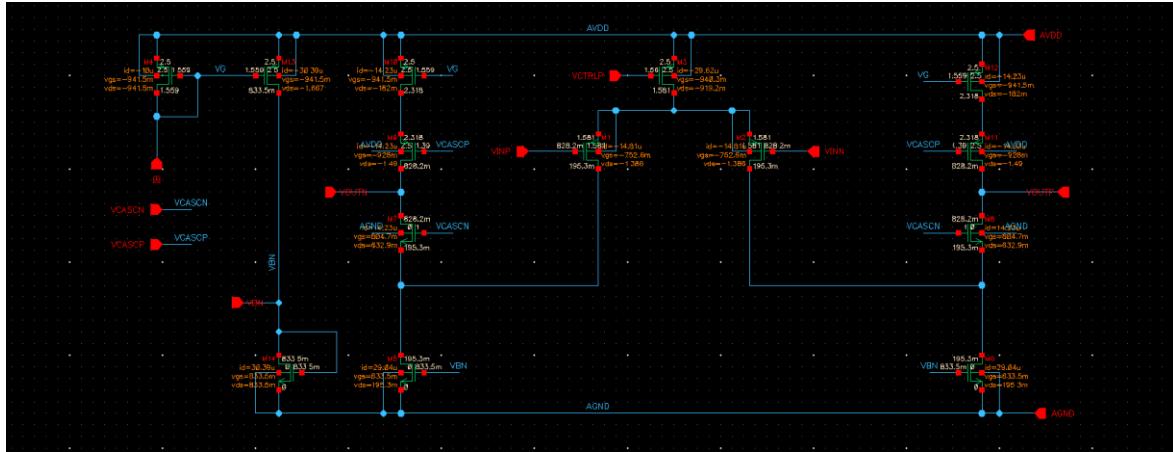
To calculate PM:  $PM = 180 - 99.5 = 80.5^\circ$ .



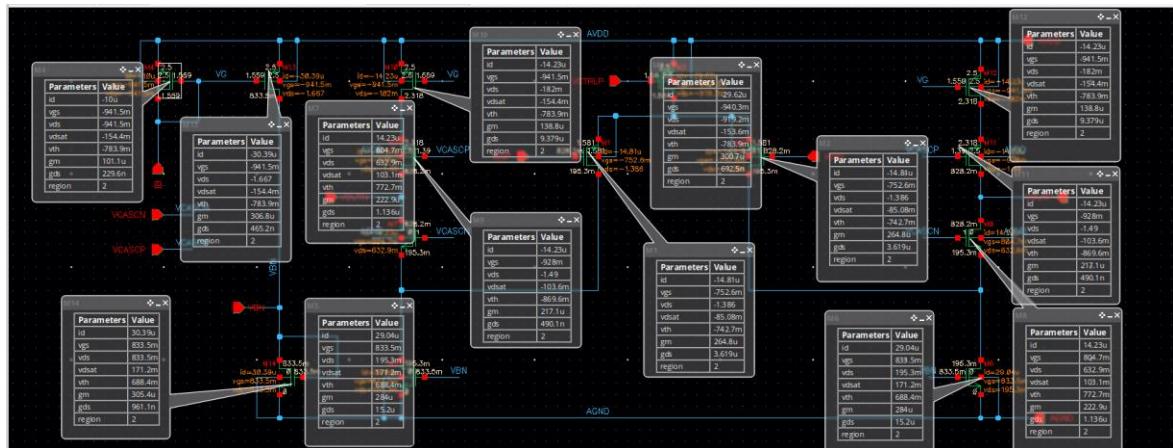
## PART 5: Closed Loop Simulation (AC and STB Analysis):

- 1) Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop configuration.

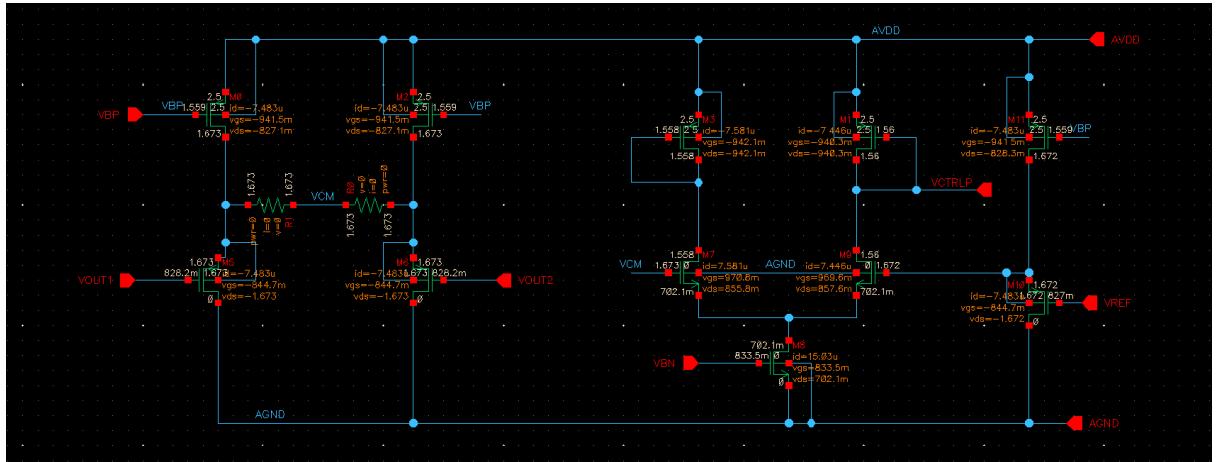
Schematic of OTA with DC node voltages:



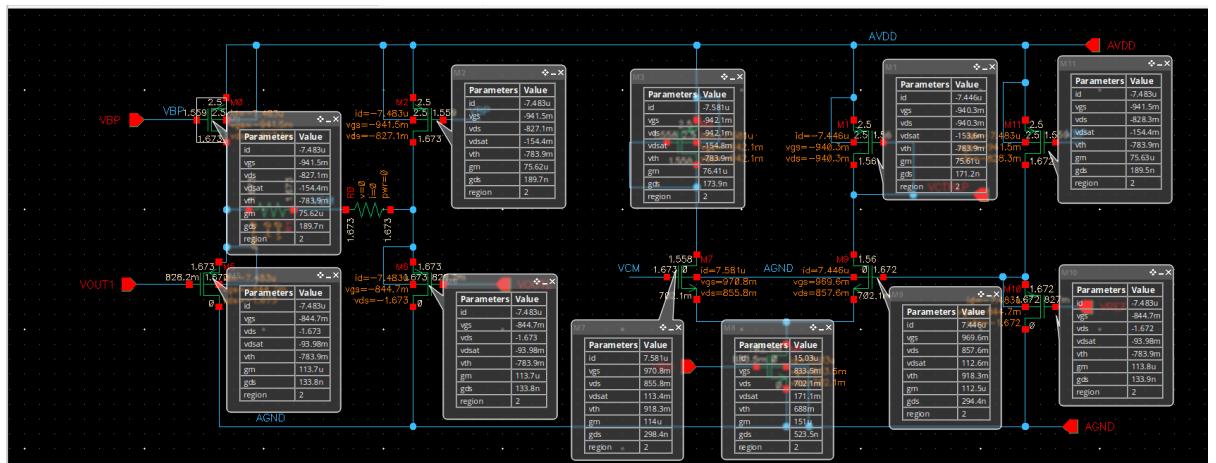
Schematic of OTA with transistors DC OP:



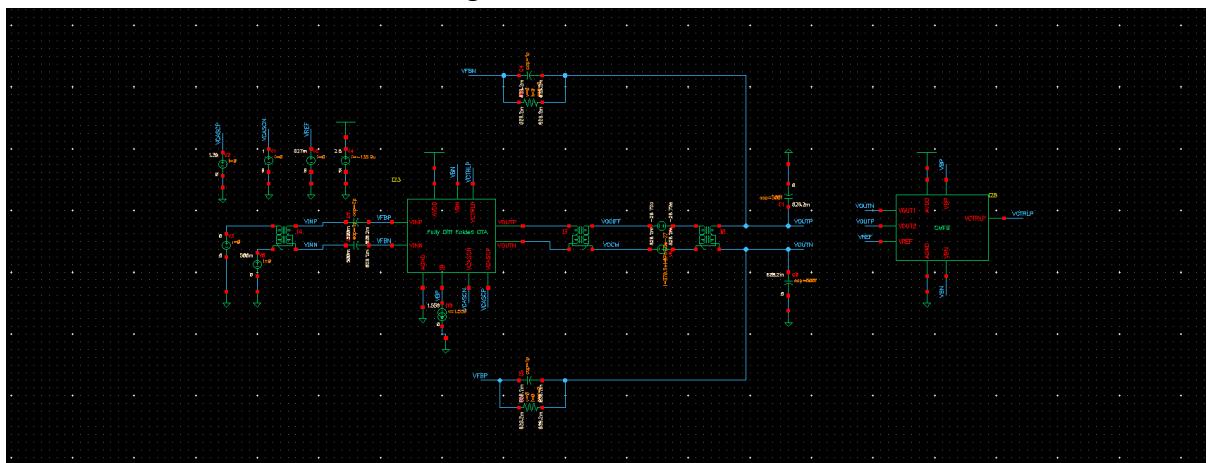
Schematic of CMFB with DC node voltages:



Schematic of CMFB with transistors DC OP:



Schematic of TB with DC node voltages:



➤ **What is the CM level at the OTA output? Why?**

the CM level at the OTA output is 828.2mV which is very close from Vref=827mV and this error is because the error amplifier doesn't have high gain.

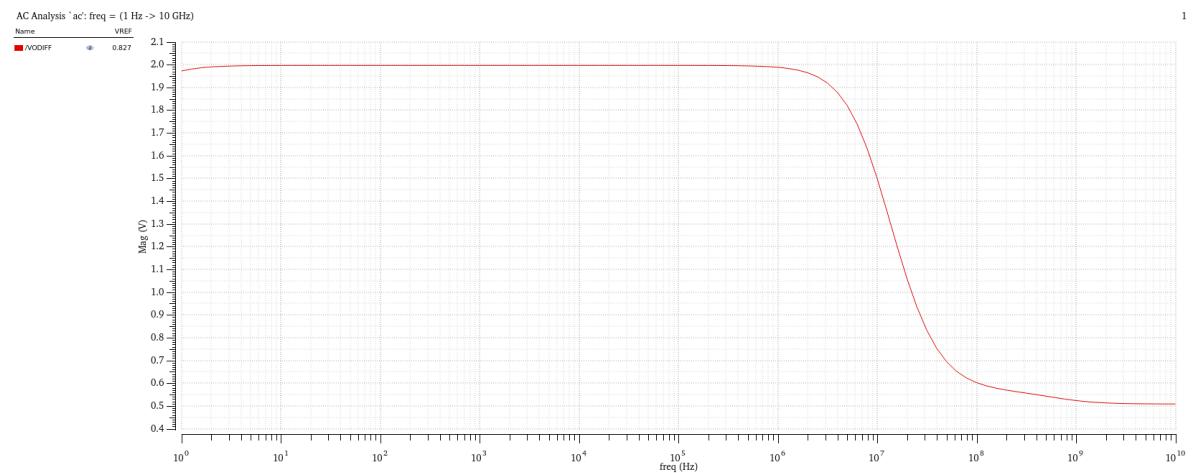
➤ **What is the CM level at the OTA input? Why?**

The CM level at the OTA input is 828.2mV which equals the CM level at the OTA output as we set the DC input node by a very high resistance which makes the input has the same DC.

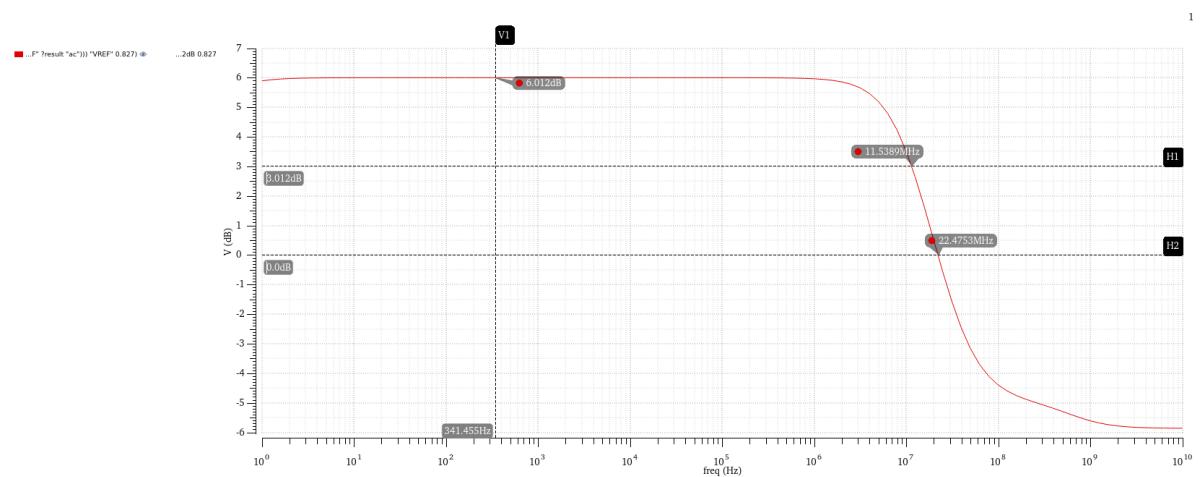
**2) Differential closed-loop response:**

➤ **Plot VODIFF vs frequency**

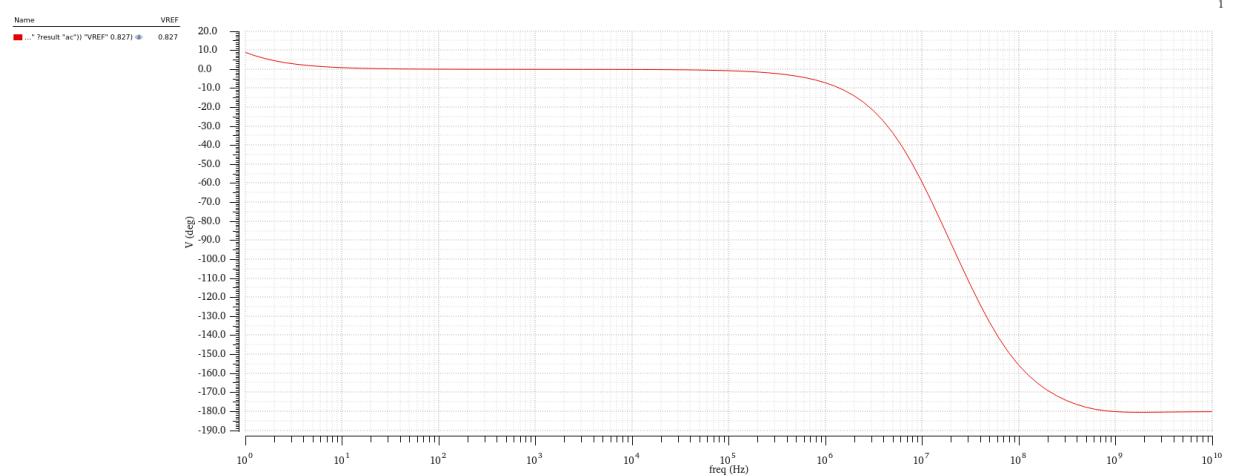
Magnitude:



Magnitude in dB:



Phase:



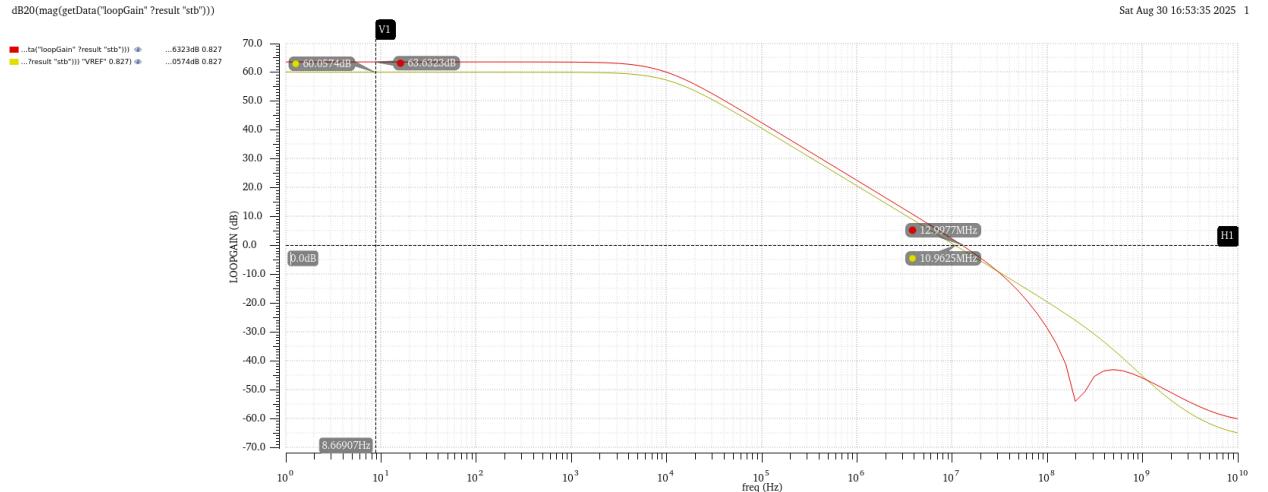
➤ Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_labs:Lab_11_TB_CL:1	Ao	1.998			
ITI_labs:Lab_11_TB_CL:1	Ao_dB	6.012			
ITI_labs:Lab_11_TB_CL:1	BW	11.88M			
ITI_labs:Lab_11_TB_CL:1	UGF	22.56M			
ITI_labs:Lab_11_TB_CL:1	GBW	23.5M			

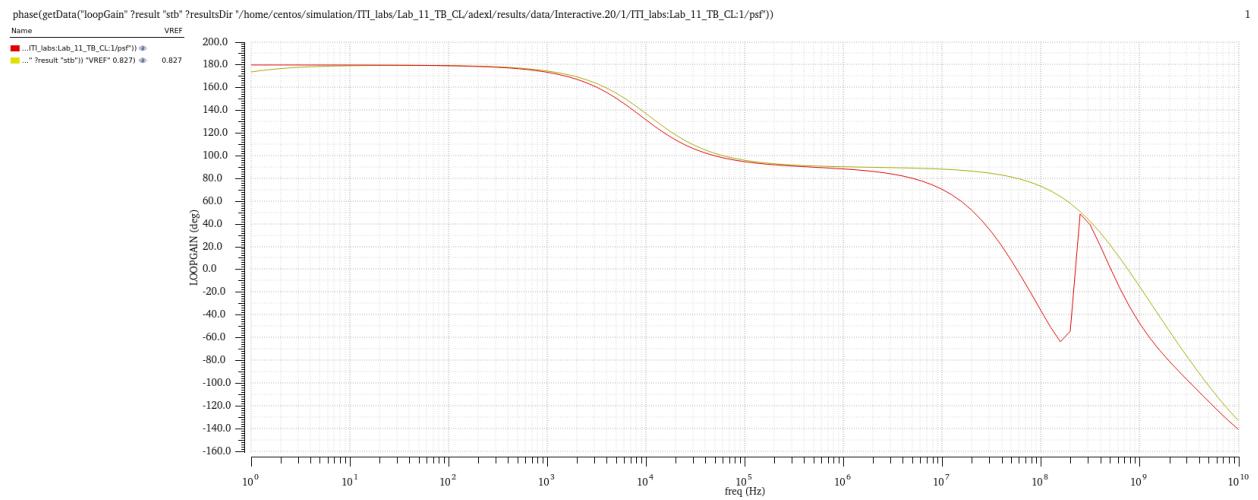
### 3) Differential and CMFB loops stability (STB analysis):

Plot loop gain in dB and phase vs frequency for the two simulations overlaid

LG in dB



## Phase:



### ➤ Compare GBW and PM of diff and CM loops. Comment.

Diff:

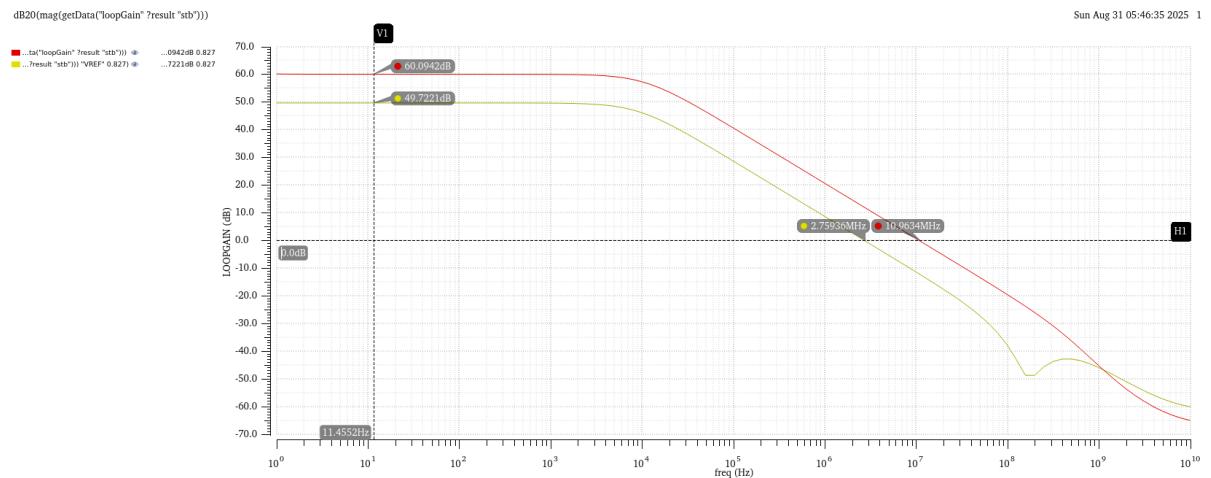
ITI_labs:Lab_11_TB_CL:1	Phase Margin	88.2			
ITI_labs:Lab_11_TB_CL:1	gainBwProd(getData("loopGain"...	10.8M			

CM:

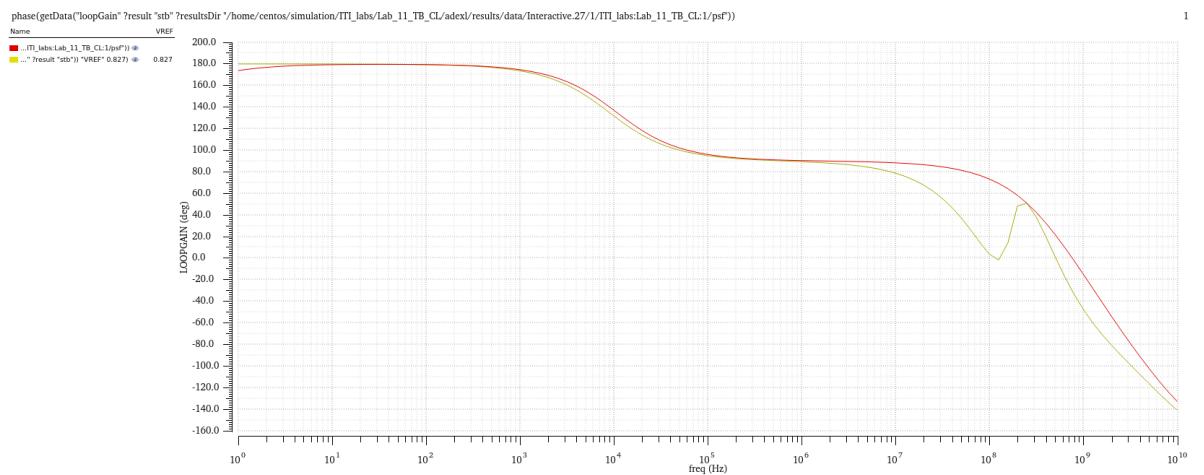
ITI_labs:Lab_11_TB_CL:1	Phase Margin	65.04			
ITI_labs:Lab_11_TB_CL:1	gainBwProd(getData("loopGain"...	13.62M			

- We can see that the phase margin isn't achieved so we will make vctrlp controls only 20% of the current which will reduce the CM LG to 20% and will increase the PM a lot.

LG in dB:



### Phase:



### CM updated PM and GBW:

ITI_labs:Lab_11_TB_CL:1	Phase Margin	87.1	
ITI_labs:Lab_11_TB_CL:1	gainBwProdgetData("loopGain" ...	2.753M	

### Comparison:

		Diff	CM
GBW	10.8MHz	2.753MHz	
PM	88.2°	87.1°	

### Comment:

The differential LG is achieved it is higher than 60dB. The PM of the both loops is higher than 70. The GBW of the CM loop was higher than the Diff as it is gain was the gain of two stages but when we decreased LG by 20% the GBW decreased to almost 20% so it became less than the diff GBW.

- **Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation. Comment.**

		Diff loop	Open loop
Gain	1011	3205	
GBW	10.8MHz	67.49MHz	

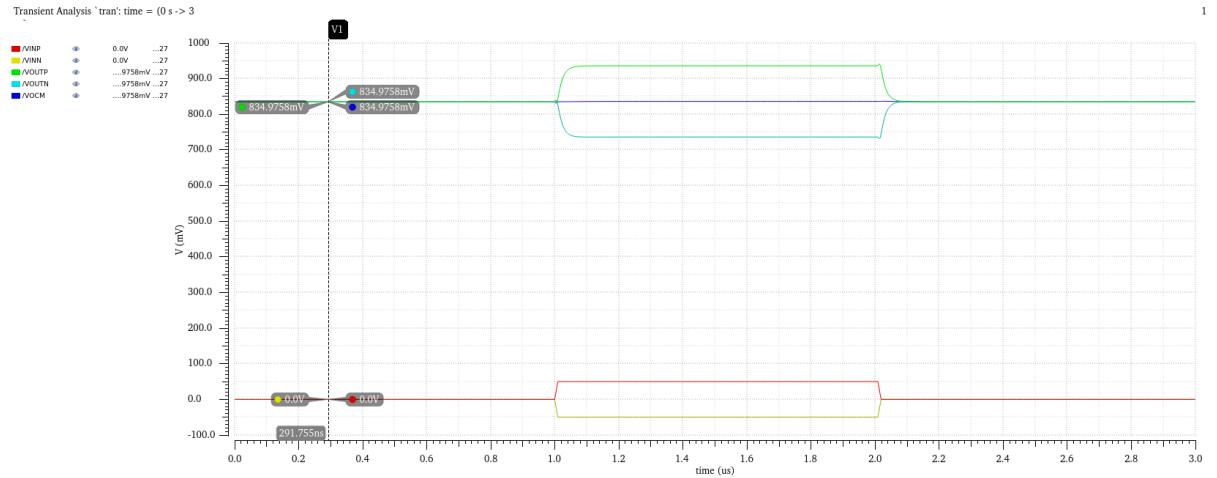
### Comment:

The LG is one third of the open loop gain as  $\beta_v = \frac{C_F}{C_F + C_{in}} = \frac{1}{3}$ . BW also will decrease because of the loading increasing COUT so GBW decreased to 1/6.

## PART 6: Closed Loop Simulation (Transient Analysis):

### 1) Differential and CMFB loops stability (transient analysis):

- Plot the transient signals at **VINP**, **VINN**, **VOUTP**, **VOUTN**, and **VOCM** overlaid in the same figure.



- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

No, there is no ringing at both loops as  $PM > 76$ . Yes, the loops are stable with adequate PM.

- Calculate the 1% settling time and compare it to the required specification. If the specification is not satisfied, what design changes could be a possible solution?

ITI\_labs:Lab\_11\_TB\_CL:1 riseTime(VT("VOUTP")) 0.83497...

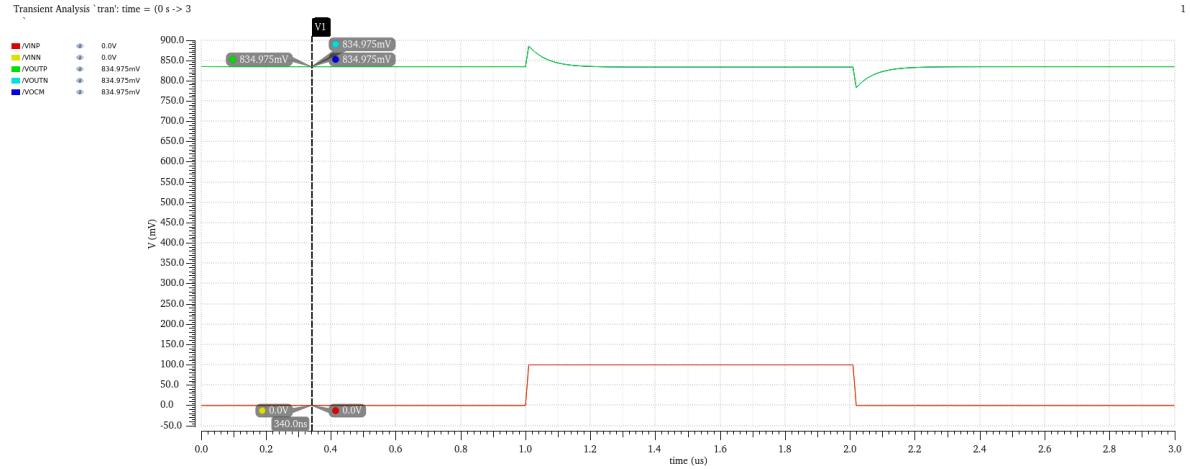
74.15n

	designed	required
Settling time	74.15ns	$\leq 100ns$

The specification is satisfied but if not a solution would be to increase the current then increase gm of input pair and then GBW and the Acl is constant so we increased the BWcl which will decrease the settling time.

## 2) Differential and CMFB loops stability (transient analysis):

- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure

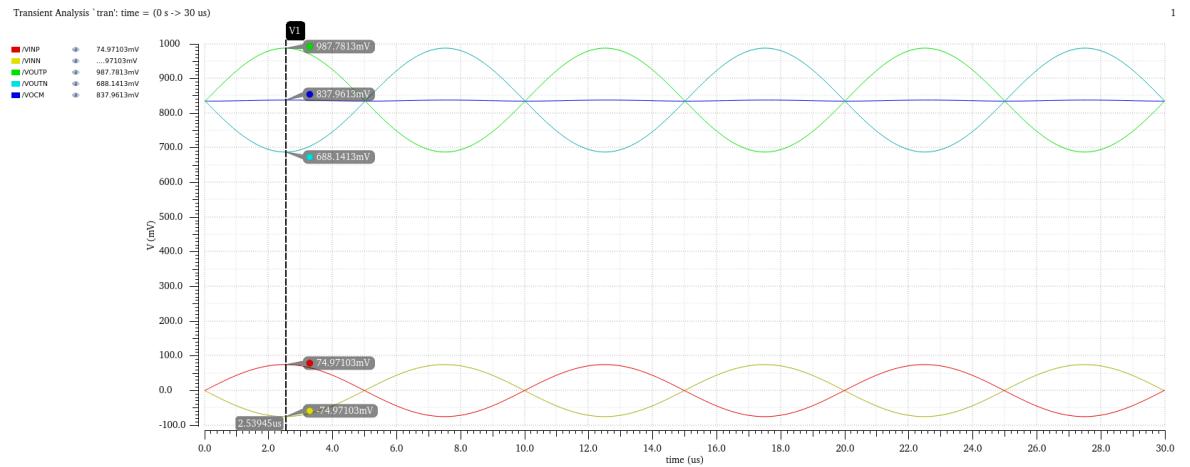


- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

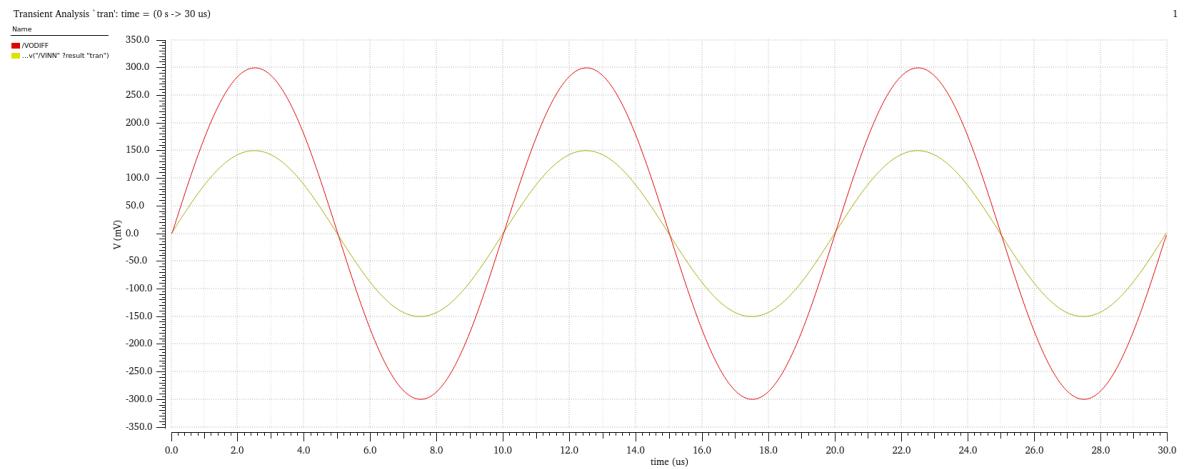
No, there is no ringing at both loops as PM>76. Yes, the loops are stable with adequate PM.

## 3) Output swing:

- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



- Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure



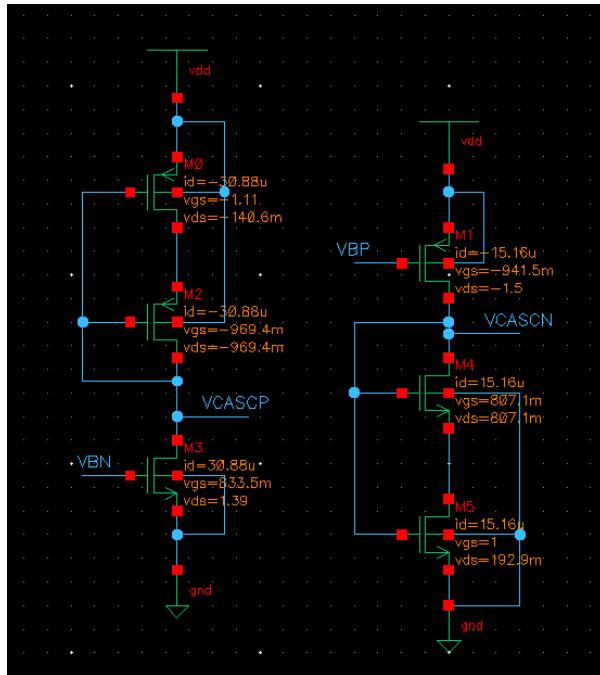
- Calculate the diff input and output peak-to-peak swings and the closed loop gain

ITI_labs:Lab_11_TB_CL:1	peakToPeak((v("/VINP")?result "t...))	300m
ITI_labs:Lab_11_TB_CL:1	peakToPeak(VT("/VODIFF"))	599.4m

$$Acl = \frac{V_{odiff}}{V_{idiff}} = 1.998$$

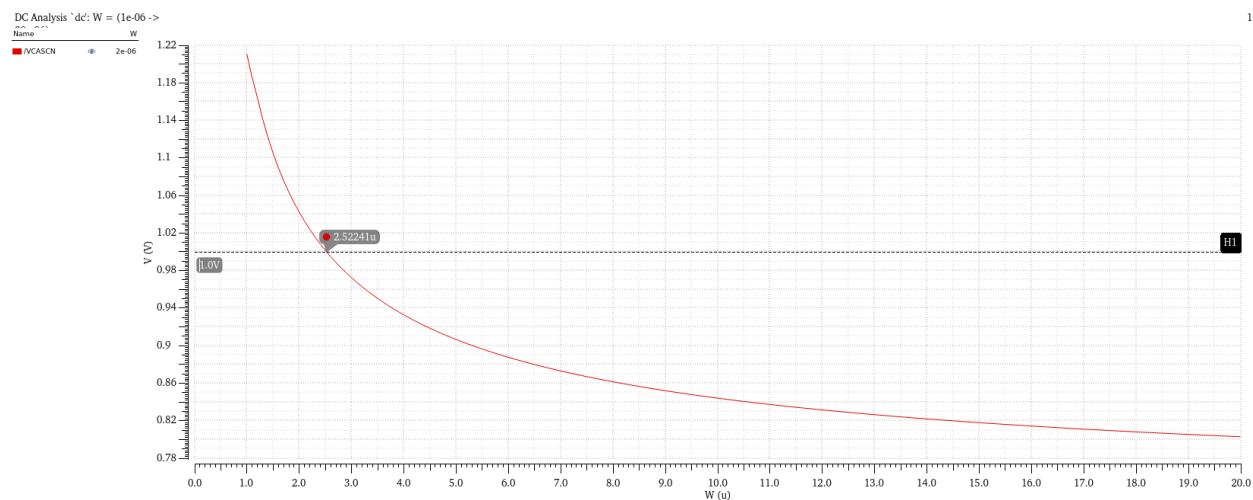
## Bonus Part:

- **Schematic:**



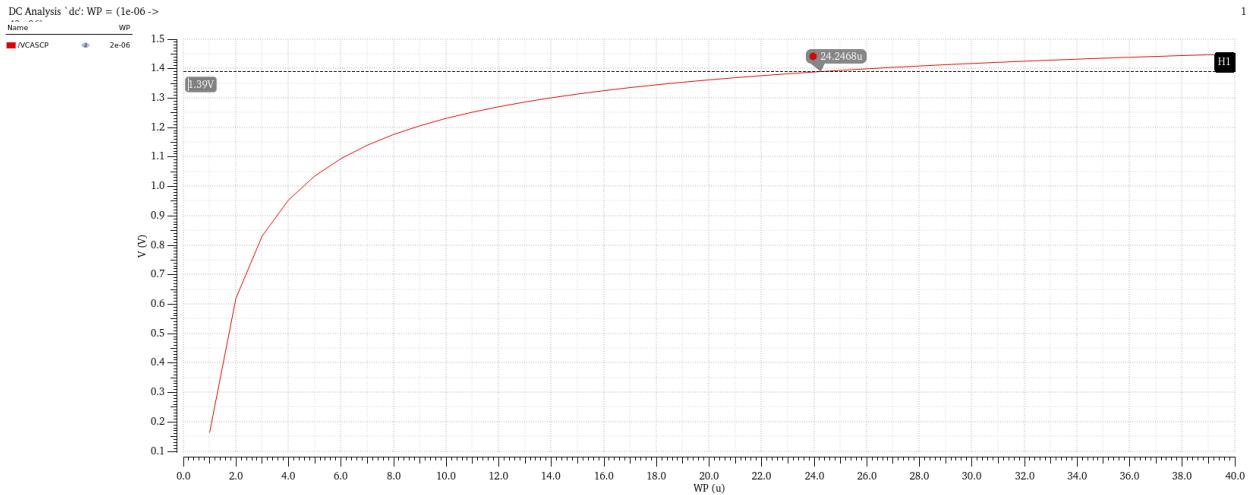
### For VCASCN :

- for M1 We want it to match PMOS current mirror so we will give it the same sizing.
- for M4 We will match it with nmos cascode.
- for M5 we assume it is  $L = 1\text{um}$  and sweep on it is  $W$  to get value which make Vcascn we want.

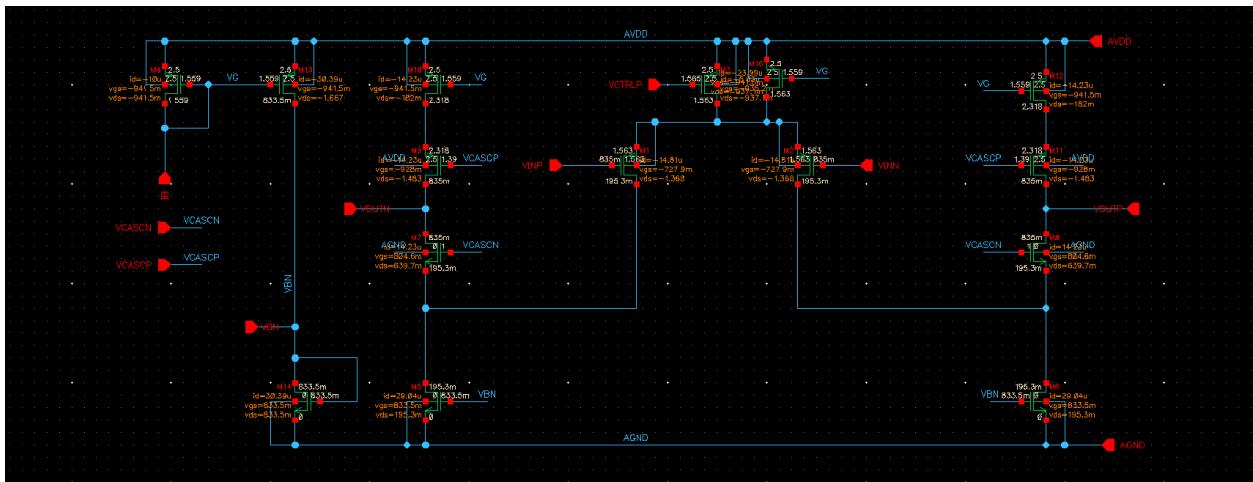


## For VCASCP:

- for M3 We want it to match NMOS current mirror so we will give it the same sizing
  - for M2 We will match it with pmos cascode.
  - for M0 we assume it is  $L = 1\text{um}$  and sweep on it is  $W$  to get value which make  $V_{cascp}$ .



- **OP result:**



- We note that it is almost the same OP and this change is because we splitted the tail current source when we were solving the CM PM problem.

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_labs:Lab_11_TB_CL:1	Ao	1.998			
ITI_labs:Lab_11_TB_CL:1	Ao_dB	6.012			
ITI_labs:Lab_11_TB_CL:1	BW	11.88M			
ITI_labs:Lab_11_TB_CL:1	UGF	22.56M			
ITI_labs:Lab_11_TB_CL:1	GBW	23.5M			