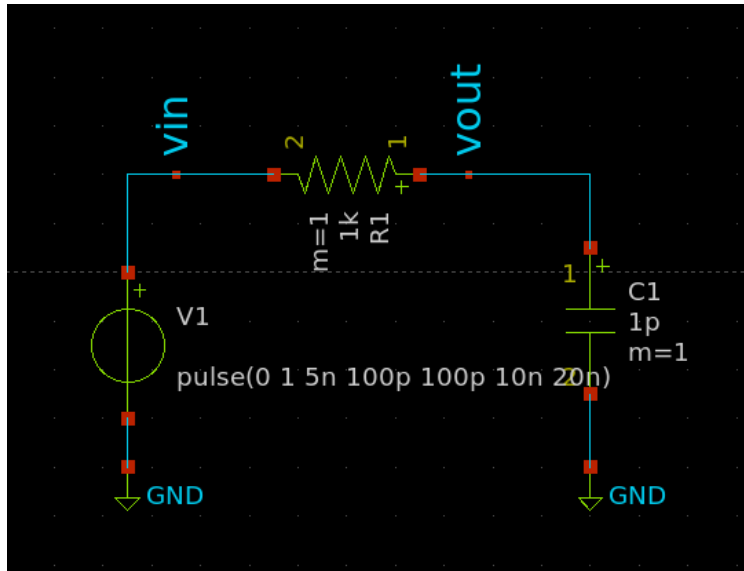


Lab 01

PART 1: Low Pass Filter Simulation (LPF):

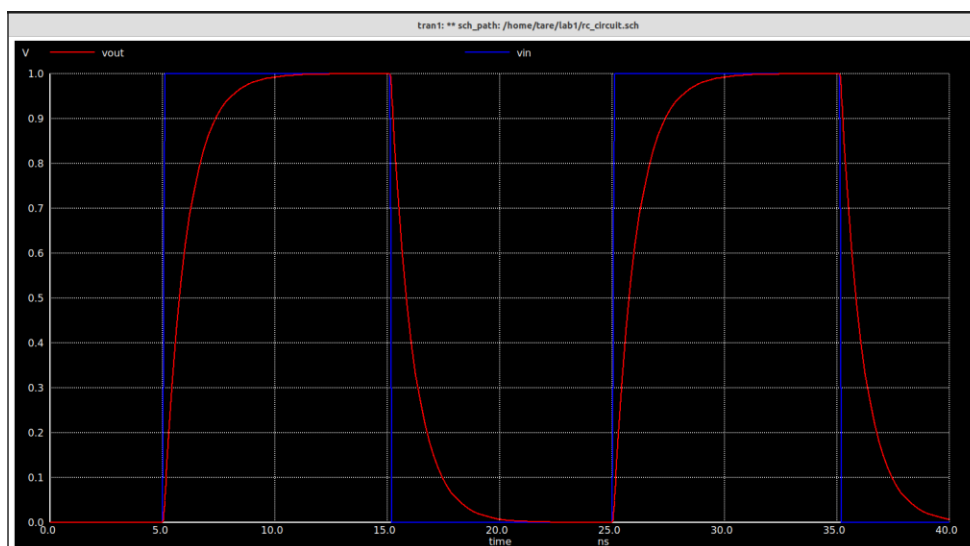
1. Transient Analysis:

- **Schematic:**



To get value of C we know that $\tau = RC$ then $C = 1 \text{ pF}$

- **Results:**



- **Rise and Fall time:**

```

RC_circuit.spice" -a || sh

Note: No compatibility mode selected!

Circuit: ** sch_path: /home/tare/lab1/rc_circuit.sch
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Initial Transient Solution
-----

Node                Voltage
----                -
vout                 0
vin                  0
v1#branch             0

No. of Data Rows : 240
t_rise               = 2.194799e-09 targ= 7.350398e-09 trig= 5.155599e-09
t_fall                = 2.190539e-09 targ= 1.744592e-08 trig= 1.525538e-08
binary raw file "RC_circuit.raw"
ngspice 1 ->

```

➤ **In a text file:**

```

1 t_rise = 2.194799e-09
2 t_fall = 2.190539e-09

```

➤ **Analytical Solution:**

Capacitor equation while charging is $v(t) = v_{max} * (1 - e^{-\frac{t}{RC}})$

At 10% $0.1 = (1 - e^{-\frac{t}{RC}})$ then $t1 = 0.10536 \text{ nS}$

At 90% $0.9 = (1 - e^{-\frac{t}{RC}})$ then $t2 = 2.30258 \text{ nS}$

Then $Trise = t2 - t1 = 2.197 \text{ ns}$

Similarly, capacitor discharging equation is $v(t) = v_0 * e^{-\frac{t}{RC}}$

At 90% $0.9 = e^{-\frac{t}{RC}}$ then $t1 = 0.10536 \text{ nS}$

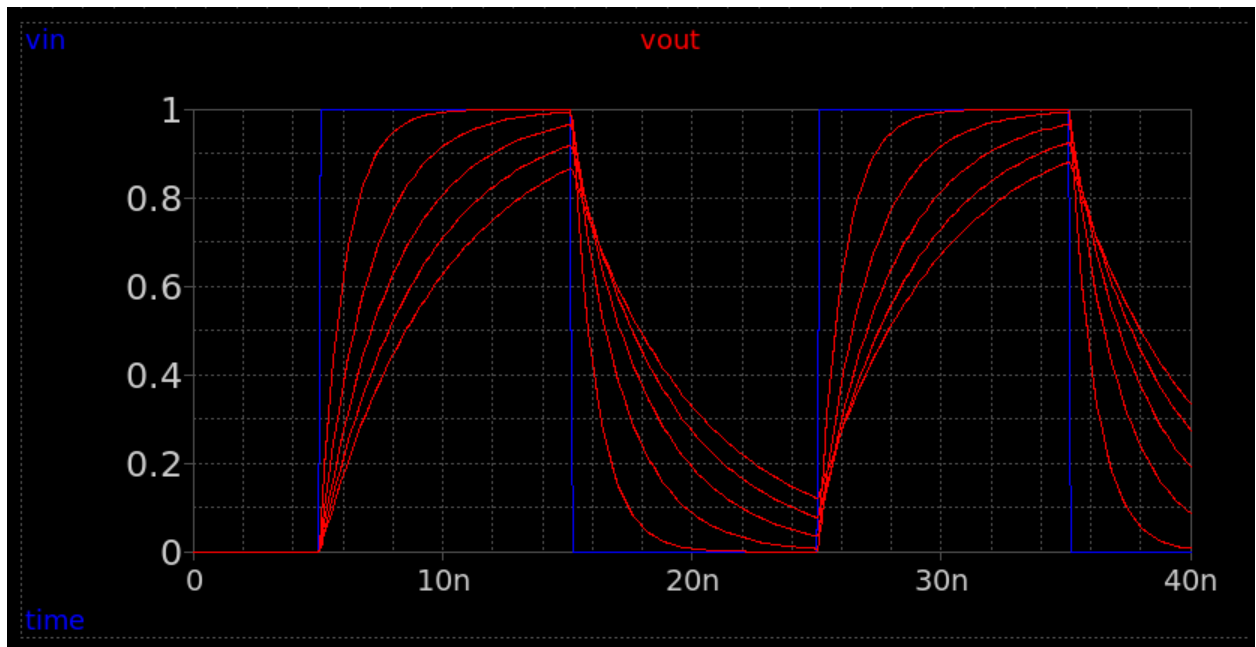
At 10% $0.1 = e^{-\frac{t}{RC}}$ then $t2 = 2.30258 \text{ nS}$

Then $Tfall = t2 - t1 = 2.197 \text{ ns}$

➤ **Comparison:**

	Analytical solution	Simulation
Rise Time	2.197 ns	2.1947 ns
Fall Time	2.197 ns	2.1905 ns

- **parametric sweep for $R = 1: 1: 5k\Omega$:**



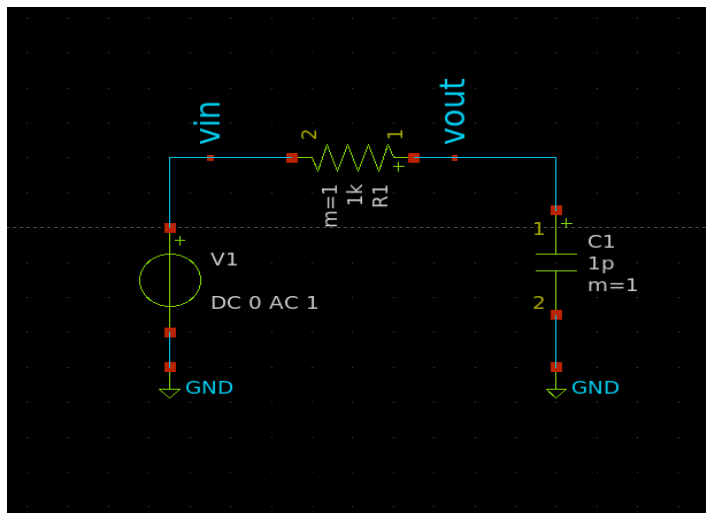
Comment:

As we expected the T_{rise} and T_{fall} increase linearly with the increment of R as $\tau = RC$. The rise and fall time between is approximately $t = 2.2 RC$ and the simulation meets the equation.

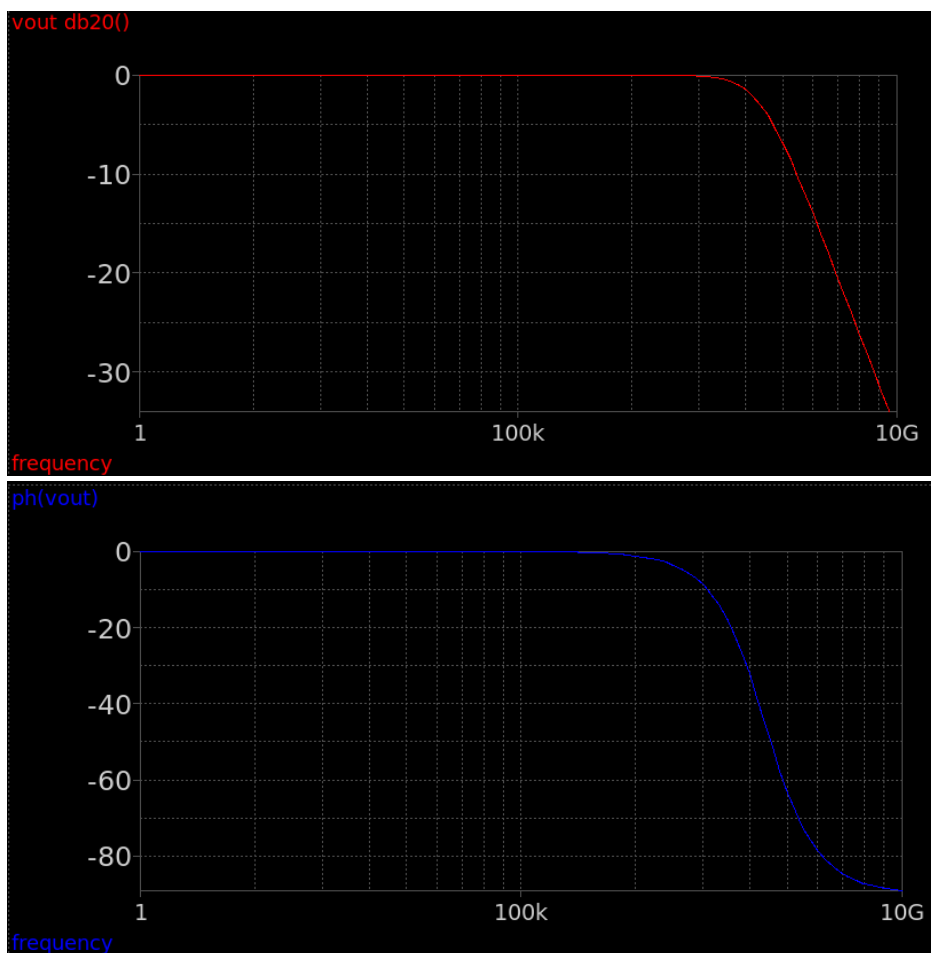
Note: In the $\tau = 5ns$ we couldn't calculate rise time as it didn't reach 90% of v_{max} .

2. AC Analysis:

- **Schematic:**



- **Bode Plot magnitude and phase:**



- **DC gain and 3dB bandwidth:**

```

ac_result.txt
~/xschem/simulations
1 max_gain = 1.000000e+00
2 bw = 1.592554e+08

```

➤ **Analytical Solution:**

DC gain is calculated at frequency = 0 then the capacitor is open circuit the $v_{out} = v_{in}$

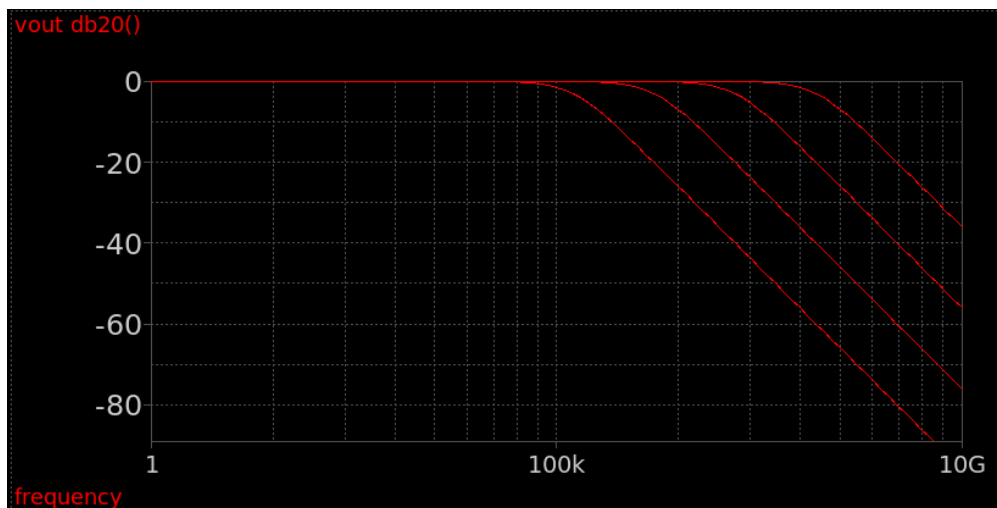
And $Gain = \frac{v_{out}}{v_{in}} = 1$

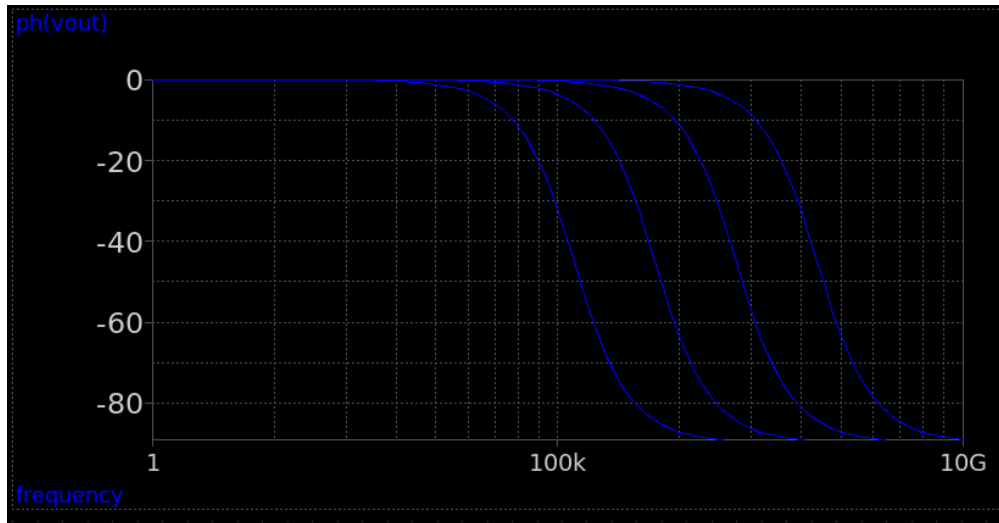
Bandwidth frequency $f = \frac{1}{2\pi RC} = 159.15 \text{ MHz}$

➤ **Comparison:**

	Analytical solution	Simulation
DC gain	1	1
BW	159.15 MHz	159.25MHz

- **parametric sweep for $R = 1, 10, 100, 1000k\Omega$:**





```

ac_result.txt
~/xschem/simulations
Open [ ] Save [ ] [X]
1 const.r_val = 1.000000e+03
2 ac1.max_gain = 1.000000e+00
3 ac1.bw = 1.592554e+08
4 const.r_val = 1.000000e+04
5 ac2.max_gain = 1.000000e+00
6 ac2.bw = 1.592554e+07
7 const.r_val = 1.000000e+05
8 ac3.max_gain = 1.000000e+00
9 ac3.bw = 1.592554e+06
10 const.r_val = 1.000000e+06
11 ac4.max_gain = 1.000000e+00
12 ac4.bw = 1.592554e+05

```

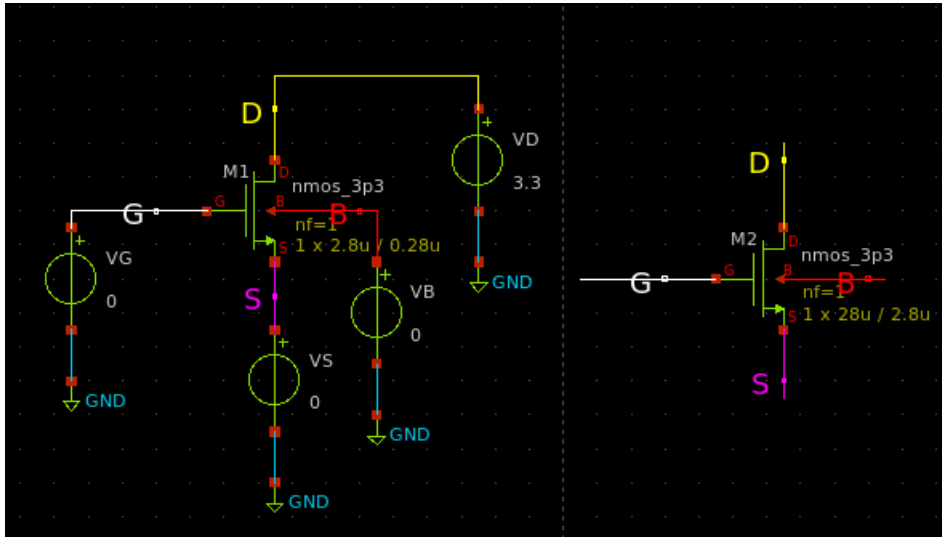
Comment:

We notice that when we increase the Resistance the Bandwidth decreases as $BW = \frac{1}{2\pi RC}$ so when multiply R by 10 the BW to 10% of its value.

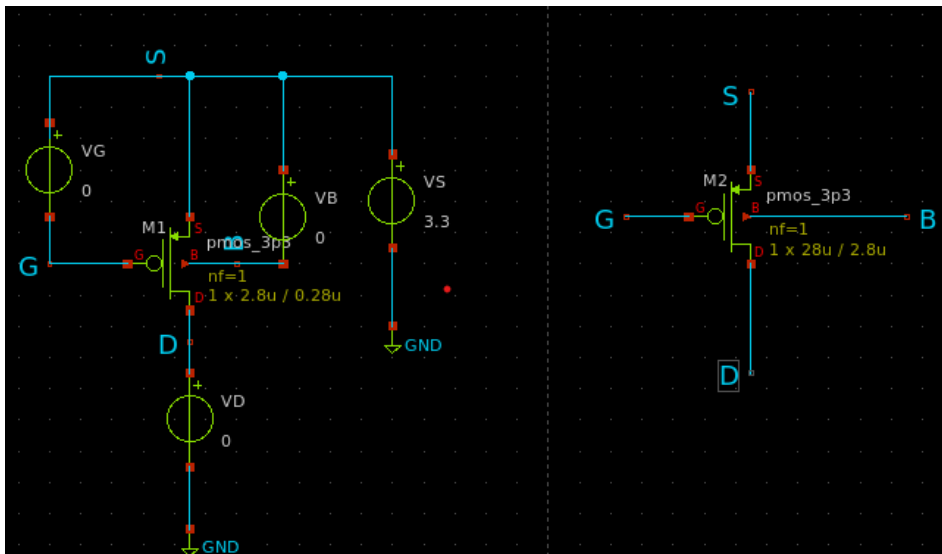
Part 2: MOSFET Characteristics:

- **Schematic:**

- **NMOS:**

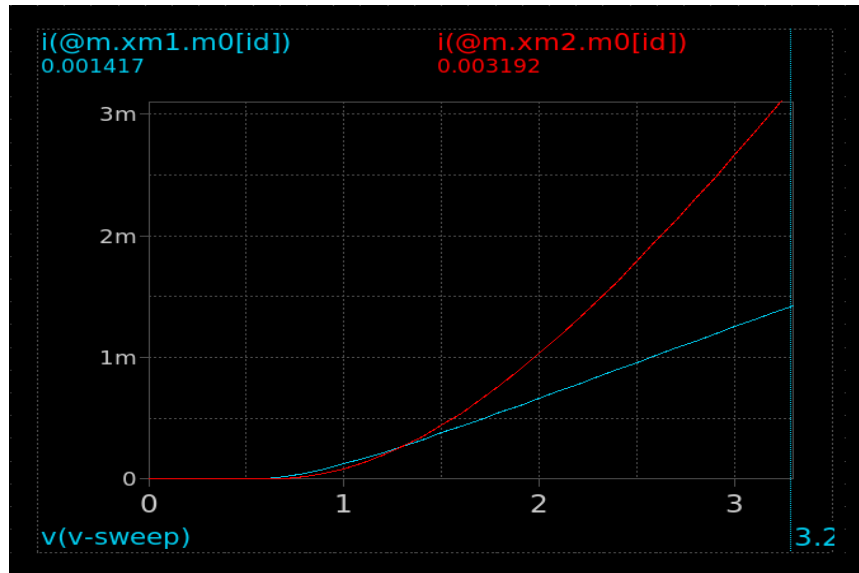


- **PMOS:**

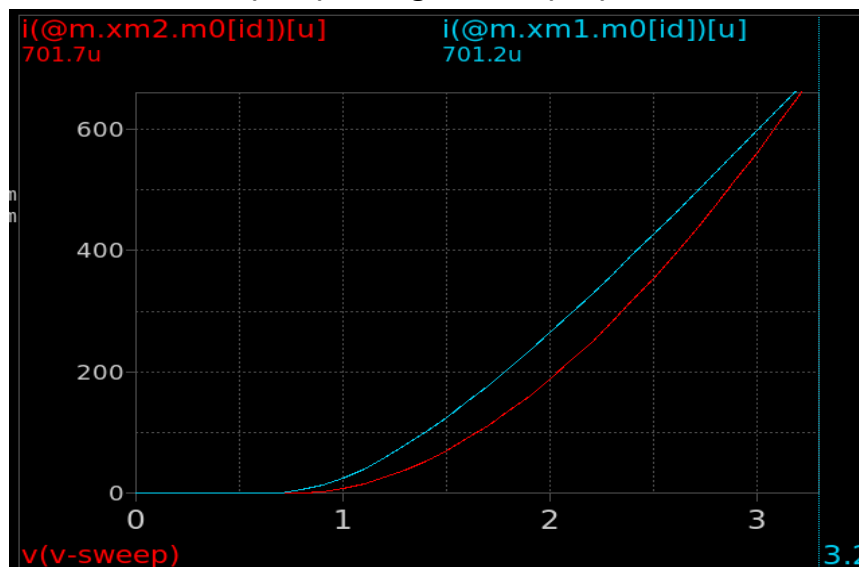


1- ID VS VGS:

➤ Short channel (blue) vs long channel (red) in NMOS:



➤ Short channel (blue) vs long channel (red) in PMOS:



Comment on the differences between short channel and long channel results:

- **Which one has higher current? Why?**

In NMOS Long channel MOSFET has higher current as the short channel MOSFET has Short channel Effects like velocity saturation which may saturate the current at a low value if $V_{Dsat} < V_{ov}$ and also the mobility degradation when V_{GS} increase the mobility starts decreasing due to scattering.

In PMOS short channel has a higher current as it is less affected by mobility degradation as its mobility is less than NMOS and also it may doesn't get in velocity saturation that quick as it has a higher VDSsat because of its lower mobility. And it is higher as DIBL increase the current because of decreasing Vth.

- **Is the relation linear or quadratic? Why?**

For Long channel the relation is quadratic and square law is valid but in short channel the relation is linear as in velocity saturation region the current depends linearly on Vov.

Comment on the differences between NMOS and PMOS:

- **Which one has higher current? Why?**

NMOS has higher current as the electrons mobility is usually higher than holes mobility by 2 to 4 times.

- **What is the ratio between NMOS and PMOS currents at VGS = VDD?**

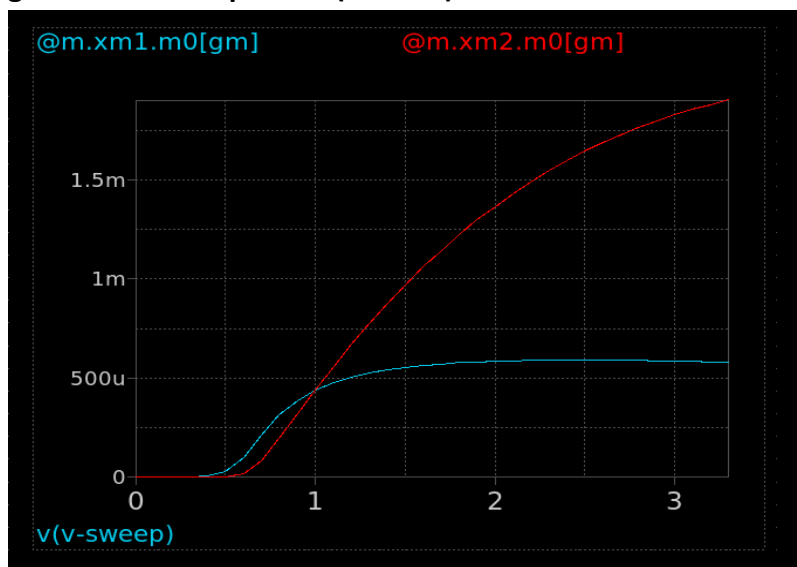
$$the\ ratio = \frac{0.003192}{701.7 \cdot 10^6} = 4.55 \text{ for long and for short } the\ ratio = \frac{0.001417}{701.2 \cdot 10^6} = 2.02$$

- **Which one is more affected by short channel effects?**

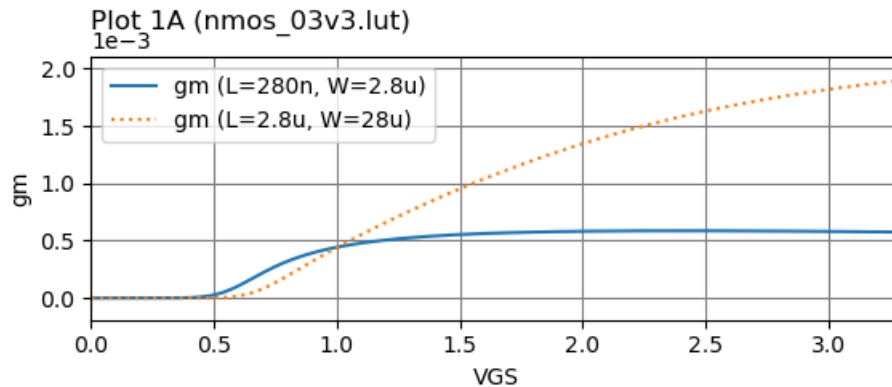
NMOS is more affected by short channel effects

2- gm VS VGS:

➤ **gm overlaid comparison (xschem):**



➤ **gm overlaid comparison (ADT):**



Comment on the differences between short channel and long channel results:

- **Does gm increase linearly? Why?**

For long channel in pinch off saturation region gm increases linearly and then in the triode it starts decreasing as gm is the differentiation of current with V_{GS} and we saw that the current is quadratic in saturation which make gm linear.

For short channel it starts linear for a small time until $V_{DSsat} < V_{ov}$ then it saturates as the current becomes linearly dependent on V_{GS} and may decrease a little due to mobility degradation.

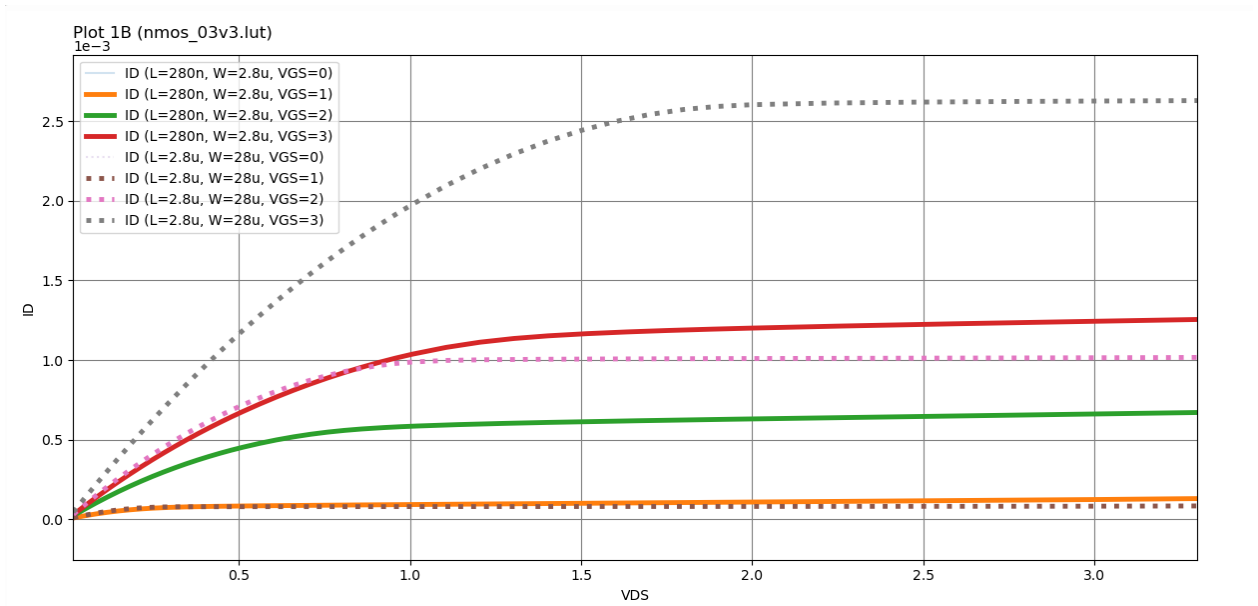
- **Does gm saturate? Why?**

For short channel yes it saturates as current becomes linearly depend on V_{GS} .

But for long channel it still increase until it gets higher gm at the edge of saturation.

3- ID VS VDS:

➤ Results:



Comment on the differences between short channel and long channel results:

- **Which one has higher current? Why?**

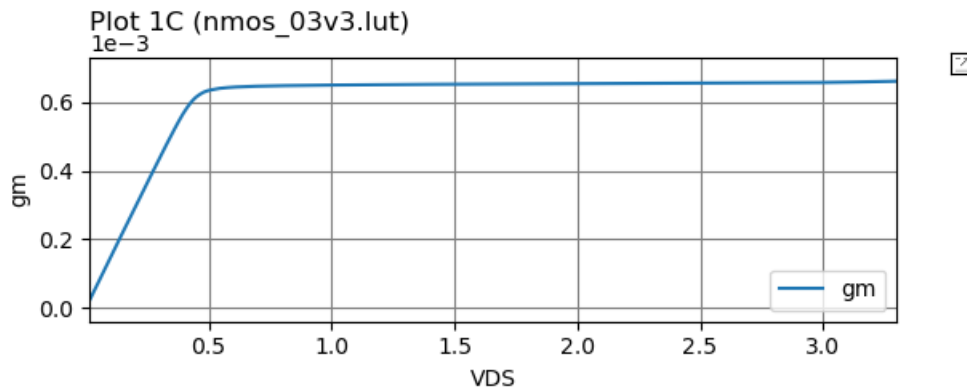
Long channel has higher current as current here has a quadratic relation with V_{GS} so it increases higher than the short channel which has a linear dependence on V_{GS} .

- **Which one has higher slope in the saturation region? Why?**

short channel has higher slope as when we decrease the channel length r_o decreases and we know that the $slope = \frac{1}{r_o}$ so the slope increases

4- [Optional] gm and ro in Triode and Saturation (use ADT):

- gm vs V_{DS} :



- In the first part of the curve, is the relation linear? Why?

yes, it is linear. In this region $V_{DS} < V_{ov}$ which makes it in Triode.

$I = K(V_{ov} * V_{DS} - \frac{V_{DS}^2}{2})$ then $gm = \frac{\partial I}{\partial V_{GS}} = K * V_{DS}$, so it is linear.

- Does gm saturate? Why?

Yes, it saturates. In this region $V_{DS} > V_{ov}$ which makes it in saturation.

$I = K \frac{V_{ov}^2}{2}$ then $gm = \frac{\partial I}{\partial V_{GS}} = K * V_{ov}$, which doesn't depend on V_{DS} so gm saturates.

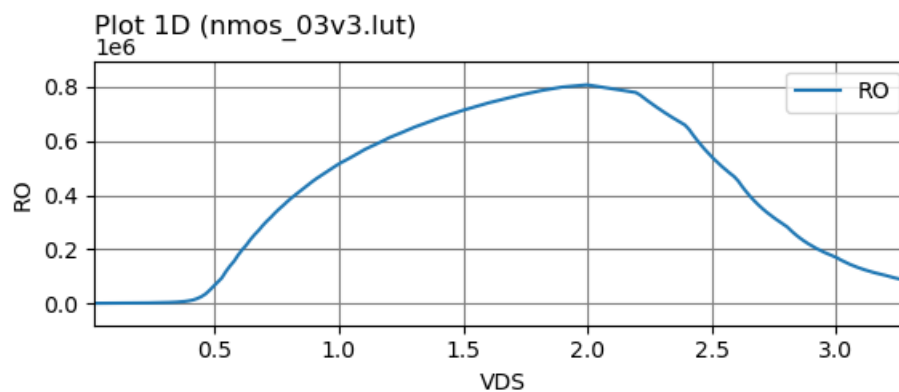
- How much is V_{DS} when the curve saturates?

Around the 0.4 as it is the overdrive voltage.

- Where do you want to operate the transistor for analog amplifier applications? Why?

in the saturation region as gm is higher which gives more gain and it is more stable which makes the circuit linear.

- ro vs V_{DS} :



- **Does r_o saturate just after the transistor enters saturation similar to g_m ? Why?**

No, as r_o depends on V_{DS} r_o increases with the increase of V_{DS} .

- **Does r_o increase if the transistor is biased more into saturation?**

Yes, it does except for high V_{DS} values.

- **Should we operate the transistor at the edge of saturation?**

No, as r_o is very low which reduces the gain and increases the dependency of current on V_{DS} and there are other drawbacks like there is no swing to maintain in saturation.

- **Where do you want to operate the transistor for analog amplifier applications? Why?**

In Saturation region as it has higher gain and g_m VS V_{DS} saturates which makes the circuit more linear.