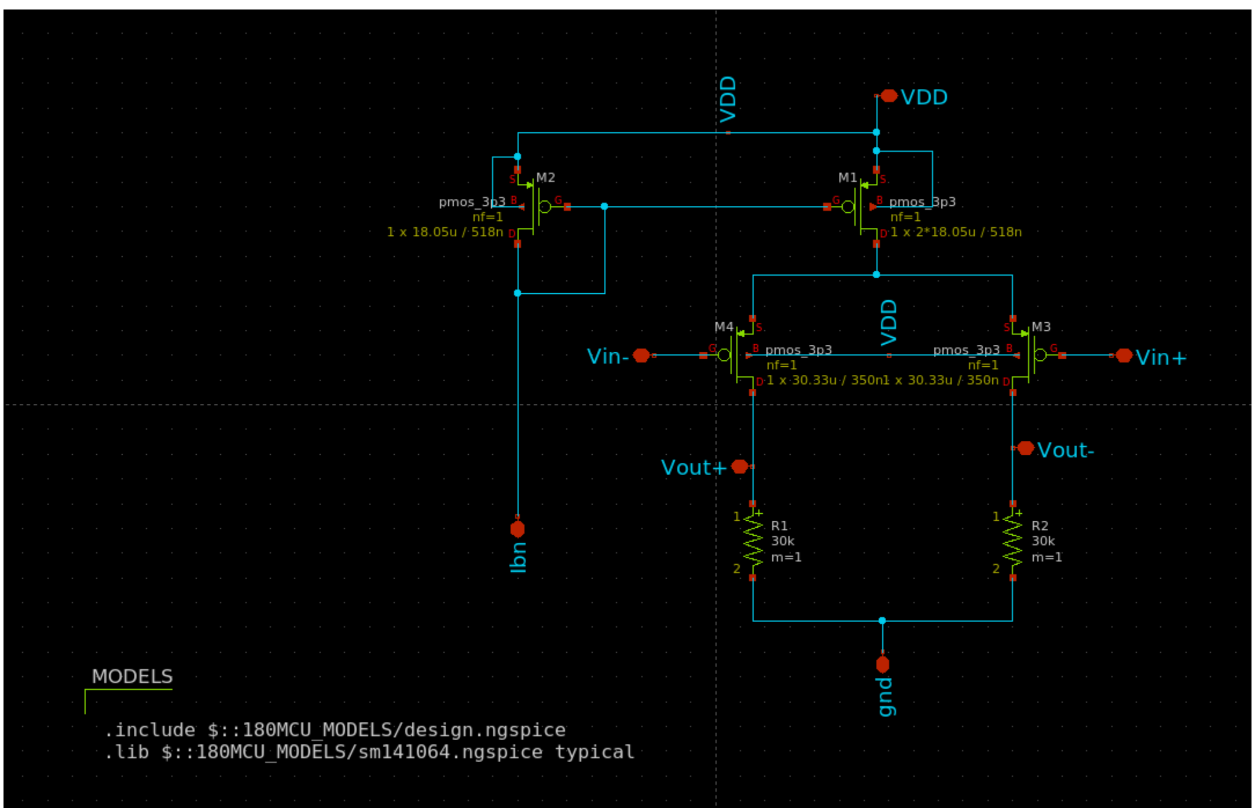
Lab 06

Part 1: Differential Amplifier Design:

- **Specs:**

Parameter	value
VDD	$1.8V$
ISS	$40\mu A$
Differential gain	8
CM output level	0.6
Load capacitance	$1pF$

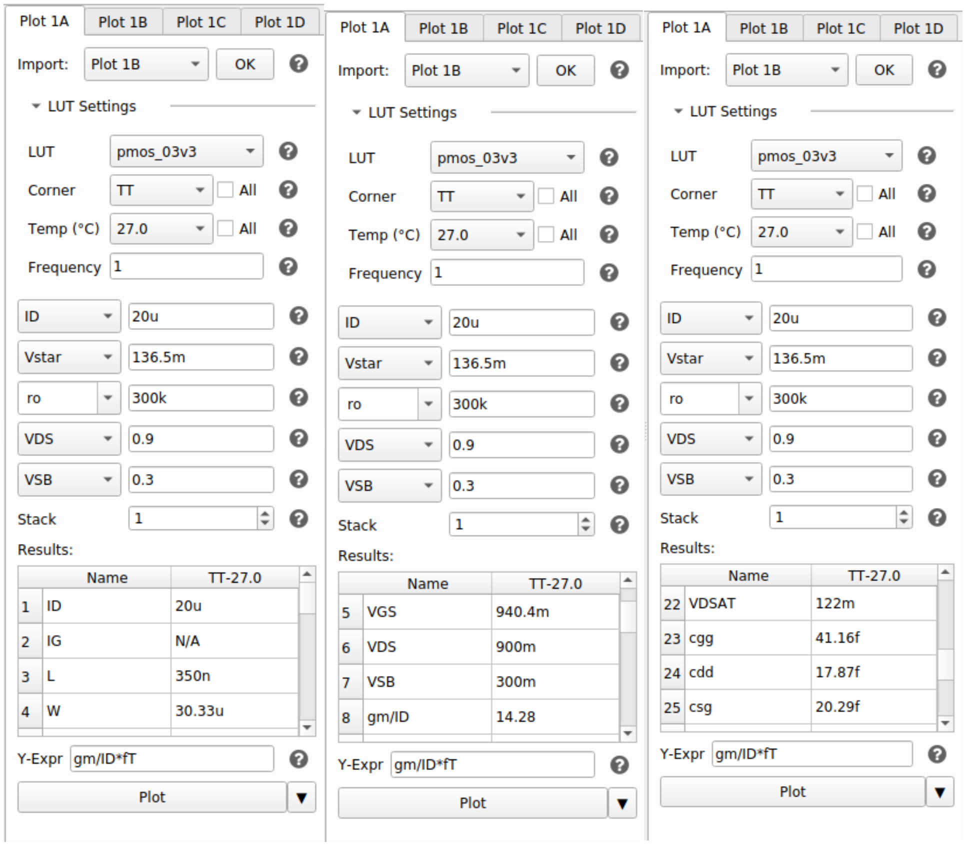
- **Schematic:**



- **Choose RD to meet the CM output level spec:**
  Each branch will have $20\mu A$ then $0.6 = 20\mu A * RD$ then $RD = 30K\Omega$.
- **Choose $V*$ to meet the differential gain spec:**

$$V^* = \frac{1.82*VRD}{Av} = \frac{1.82*0.6}{8} = 136.5mV.$$

- **Assume we will set VDS of the tail current source to $300mV$ to allow more output swing. Report the input pair sizing using SA:**



We got sizing of the input pair: $\frac{W}{L} = \frac{30.33\mu m}{350nm}$ and we got VGS and VDSsat as we will need them I hand analysis.

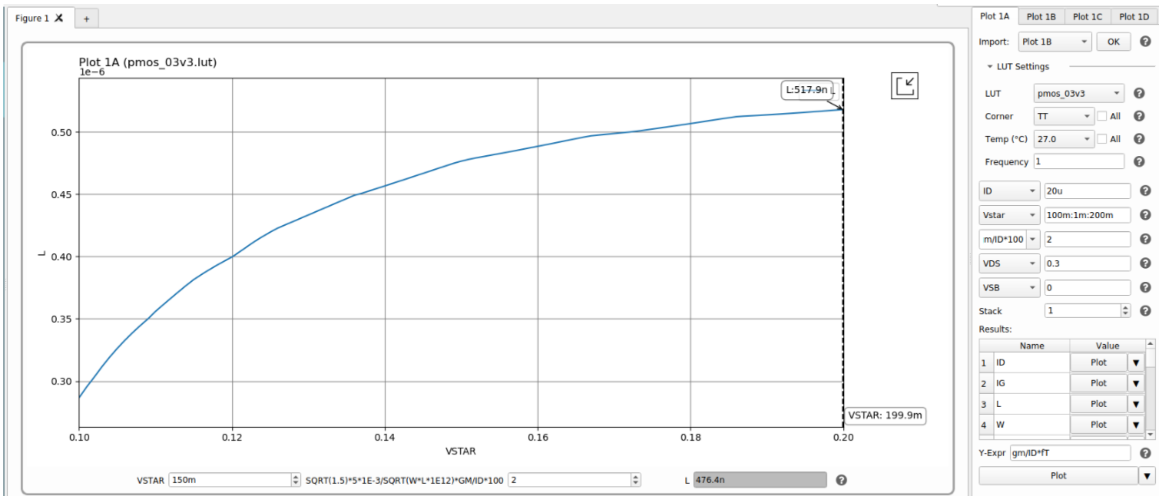
- **Given the above assumption for VDS of the tail current source, calculate the required CM input level:**

$$VCM = -|VGS4| + 1.5 = -0.94 + 1.5 = 560mV$$

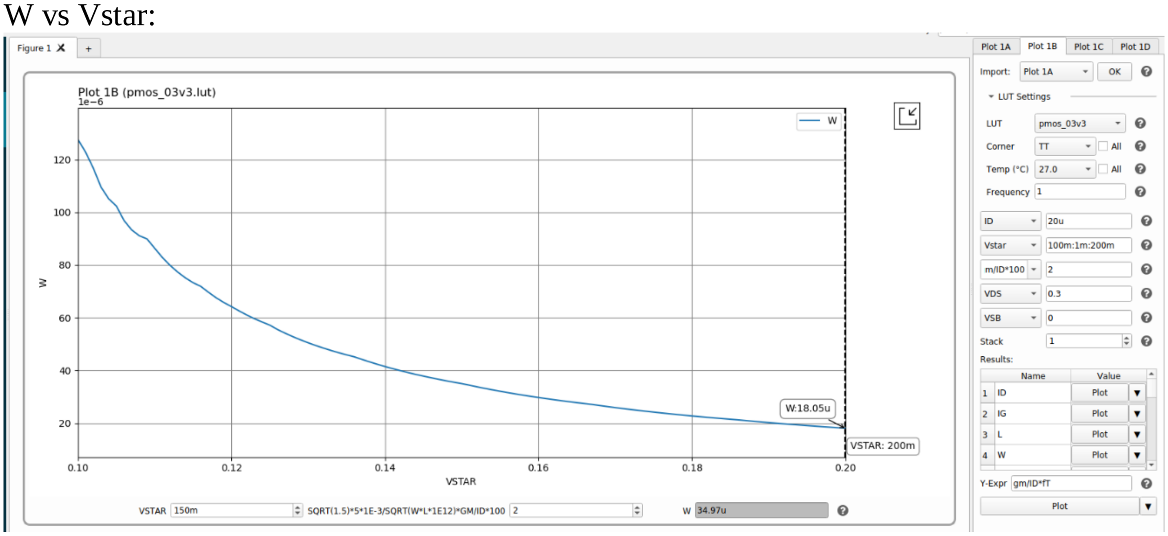
- **Tail current source sizing:**

➢ **Given the compliance voltage spec, report the above figure with a cursor added to the selected design point:**

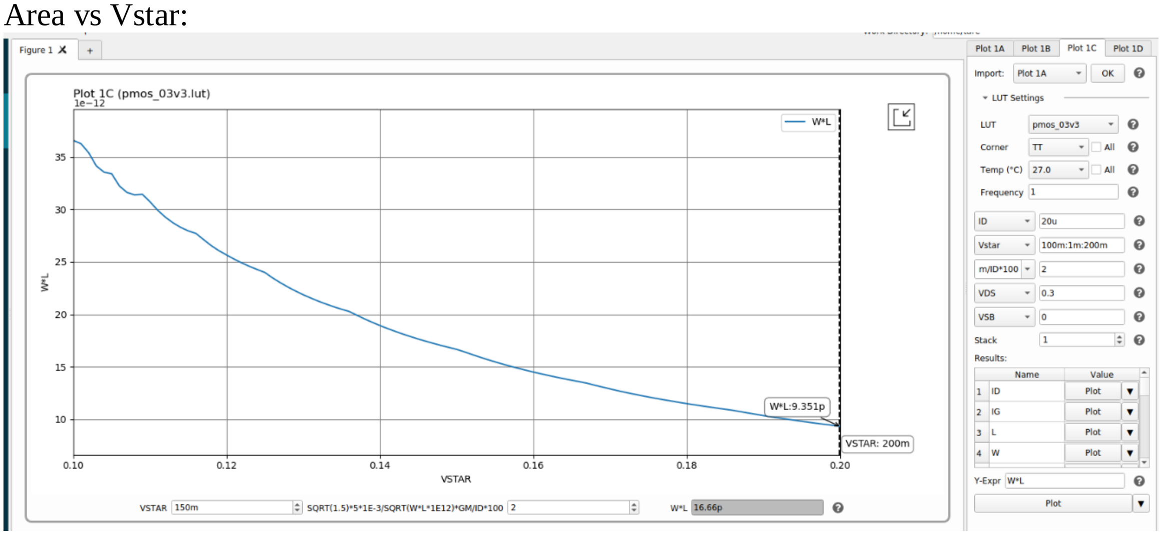
- L vs Vstar:



- W vs Vstar:



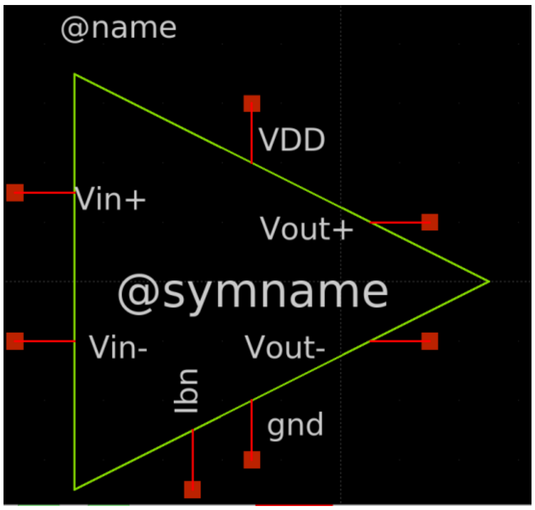
- Area vs Vstar:



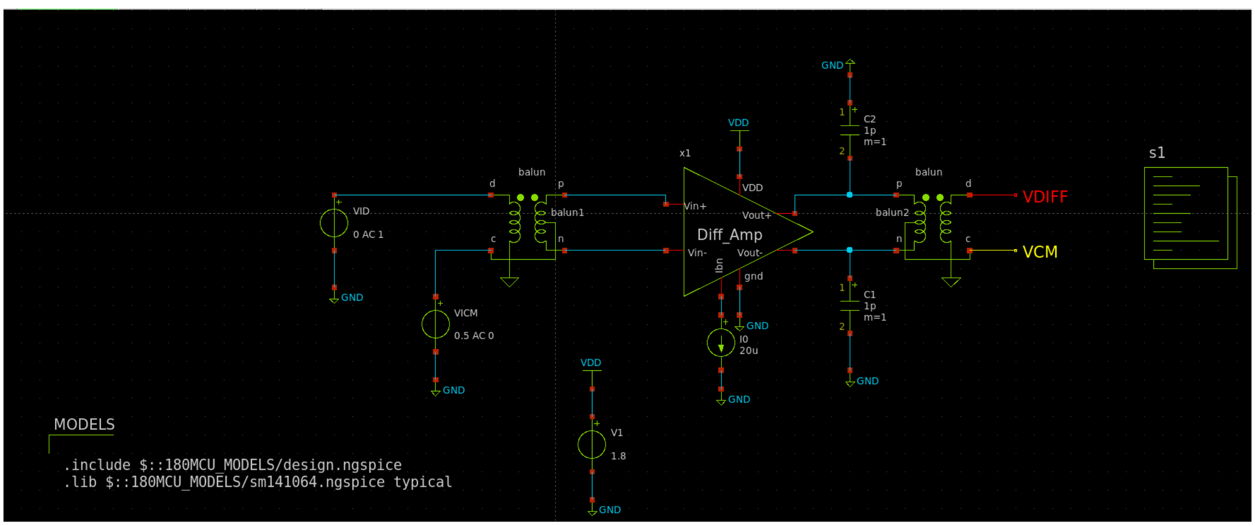
- **Calculate the min and max CM input levels. Is the previously selected CM input level in the valid range:**
  Minimum: $VCMmin = -|VGS4| + |VDsat4| + 0.6 = -0.2184V$.
  Maximum: $VCMmax = -|VGS4| - Vcomp + VDD = 0.66V$.

Part 2: Differential Amplifier Simulation:

- **Differential Amplifier symbol:**



- **Testbench Schematic:**



1) OP simulation:

- **Report a snapshot clearly showing the following parameters:**

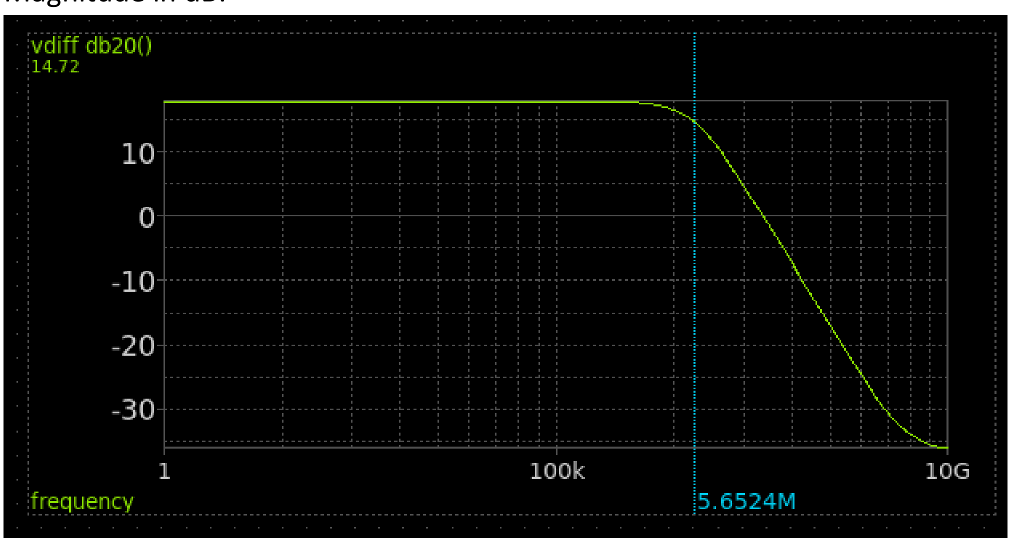
```
     device          m.x1.xm4.m0          m.x1.xm3.m0          m.x1.xm2.m0
      model          pmos_3p3.12          pmos_3p3.12          pmos_3p3.13
         id          1.90478e-05          1.90478e-05                2e-05
         gm          0.000281025          0.000281025          0.000205292
        gds          3.05838e-06          3.05838e-06          1.01521e-06
        vgs             0.938679             0.938679             0.939579
        vth             0.874456             0.874456             0.788987
        vds             0.927244             0.927244             0.939578
     vdsat              0.117562             0.117562             0.166155
       gmbs          9.13729e-05          9.13729e-05          9.19137e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm1.m0
      model          pmos_3p3.13
         id          3.80956e-05
         gm          0.000390035
        gds          5.79813e-06
        vgs             0.939579
        vth              0.78946
        vds             0.301318
      vdsat             0.165804
       gmbs          0.000174742
```

The region can be determined by comparing VDS with VDsat and we find all transistors are in saturation as VDS>VDsat. There is no direct way to calculate region in xschem.

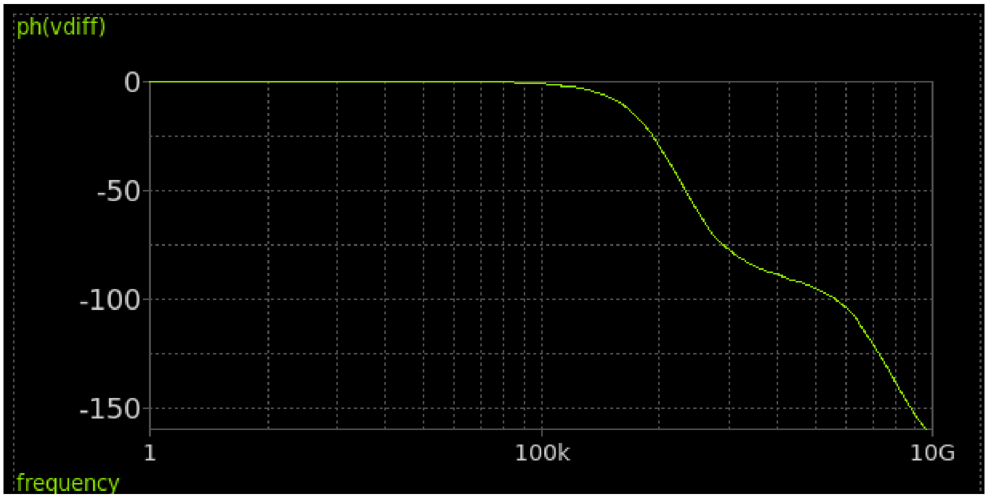
2) Diff small signal ccs:

Report the Bode plot of small signal diff gain:

Magnitude in dB:



Phase:



Gain and BW results:

```
No. of Data Rows : 101
gain                 =  7.722126e+00 at=  1.000000e+00
bw                   =  5.673868e+06
binary raw file "lab6_ac.raw"
ngspice 1 ->
```

Hand Analysis:

$A = gm(RD//ro) \ = 7.72$

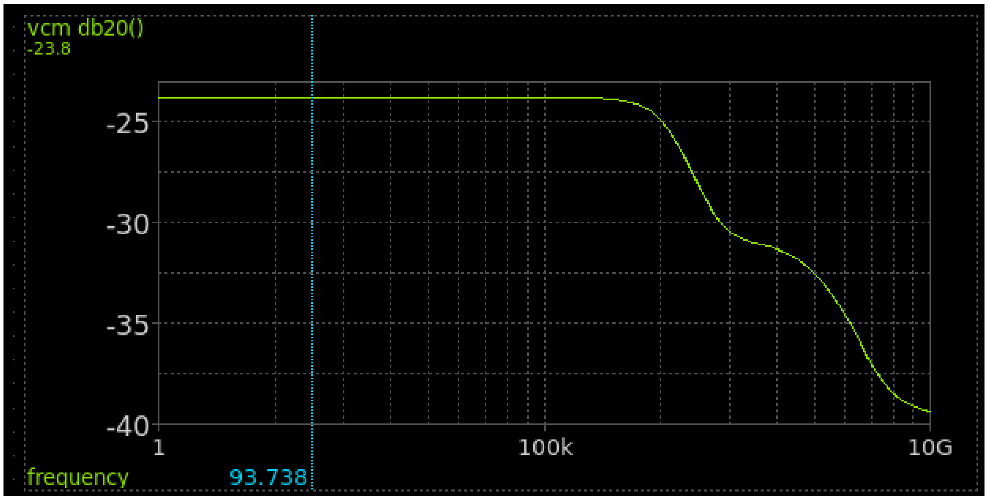
$BW = \frac{1}{Cl*(RD//ro)}$ then $BW = \frac{1}{27.48*10^3*10^{-12}} = 5.79MHz$

	Analytical	Simulation
Gain	7.72	7.72
BW	5.79MHz	$5.67MHz$

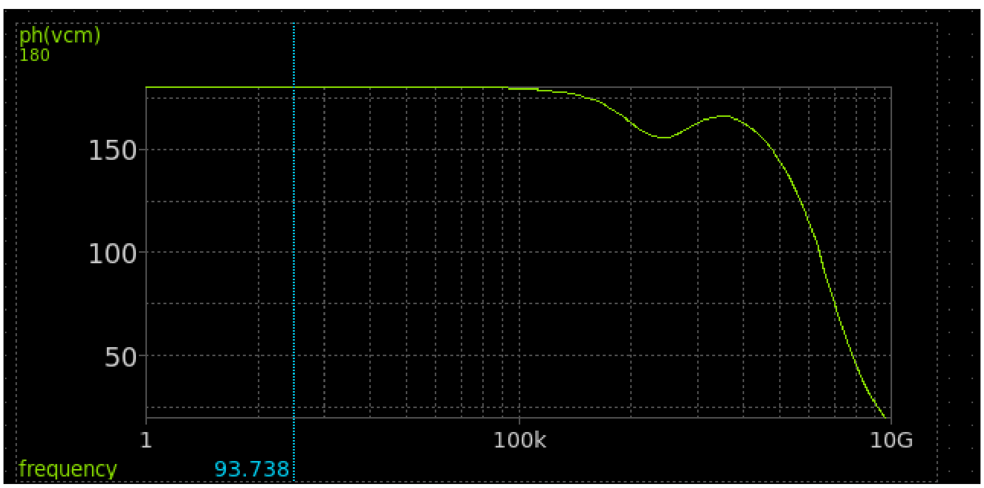
3) CM small signal ccs:

Report the Bode plot of small signal CM gain:

Magnitude in dB:



Phase:



Hand Analysis:

$$ACM = \frac{gm*RD}{1+gm*2ro1} = 0.086$$

```
No. of Data Rows : 101
cmgain              =  6.455234e-02 at=  1.000000e+00
binary raw file "lab6_ac.raw"
ngspice 1 ->
```

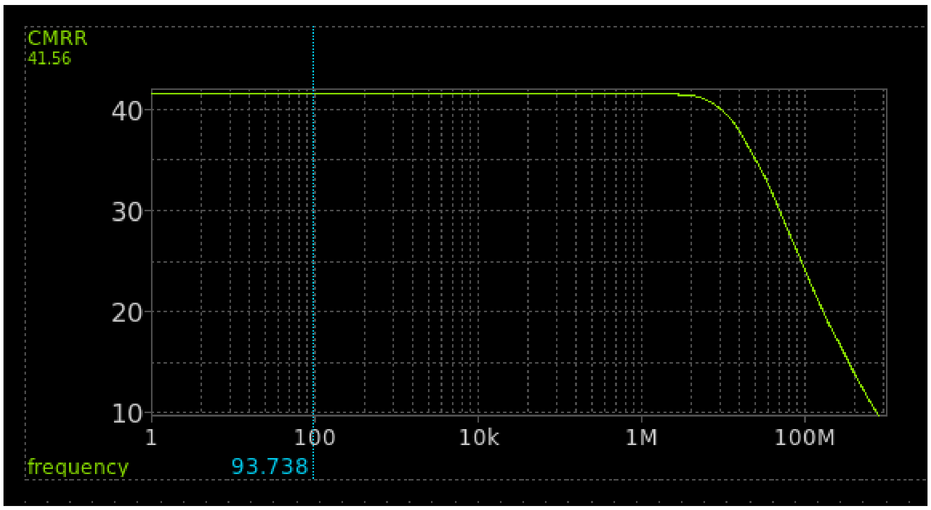
	Analytical	Simulation
Gain	0.086	0.06455

Gain is smaller than 1 as in CM the transistor is degenerated with a large resistance ro of device M1.

Justify the variation of Avcm vs frequency:

At high frequencies the impedance of the capacitance CL decreases a lot which decreases ZD and decreases the gain.

Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table:



Hand Analysis:

$$\frac{Avd}{Avcm} = \frac{7.72}{0.086} = 89.767 = 39dB$$

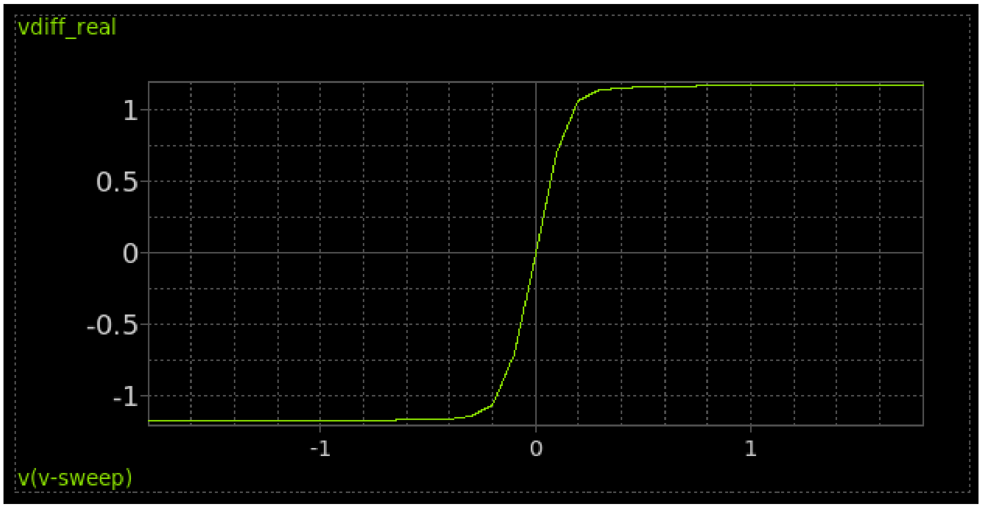
	Analytical	Simulation
CMRR	39dB	$41.56dB$

CMRR decreases at high frequencies as CMRR is proportional to RSS and at high frequencies the capacitance associated with the drain of M1 decreases the equivalent impedance.

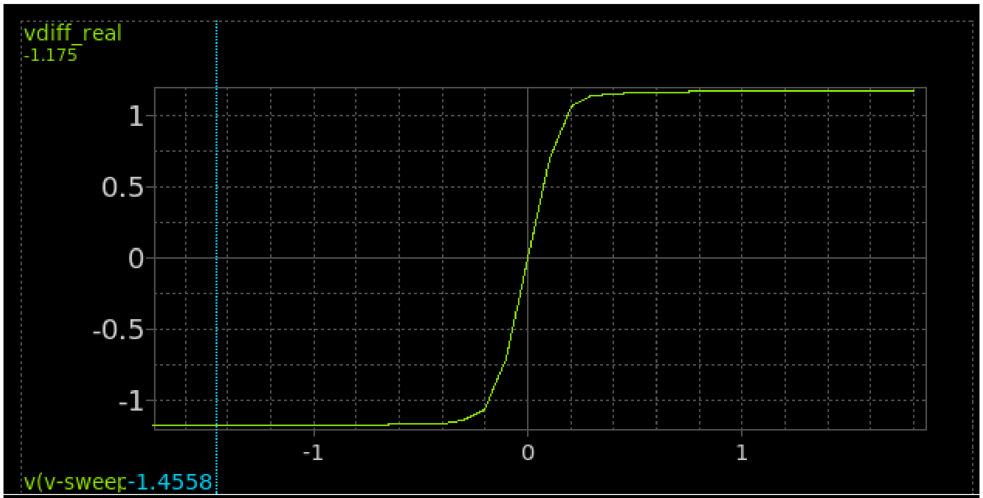
4) Diff large signal ccs:

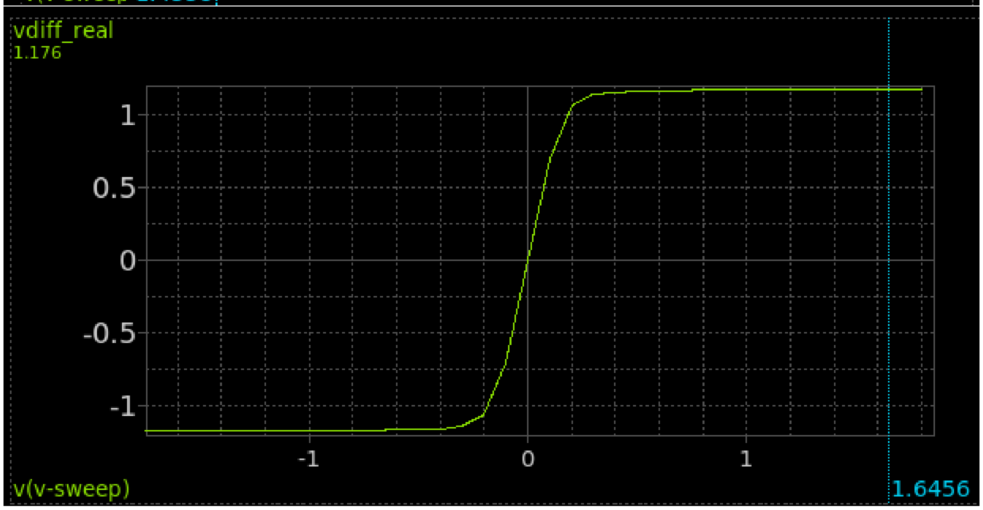
Report diff large signal ccs (VODIFF vs VIDIFF). Compare the extreme values with hand analysis in a table.

VODIFF vs VIDIFF:



Extreme values:



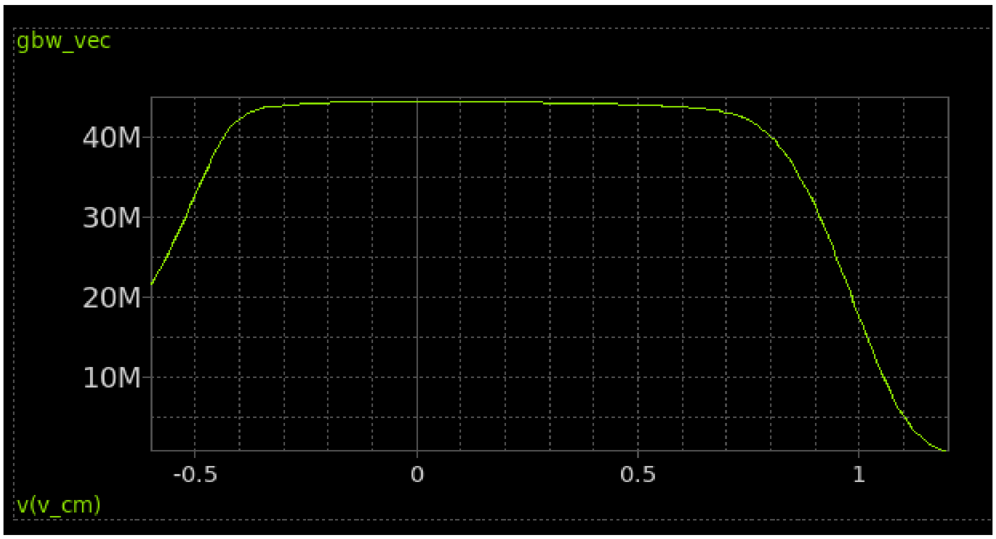


Hand analysis:
At Vid =VDD: $Vod = ISS * RD = 1.2V$
At Vid =-VDD: $Vod = -ISS * RD = -1.2V$

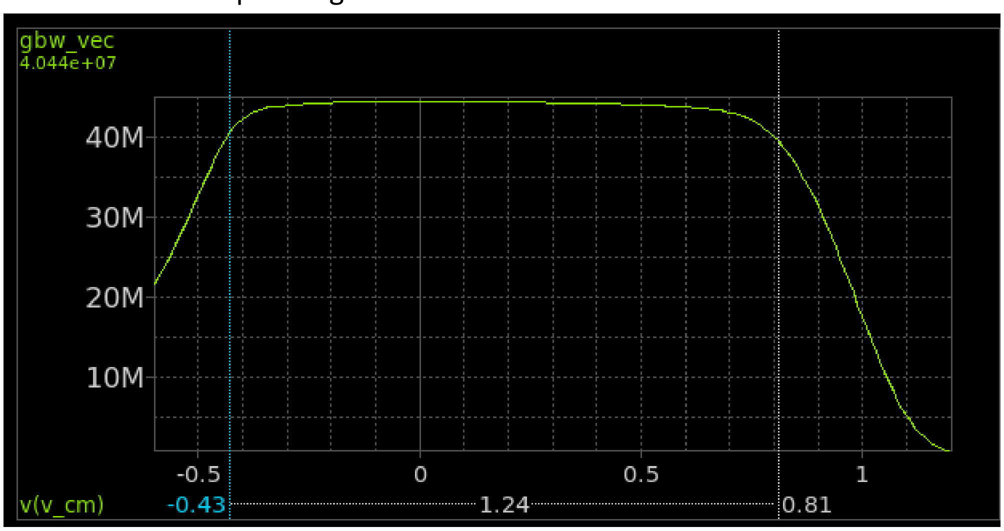
	Analytical	Simulation
Vod at Vid=VDD	1.2	1.175
Vod at Vid=-VDD	-1.2	-1.175

5) CM large signal ccs (GBW vs Vicm):

Report CM large signal ccs (GBW vs VICM):



Common mode input range:




```
vcm_min = -4.30000e-01
vcm_max = 8.100000e-01
ngspice 1 ->
```

Hand analysis was done in first part.

	Analytical	Simulation
VICM min	-0.2184	-0.43
VICM max	0.66	0.81