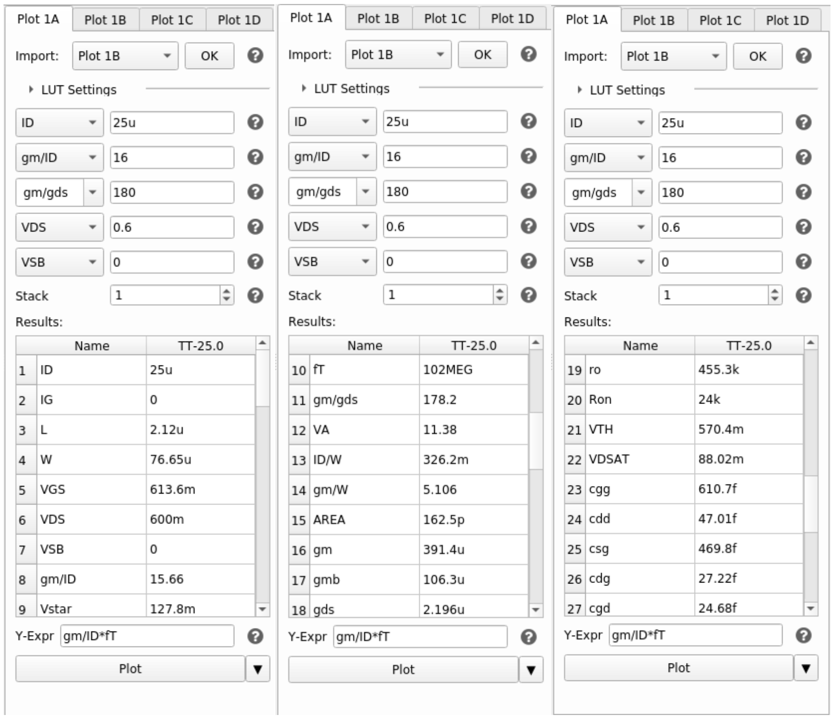
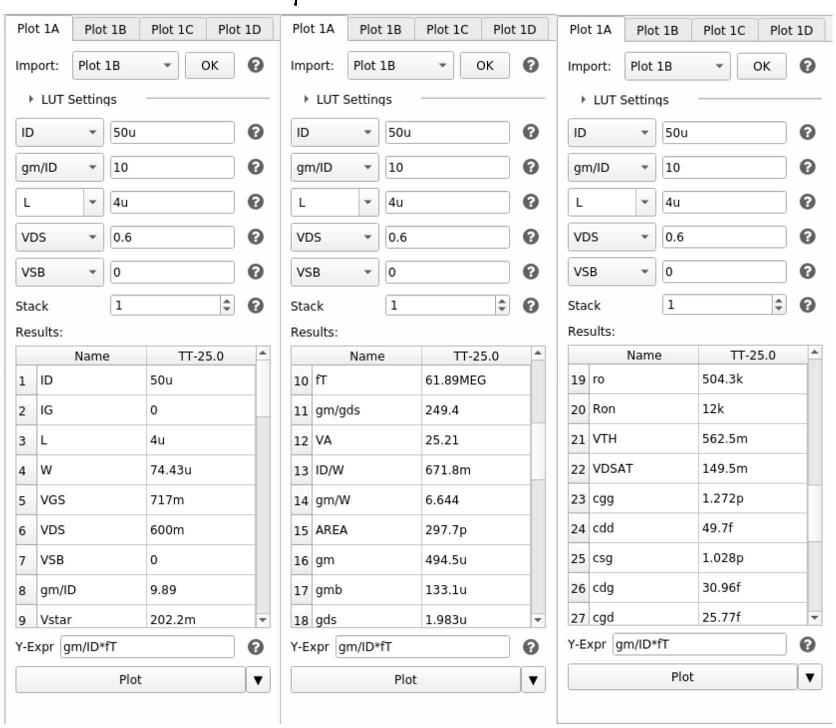
Design Challenge 1

PART 1:

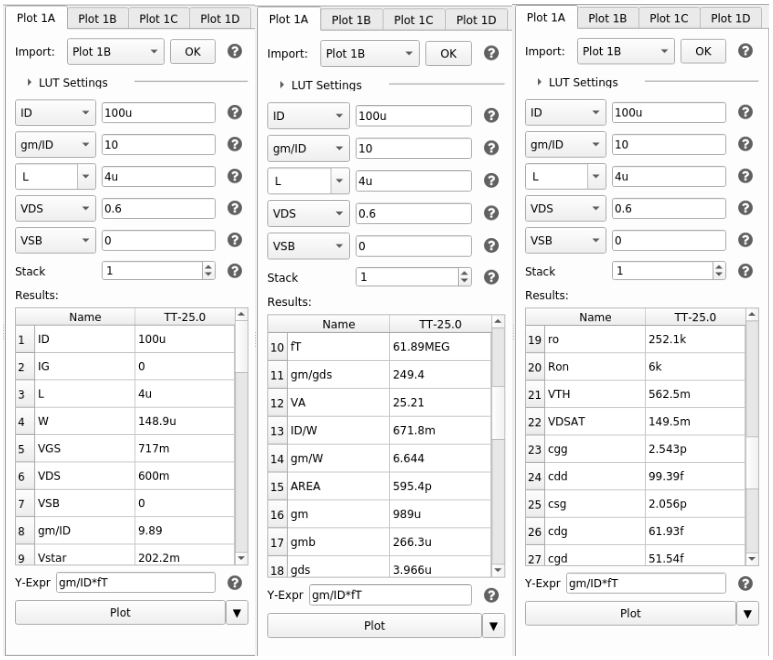
- **From the closed loop specs, calculate the OTA open loop specs.**
- $BWcl = BWol * (1 + \beta Aol) \approx BWol * \beta Aol \approx \beta * GBWol$
- We want $BWcl = 10MHz$ then worst GBW will be at the lowest $\beta = \frac{Cf}{Cf+Cin} = \frac{1}{5}$ at the $gain = 4$ then $GBWol = 50MHz$.
- $\frac{g_{m-input}}{2\pi * Cc} = 50MHz$, We will assume Cc half the worst Cout and worst Cout is at the unity gain buffer connection then $Cout = Cin + Cf = 2.5pF$ then $Cc = 1.25pF$ and we get $g_{m-input} = 392.699\mu S$.
- $LG = \beta Aol = 54dB = 501.18 \; then \; Aol = 2505.9$.
- Finally, the BWol will depend on the value of Aol we get as GBWol will stay constant.
- **OTA topology selection and design steps (use ADT cockpit or the Sizing Assistant).**
- The gain is high and we need high output swing so we will use the two-stage miller OTA. We can't use folded or telescopic as they have low output swing.
- We will distribute the gain between the two stages $A1 = 38dB = 79.43$ and $A2 = 30dB = 31.6227$.
- We will start with the input pair. We will assume $\frac{gm}{ID} = 16$ and then assume $ID = 25\mu A$ to get $gm = 400\mu S$.
- To achieve the gain spec, $\frac{g_m}{g_{ds-input}+g_{gs-load}} \geq 79.43$ We will assume input pair and CM load have the same gds and take the first stage gain to be 90 then $\frac{g_m}{g_{ds}} = 180$.



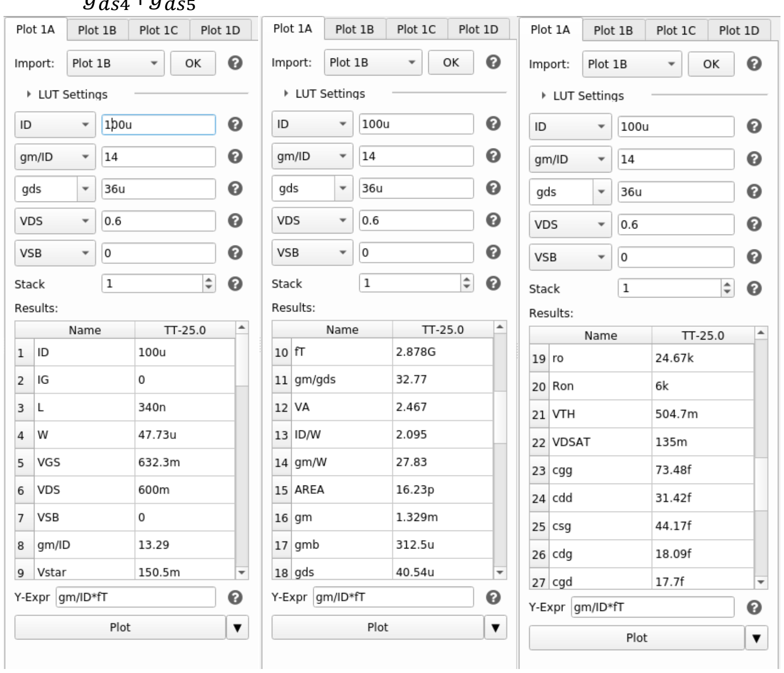
- Now, We will design the tail current source. To put $Vincm = 1V$ then $V_{GS1} + V_{Dsat3} \leq 1$ then $V_{Dsat3} \leq 0.3864$. We will choose $V^* = 0.2V$ then $\frac{gm}{ID} = 10$.
- We will assume $L = 4\mu m$ to increase ro and have less variations when VDS changes. And we know that $ID = 50\mu A$.



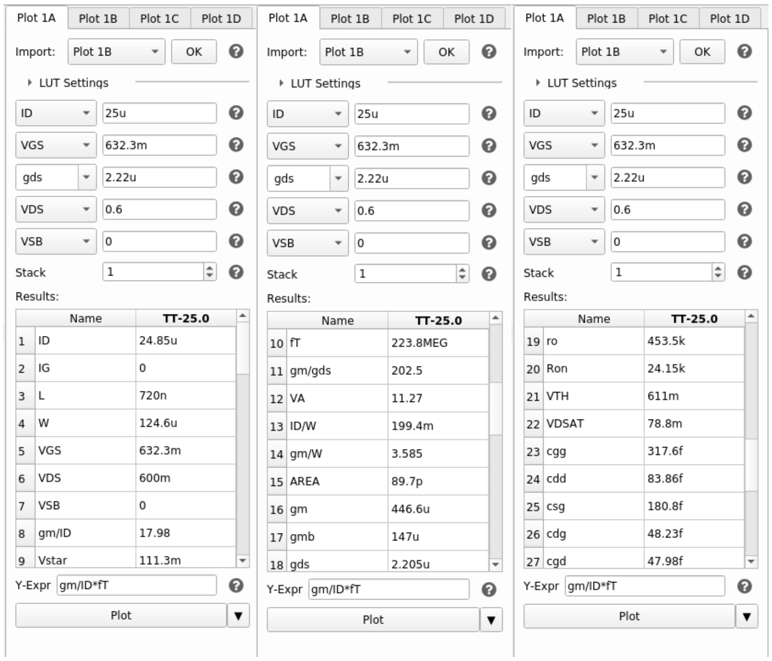
- To design the current mirror of the second stage we want it to match tail current source then $L = 4\mu m$ and $\frac{gm}{ID} = 10$ and we will use $Id = 100\mu A$ as it is a reasonable when calculating the PM spec in the next step.



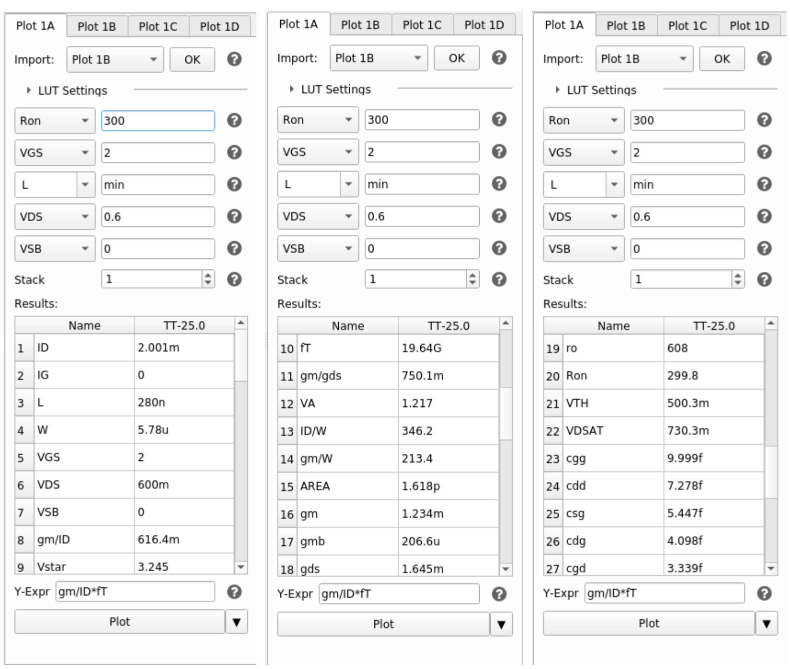
- $PM = 90 - \tan^{-1}\left(\frac{\omega u}{\omega p2}\right) = 60$ then $\omega u < \frac{\sqrt{3}}{3}\omega p2$ then $\frac{g_{m1,2}}{2\pi * Cc} < \frac{\sqrt{3}}{3}\frac{g_{m4}}{2\pi * Cout}$ then $gm4 > 2\sqrt{3}g_{m1,2}$ then $gm4 > 1385.64\mu S$. We choose $gm4 = 1400\mu S$.
- We may assume $\frac{gm}{ID} = 14$ then $ID = 100\mu A$.
- $A2 = \frac{g_{m4}}{g_{ds4} + g_{ds5}} > 32$ then $g_{ds4} < 39.784$. We will choose $g_{ds4} = 36\mu S$.



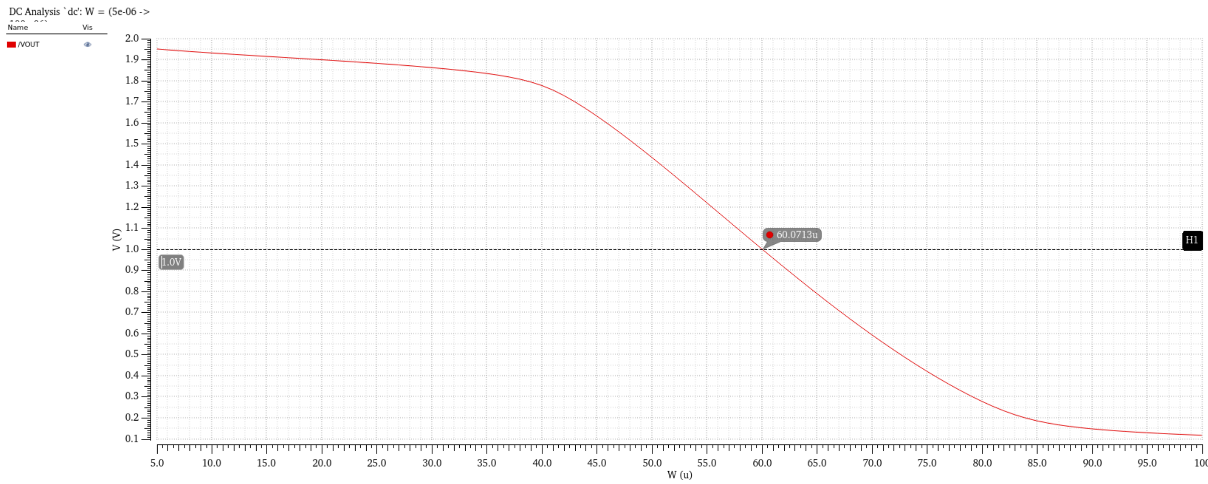
- ➢ We will put $VGS = 632.2mV$ and we know $ID = 25\mu A$ and we assumed $g_{ds} = g_{ds1,2} = 2.22\mu S$.



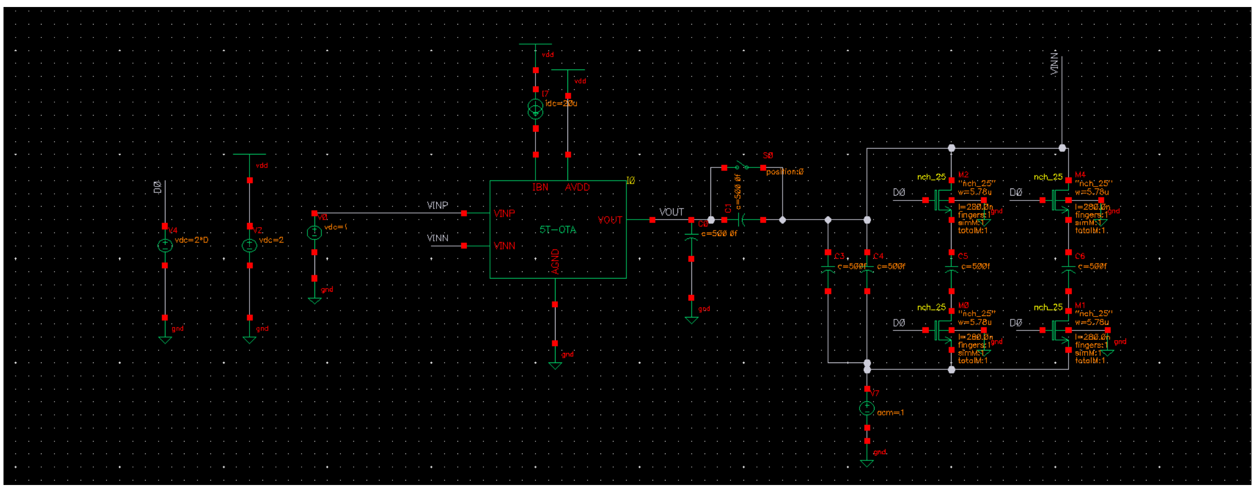
- ➢ $Rz = \frac{1}{g_{m4}} = \frac{1}{1.329*10^{-3}} = 752.44.$
- ➢ Switch design $Xc = \frac{1}{2\pi*f*C} = 31830.988$ at max frequency we want ar least ron less than 100 order then $ron = 300$ and $VGS = VDD$ and minimum L.

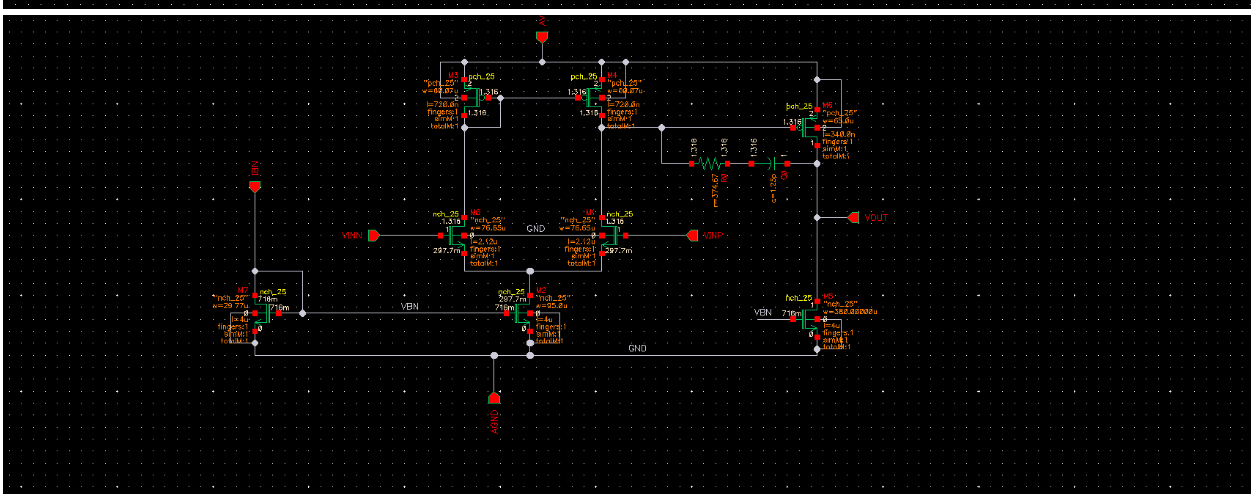


- We made sweep on CM width to cancel offset when we run open loop and set Vout=1.



- **Schematics with device sizing.**

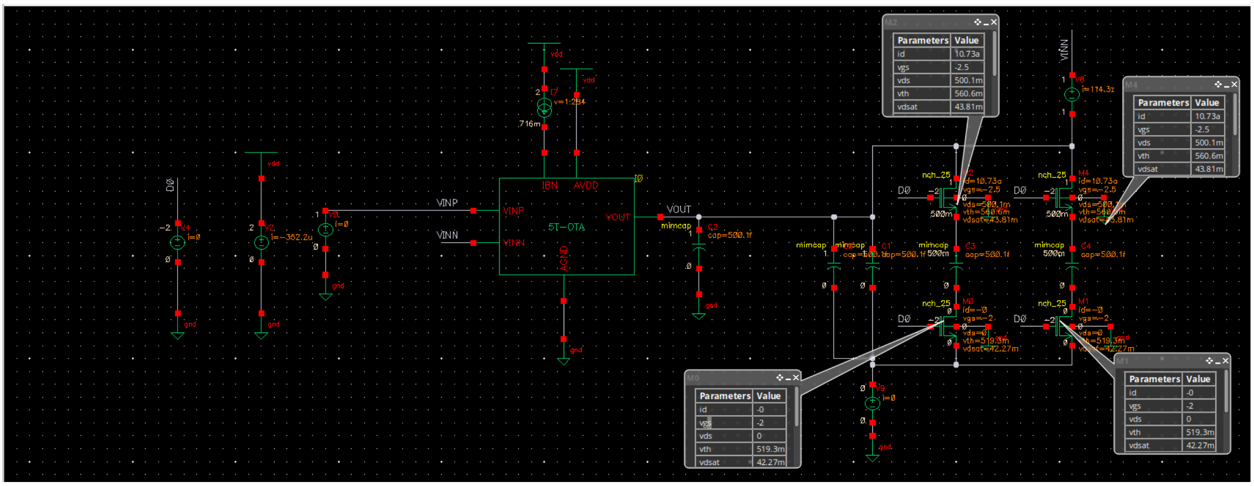


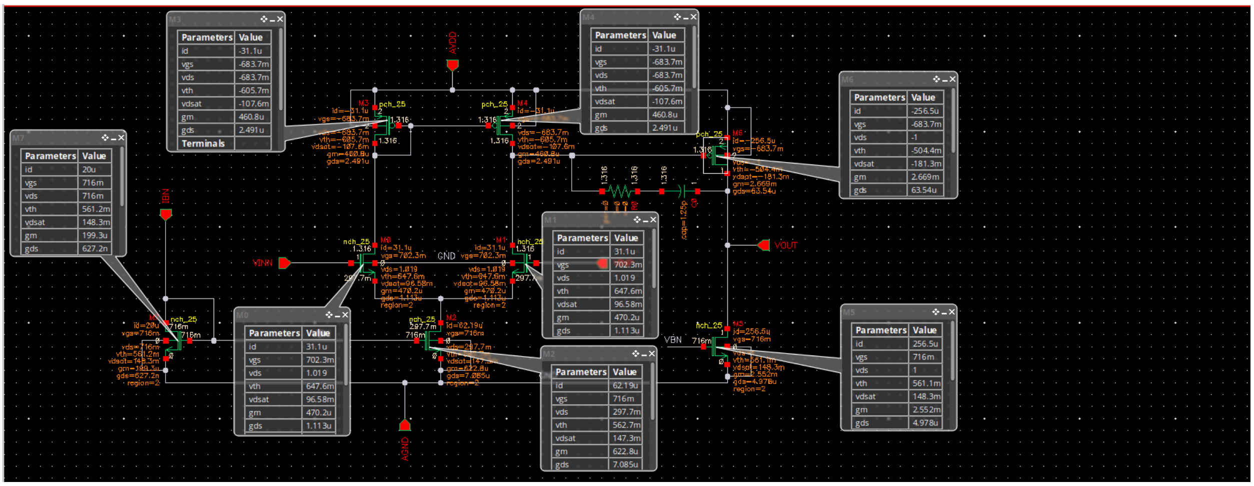


- **Note:** We put two switches to completely separate caps from the circuit and we increased the width of current sources and the second stage PMOS to satisfy the GBW and PM.

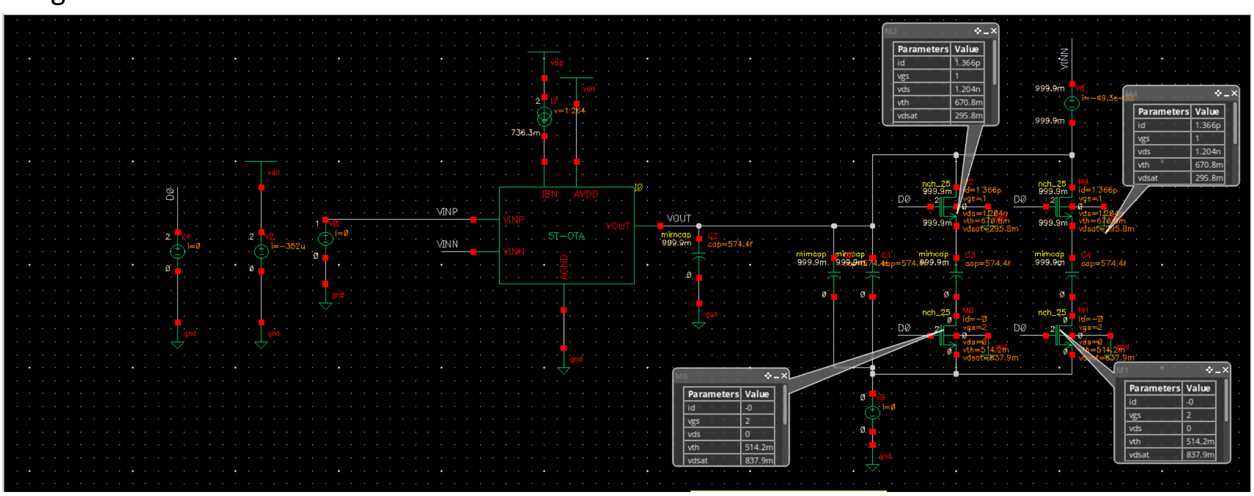
- **Schematics with DC OP and node voltages annotated.**

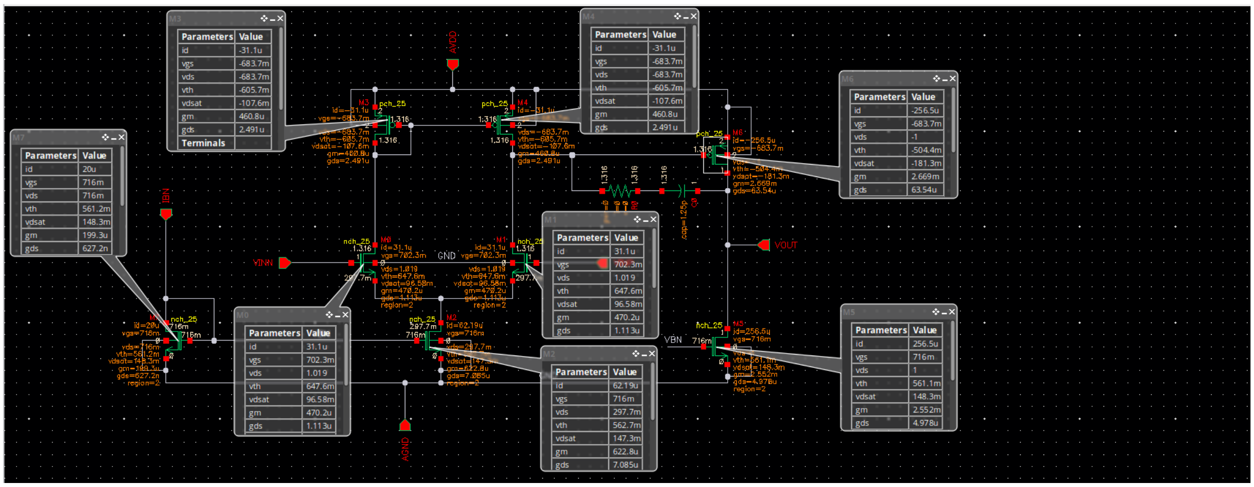
➢ For gain=2:





➢ For gain=4:





- **Closed loop stb analysis results showing the amplifier closed loop specs (Closed loop gain and BW, DC LG, and PM) at the two different gain settings.**
  - Open loop:

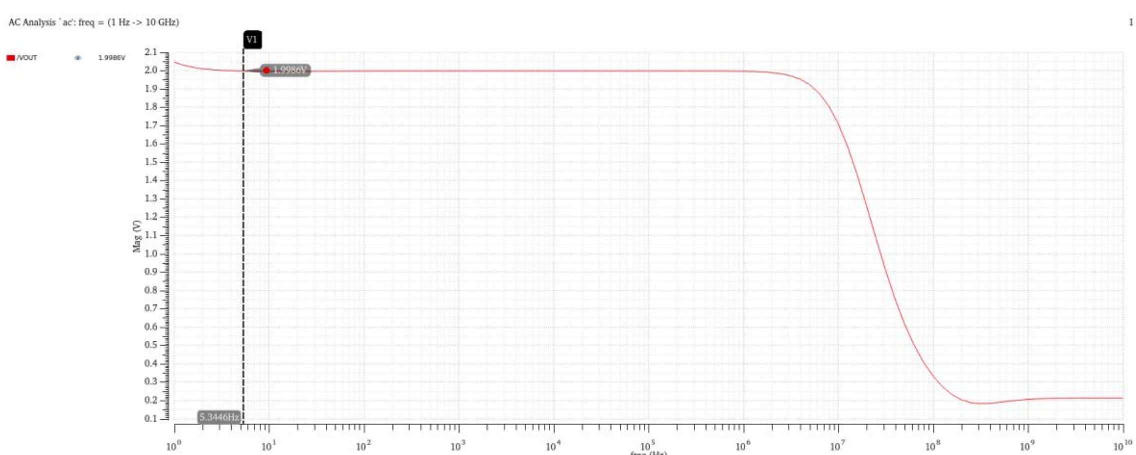
Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	ymax(mag(VF("/VOUT")))	5.069k			
Design_Challenge:design1_TB:1	dB20(ymax(mag(VF("/VOUT"))))	74.1			
Design_Challenge:design1_TB:1	bandwidth(VF("/VOUT") 3 "low")	11.23k			
Design_Challenge:design1_TB:1	gainBwProd(VF("/VOUT"))	57.04M			
Design_Challenge:design1_TB:1	unityGainFreq(VF("/VOUT"))	55.74M			

Note: the open loop gain and GBW are satisfied.

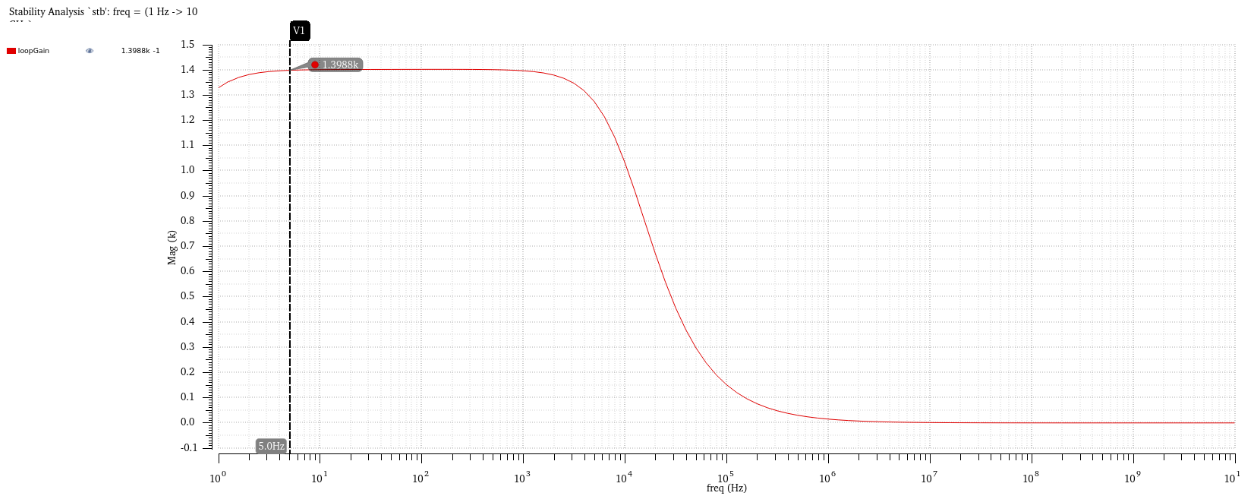
  - Closed loop for A=2:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	ymax(mag(VF("/VOUT")))	2.047			
Design_Challenge:design1_TB:1	dB20(ymax(mag(VF("/VOUT"))))	6.224			
Design_Challenge:design1_TB:1	bandwidth(VF("/VOUT") 3 "low")	15.55M			
Design_Challenge:design1_TB:1	gainBwProd(VF("/VOUT"))	31.91M			
Design_Challenge:design1_TB:1	unityGainFreq(VF("/VOUT"))	28.38M			

Closed loop gain:



DC LG:



PM at the feedback capacitor:

Design_Challenge:design1_TB:1	Phase Margin	84.52	

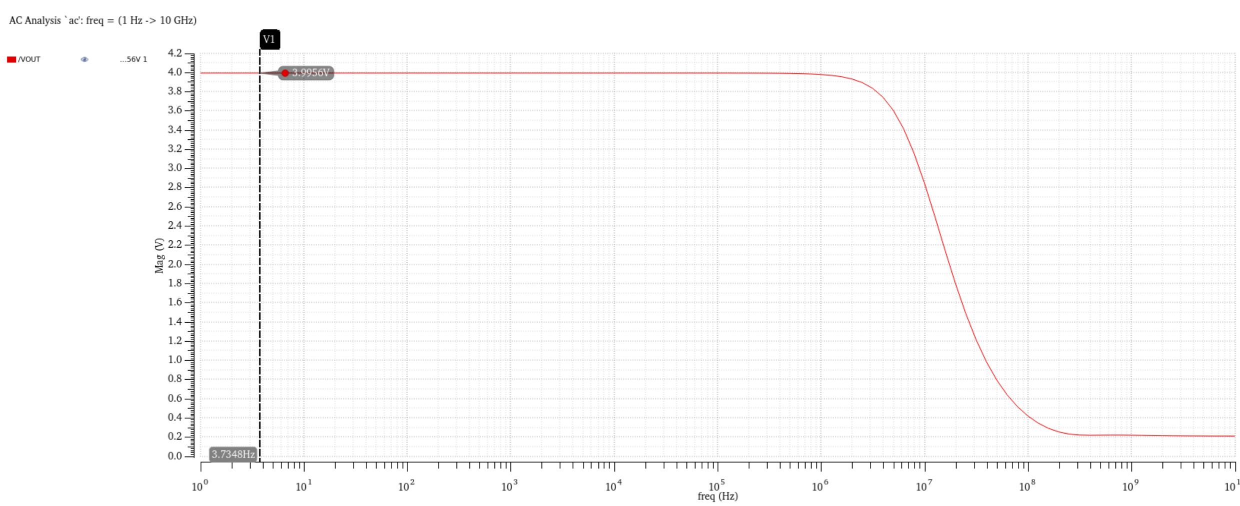
PM at unity gain buffer connection:

Design_Challenge:design1_TB:1	Phase Margin	65.41			

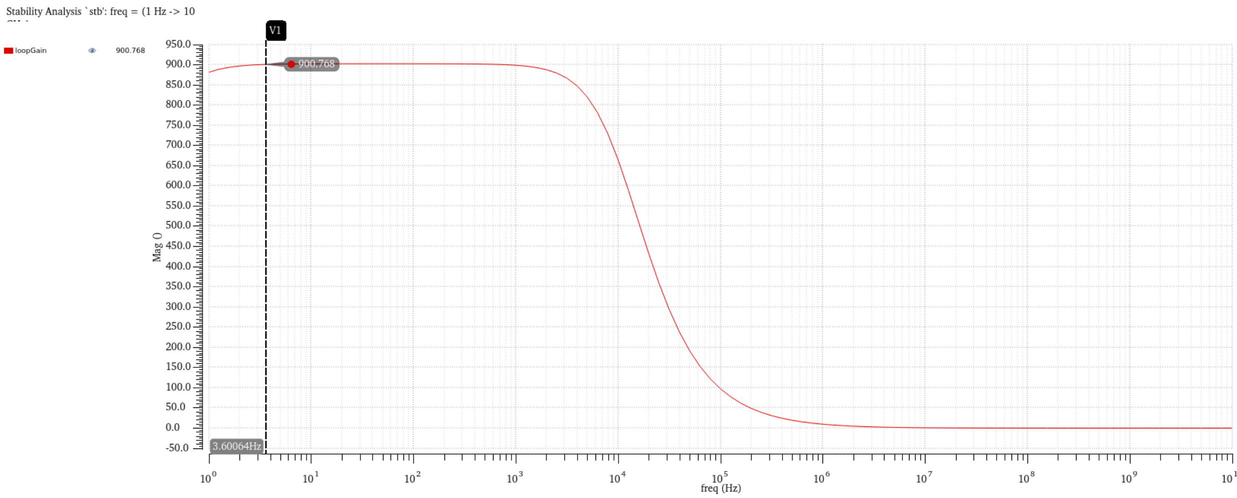
- Closed loop for A=4:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	ymax(mag(VF("/VOUT")))	3.996			
Design_Challenge:design1_TB:1	dB20(ymax(mag(VF("/VOUT"))))	12.03			
Design_Challenge:design1_TB:1	bandwidth(VF("/VOUT") 3 "low")	10.5M			
Design_Challenge:design1_TB:1	gainBwProd(VF("/VOUT"))	42.05M			
Design_Challenge:design1_TB:1	unityGainFreq(VF("/VOUT"))	40.65M			

Closed loop gain:



DC LG:



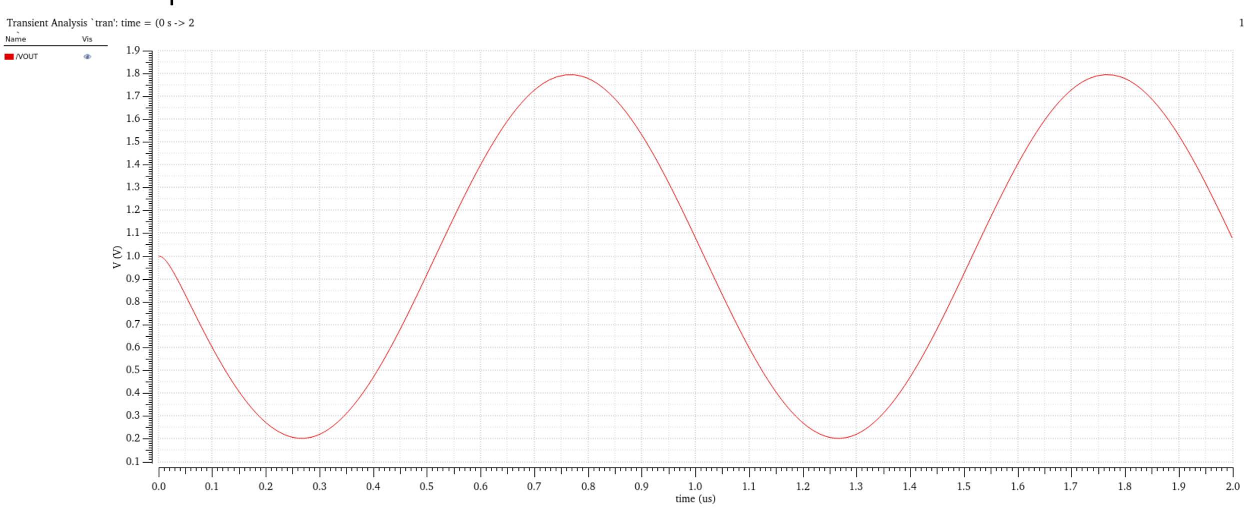
PM at the feedback capacitor:

Design_Challenge:design1_TB:1	Phase Margin	86.66		

PM at unity gain buffer connection:

Design_Challenge:design1_TB:1	Phase Margin	60.24			

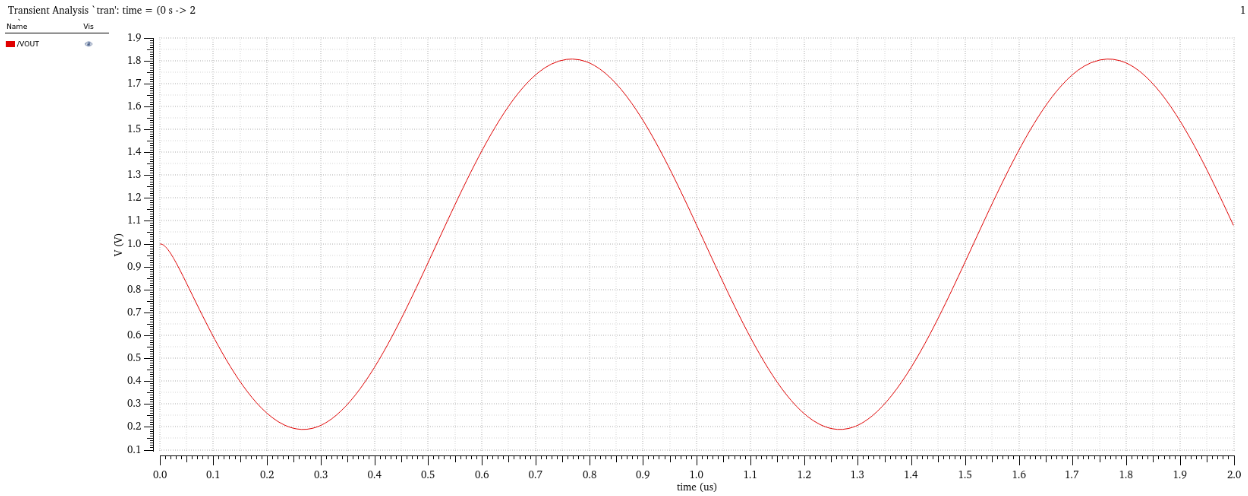
- **Closed loop transient simulation results with sinusoidal input (1 MHz) at the nominal corner showing the maximum output swing at the two different gain settings.**
  - Transient response at A=2:



Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(v("/VOUT" ?result "t...	1.623			

Note: We put input signal amplitude of 406.5mV to have this response. The signal has 180 degree shift as we use inverting topology. We notice that the swing spec is satisfied. And this is the max symmetrical swing as $swing = 2 - 2 * VDsat = 1.638$ almost the same here.

- Transient response at A=4:



Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(v("/VOUT" ?result "t...	1.618			

Note: We put input signal amplitude of 203.5mV to have this response. The signal has 180 degree shift as we use inverting topology. We notice that the swing spec is satisfied.

PART 2:

- **Use the THD function in the calculator to calculate the output distortion.**

- For A=2:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(v("/VOUT" ?result "t...	1.624			
Design_Challenge:design1_TB:1	thd(VT("/VOUT") 1e-06 2e-06 51...	83.57m			

- For A=4:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_Challenge:design1_TB:1	peakToPeak(v("/VOUT" ?result "t...	1.619			
Design_Challenge:design1_TB:1	thd(VT("/VOUT") 1e-06 2e-06 51...	98.05m			

- **Report the simulation results across corners**
  - A=2:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	ymax(mag(VF("/VOUT")))	2.047				2.02	2.064	2.02	2.064
Design_Challenge:design1_TB:1	dB20(ymax(mag(VF("/VOUT"))))	6.224				6.106	6.293	6.106	6.293
Design_Challenge:design1_TB:1	bandwidth(VF("/VOUT") 3 "low")	15.55M				12.25M	20.82M	12.25M	20.82M
Design_Challenge:design1_TB:1	gainBwProd(VF("/VOUT"))	31.91M				24.81M	43.09M	24.81M	43.09M
Design_Challenge:design1_TB:1	unityGainFreq(VF("/VOUT"))	28.38M				21.84M	38.21M	21.84M	38.21M
Design_Challenge:design1_TB:1	Phase Margin	84.52				83.2	85.64	85.64	83.2
Design_Challenge:design1_TB:1	ymax(mag(getData("loopGain" ?...	1.403k				1.359k	1.454k	1.454k	1.359k

We notice that in FF corner at T=-40 the current increased so gm input pair increased and GBW and BW increased and the current in the second branch didn't increase with the same ratio so PM reduced and vice versa in SS at T=100 corner.

PM at unity gain connection:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	Phase Margin	65.45				59.92	69.76	69.76	59.92

  - A=4:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	ymax(mag(VF("/VOUT")))	3.995				3.995	3.995	3.995	3.995
Design_Challenge:design1_TB:1	dB20(ymax(mag(VF("/VOUT"))))	12.03				12.03	12.03	12.03	12.03
Design_Challenge:design1_TB:1	bandwidth(VF("/VOUT") 3 "low")	10.18M				7.72M	14.07M	7.72M	14.07M
Design_Challenge:design1_TB:1	gainBwProd(VF("/VOUT"))	40.79M				30.92M	56.35M	30.92M	56.35M
Design_Challenge:design1_TB:1	unityGainFreq(VF("/VOUT"))	39.36M				30.24M	54.04M	30.24M	54.04M
Design_Challenge:design1_TB:1	Phase Margin	86.66				85.51	87.68	87.68	85.51
Design_Challenge:design1_TB:1	ymax(mag(getData("loopGain" ?...	902.6				887.8	925.7	925.7	887.8

PM at unity gain connection:

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	SS	FF
Design_Challenge:design1_TB:1	Phase Margin	60.63				55.19	64.96	64.96	55.19