3.2 System control processor registers

This section gives details of all the registers in the system control coprocessor. The section presents a summary of the registers and detailed descriptions in register order of CRn, Opcode_1, CRm, Opcode_2.

You can access CP15 registers with MRC and MCR instructions:

```
MCR{cond} P15,<Opcode_1>,<Rd>,<CRn>,<CRm>,<Opcode_2>
MRC{cond} P15,<Opcode_1>,<Rd>,<CRn>,<CRm>,<Opcode_2>
```

3.2.1 Register allocation

Table 3-2 on page 3-14 lists the allocation and reset values of the registers of the system control coprocessor where:

- CRn is the register number within CP15
- Op1 is the Opcode_1 value for the register
- CRm is the operational register
- Op2 is the Opcode_2 value for the register.
- Type applies to the Secure, S, or the Non-secure, NS, world and is:
  - B, registers banked in Secure and Non-secure worlds. If the registers are not banked then they are common to both worlds or only accessible in one world.
  - NA, no access
  - **RO**, read-only access
  - RO, read-only access in privileged modes only
  - **R/W**, read/write access
  - R/W, read/write access in privileged modes only
  - **WO**, write-only access
  - WO, write-only access in privileged modes only
  - X, access depends on another register or external signal.

Table 3-2 Summary of CP15 registers and operations

CRn	Op1	CRm	Op2	Register or operation	S type	NS type	Reset value	Page
c0	0	c0	0	Main ID	RO	RO	0x41xFB76x[a]	page 3-20
			1	Cache Type	RO	RO	0x10152152[b]	page 3-21
			2	TCM Status	RO	RO	0x00020002[c]	page 3-24
			3	TLB Type	RO	RO	0x00000800	page 3-25
		c1	0	Processor Feature 0	RO	RO	0x00000111	page 3-26
			1	Processor Feature 1	RO	RO	0x00000011	page 3-27
			2	Debug Feature 0	RO	RO	0x00000033	page 3-29
			3	Auxiliary Feature 0	RO	RO	0x00000000	page 3-30
			4	Memory Model Feature 0	RO	RO	0x01130003	page 3-31
			5	Memory Model Feature 1	RO	RO	0x10030302	page 3-32
			6	Memory Model Feature 2	RO	RO	0x01222100	page 3-33
			7	Memory Model Feature 3	RO	RO	0x00000000	page 3-35
		c2	0	Instruction Set Feature Attribute 0	RO	RO	0x00140011	page 3-36
			1	Instruction Set Feature Attribute 1	RO	RO	0x12002111	page 3-37
			2	Instruction Set Feature Attribute 2	RO	RO	0x11231121	page 3-39
			3	Instruction Set Feature Attribute 3	RO	RO	0x01102131	page 3-40
			4	Instruction Set Feature Attribute 4	RO	RO	0x00001141	page 3-42
			5	Instruction Set Feature Attribute 5	RO	RO	0x00000000	page 3-43
			6-7	Reserved	-	-	-	-
		c3-c7	-	Reserved	-	-	-	-
c1	0	c0	0	Control	R/W, B[d], X	R/W	0x00050078[e]	page 3-44
			1	Auxiliary Control	R/W	RO	0x00000007	page 3-48
			2	Coprocessor Access Control	R/W	R/W	0x00000000	page 3-51
		c1	0	Secure Configuration	R/W	NA	0x00000000	page 3-52
			1	Secure Debug Enable	R/W	NA	0x00000000	page 3-54
			2	Non-Secure Access Control	R/W	RO	0x00000000	page 3-55

Table 3-2 Summary of CP15 registers and operations (continued)

CRn	Op1	CRm	Op2	Register or operation	S type	NS type	Reset value	Page
c2	0	c0	0	Translation Table Base 0	R/W, B, X	R/W	0x00000000	page 3-57
			1	Translation Table Base 1	R/W, B	R/W	0x00000000	page 3-59
			2	Translation Table Base Control	R/W, B, X	R/W	0x00000000	page 3-60
c3	0	c0	0	Domain Access Control	R/W, B, X	R/W	0x00000000	page 3-63
c4				Not used				
c5	0	c0	0	Data Fault Status	R/W, B	R/W	0x00000000	page 3-64
			1	Instruction Fault Status	R/W, B	R/W	0x00000000	page 3-66
c6	0	c0	0	Fault Address	R/W, B	R/W	0x00000000	page 3-68
			1	Watchpoint Fault Address	R/W	NA	0x00000000	page 3-69
			2	Instruction Fault Address	R/W, B	R/W	0x00000000	page 3-69
c7	0	c0	4	Wait For Interrupt	WO	WO	-	page 3-85
		c4	0	PA	R/W, B	R/W	0x00000000	page 3-80
		c5	0	Invalidate Entire Instruction Cache	WO	WO, X	-	page 3-71
			1	Invalidate Instruction Cache Line by MVA	WO	WO	-	page 3-71
			2	Invalidate Instruction Cache Line by Index	WO	WO	-	page 3-71
			4	Flush Prefetch Buffer	**WO**	**WO**	-	page 3-79
			6	Flush Entire Branch Target Cache	WO	WO	-	page 3-79
			7	Flush Branch Target Cache Entry by MVA	WO	WO	-	page 3-79
		c6	0	Invalidate Entire Data Cache	WO	NA	-	page 3-71
			1	Invalidate Data Cache Line by MVA	WO	WO	-	page 3-71
			2	Invalidate Data Cache Line by Index	WO	WO	-	page 3-71
		c7	0	Invalidate Both Caches	WO	NA	-	page 3-71
		c8	0-3	VA to PA translation in the current world	WO	WO	-	page 3-82
			4-7	VA to PA translation in the other world	WO	NA	-	page 3-83

Table 3-2 Summary of CP15 registers and operations (continued)

CRn	Op1	CRm	Op2	Register or operation	S type	NS type	Reset value	Page
c7	0	c10	0	Clean Entire Data Cache	WO, X	WO, X	-	page 3-71
			1	Clean Data Cache Line by MVA	WO	WO	-	page 3-71
			2	Clean Data Cache Line by Index	WO	WO	-	page 3-71
			4	Data Synchronization Barrier	**WO**	**WO**	-	page 3-83
			5	Data Memory Barrier	**WO**	**WO**	-	page 3-84
			6	Cache Dirty Status	RO, B	RO	0x00000000	page 3-78
		c13	1	Prefetch Instruction Cache Line	WO	WO	-	page 3-71
		c14	0	Clean and Invalidate Entire Data Cache	WO, X	WO, X	-	page 3-71
			1	Clean and Invalidate Data Cache Line by MVA	WO	WO	-	page 3-71
			2	Clean and Invalidate Data Cache Line by Index	WO	WO	-	page 3-71
c8	0	c5	0	Invalidate Instruction TLB unlocked entries	WO, B	WO	-	page 3-86
			1	Invalidate Instruction TLB entry by MVA	WO, B	WO	-	page 3-86
			2	Invalidate Instruction TLB entry on ASID match	WO, B	WO	-	page 3-86
c8	0	c6	0	Invalidate Data TLB unlocked entries	WO, B	WO	-	page 3-86
			1	Invalidate Data TLB entry by MVA	WO, B	WO	-	page 3-86
			2	Invalidate Data TLB entry on ASID match	WO, B	WO	-	page 3-86
		c7	0	Invalidate unified TLB unlocked entries	WO, B	WO	-	page 3-86
			1	Invalidate unified TLB entry by MVA	WO, B	WO	-	page 3-86
			2	Invalidate unified TLB entry on ASID match	WO, B	WO	-	page 3-86

Table 3-2 Summary of CP15 registers and operations (continued)

CRn	Op1	CRm	Op2	Register or operation	S type	NS type	Reset value	Page
c9	0	c0	0	Data Cache Lockdown	R/W	R/W, X	0xFFFFFFF0	page 3-87
			1	Instruction Cache Lockdown	R/W	R/W, X	0xFFFFFFF0	page 3-87
		c1	0	Data TCM Region	R/W, X	R/W, X	0x00000014[f]	page 3-89
			1	Instruction TCM Region	R/W, X	R/W, X	0x00000014[g]	page 3-91
			2	Data TCM Non-secure Control Access	R/W, X	NA	0x00000000	page 3-93
			3	Instruction TCM Non-secure Control Access	R/W, X	NA	0x00000000	page 3-94
		c2	0	TCM Selection	R/W, B	R/W	0x00000000	page 3-96
		c8	0	Cache Behavior Override	R/W[h]	R/W	0x00000000	page 3-97
c10	0	c0	0	TLB Lockdown	R/W, X	R/W, X	0x00000000	page 3-100
		c2	0	Primary Region Memory Remap Register	R/W, B, X	R/W	0x00098AA4	page 3-101
			1	Normal Memory Region Remap Register	R/W, B, X	R/W	0x44E048E0	page 3-101
c11	0	c0	0-3	DMA identification and status	RO	RO, X	0x0000000B[i]	page 3-106
		c1	0	DMA User Accessibility	R/W	R/W, X	0x00000000	page 3-107
		c2	0	DMA Channel Number	**R/W**, X	**R/W**, X	0x00000000	page 3-109
		c3	0-2	DMA enable	**WO**, X	**WO**, X	-	page 3-110
		c4	0	DMA Control	**R/W**, X	**R/W**, X	0x08000000	page 3-112
		c5	0	DMA Internal Start Address	**R/W**, X	**R/W**, X	-	page 3-114
		c6	0	DMA External Start Address	**R/W**, X	**R/W**, X	-	page 3-115
		c7	0	DMA Internal End Address	**R/W**, X	**R/W**, X	-	page 3-116
		c8	0	DMA Channel Status	**RO**, X	**RO**, X	0x00000000	page 3-117
		c15	0	DMA Context ID	R/W	R/W, X	-	page 3-120
c12	0	c0	0	Secure or Non-secure Vector Base Address	R/W, B, X	R/W	0x00000000	page 3-121
			1	Monitor Vector Base Address	R/W, X	NA	0x00000000	page 3-122
		c1	0	Interrupt Status	RO	RO	0x00000000[j]	page 3-123

Table 3-2 Summary of CP15 registers and operations (continued)

CRn	Op1	CRm	Op2	Register or operation	S type	NS type	Reset value	Page
c13	0	c0	0	FCSE PID	R/W, B, X	R/W	0x00000000	page 3-126
			1	Context ID	R/W, B	R/W	0x00000000	page 3-128
			2	User Read/Write Thread and Process ID	**R/W**, B	**R/W**	0x00000000	page 3-129
			3	User Read-only Thread and Process ID	R/W, **RO**, B[k]	R/W, **RO**	0x00000000	page 3-129
			4	Privileged Only Thread and Process ID	R/W, B	R/W	0x00000000	page 3-129
c14				Not used				
c15	0	c2	4	Peripheral Port Memory Remap	R/W, B, X	R/W	0x00000000	page 3-130
		c9	0	Secure User and Non-secure Access Validation Control	R/W, X	NA	0x00000000	page 3-132
		c12	0	Performance Monitor Control	**R/W**, X	**R/W**, X	0x00000000	page 3-133
			1	Cycle Counter	**R/W**, X	**R/W**, X	0x00000000	page 3-137
			2	Count 0	**R/W**, X	**R/W**, X	0x00000000	page 3-138
			3	Count 1	**R/W**, X	**R/W**, X	0x00000000	page 3-139
			4-7	System Validation Counter	**R/W**, X	**R/W**, X	0x00000000	page 3-140
		c13	1-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142
		c14	0	System Validation Cache Size Mask	**R/W**, X	**R/W**, X	0x00006655[l]	page 3-145
c15	1	c13	0-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142
c15	2	c13	1-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142
c15	3	c8	0-7	Instruction Cache Master Valid	R/W, X	NA	0x00000000	page 3-147
		c12	0-7	Data Cache Master Valid	R/W, X	NA	0x00000000	page 3-148
		c13	0-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142
c15	4	c13	0-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142
c15	5	c4	2	TLB Lockdown Index	R/W, X	NA	0x00000000	page 3-149
		c5	2	TLB Lockdown VA	R/W, X	NA	-	page 3-149
		c6	2	TLB Lockdown PA	R/W, X	NA	-	page 3-149
		c7	2	TLB Lockdown Attributes	R/W, X	NA	-	page 3-149
		c13	0-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142
c15	6	c13	0-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142
c15	7	c13	0-7	System Validation Operations	**R/W**, X	**R/W**, X	0x00000000	page 3-142

a. See *c0, Main ID Register* on page 3-20 for the values of bits [23:20] and bits [3:0].

b. Reset value depends on the cache size implemented. The value here is for 16KB instruction and data caches.
c. Reset value depends on the number of TCM banks implemented. The value here is for 2 data TCM and 2 instruction TCM banks.
d. Some bits in this register are banked and some Secure modify only.
e. Reset value depends on external signals.
f. Reset value depends on the TCM sizes implemented. The value here is for 16KB TCM banks.
g. Reset value depends on the TCM sizes implemented, and on the value of the **INITRAM** static configuration signal. The value here is for 16KB TCM banks, with **INITRAM** tied LOW.
h. Some bits in this register are common and some Secure modify only.
i. Reset value depends on the number of DMA channels implemented and the presence of TCMs.
j. Reset value depends on external signals.
k. This register is read/write in Privileged modes and read-only on User mode.
l. Reset value depends on the cache and TCM sizes implemented. The value here is for 2 banks of 16KB instruction and data TCMs and 16KB instruction and data caches.

Table 3-3 lists the operations available with MCRR operations:

```
MCRR{cond} P15,<Opcode_1>,<End Address>,<Start Address>,<CRm>
```

Table 3-3 Summary of CP15 MCRR operations

Op1	CRm	Register or operation	S type	NS type	Reset value	Page
0	c5	Invalidate instruction cache range	WO	WO	-	page 3-69
	c6	Invalidate data cache range	WO	WO	-	page 3-69
	c12	Clean data cache range	**WO**	**WO**	-	page 3-69
	c14	Clean and invalidate data cache range	WO	WO	-	page 3-69