Ass_Syn_2.0

You have to synthesize **your UART_TX** files using Design Compiler shell and generate Technology Dependent gate level netlists in Verilog format using standard cell libraries (typical, worst, best) inside std_cells folder:-

- scmetro_tsmc_cl013g_rvt_tt_1p2v_25c.db
- scmetro_tsmc_cl013g_rvt_ff_1p32v_m40c
- scmetro_tsmc_cl013g_rvt_ss_1p08v_125c

Required: -

1. Add the following Optimization Constraints in cons.tcl: -
    - Clock Frequency with 115.2 KHz
    - Clock uncertainty with 0.25 ns for setup
    - Clock uncertainty with 0.05 ns for hold
    - Clock transition with 0.1 ns
    - Input delays on all input ports except (CLK & RST) with 30% clock period
    - Output delays on all output ports with 30% clock period
    - Add Buffer driving cell for all input ports
    - Add load of 0.5 pf on all output ports
    - Add dont_touch attribute on CLK port
    - Set operation condition using slow and fast libraries
    - Set wireload model using slow library
2. Check the synthesis log (syn.log) is free of (Errors, Latches, Comb Loops) and modify your RTL files to fix any issues.
3. Generate the following reports: -
    1) Power report using (report_power -hierarchy) command
    2) Area report using (report_area -hierarchy) command
    3) Setup timing analysis report (report_timing -max_paths 100 -delay_type max) command
    4) Hold timing analysis report (report_timing -max_paths 100 -delay_type min) command
    5) Clocks report using (report_clock –attributes) command
    6) Constraints report using (report_constraint -all_violators) command

4. Generate the following Output files: -
    1) Technology Dependent Gate Level Netlist in Verilog Format
    2) Technology Dependent Gate Level Netlist in ddc Format
    3) SDF File
    4) SDC File

Required: -

A) You have to deliver the following files: -
    0- Synthesis script >> syn_script.tcl
    1- Constraints file >> cons.tcl
    2- Synthesis log >> syn.log
    3- Technology Dependent Verilog Netlist >> UART_TX.v
    4- Technology Dependent ddc Netlist >> UART_TX.ddc
    5- SDC File >> UART_TX.sdc
    6- SDF File >> UART_TX.sdf
    7- Area report >> Area.rpt
    8- Power report >> power.rpt
    9- Hold analysis report >> hold.rpt
    10- Setup analysis report >> setup.rpt
    11- Clocks report >> clocks.rpt
    12- Constraints report >> constraints.rpt