Design, UVM_Enviroment Using DPI-c and Implementation for a Low-Power, Configurable Multi-Clock Digital System RTL to GDS

ASIC FLOW

Ahmed Awad

Abstract

- Designed RTL for system blocks, including ALU, Register File, Synchronous FIFO, Integer Clock Divider, Clock Gating, Synchronizers, Main Controller, UART TX, and UART RX.
- Integrated and verified design functionality with a self-checking testbench.
- Create UVM Environment using Double environments then making a reference model for scoreboard using C++.
- Connect between scoreboard and reference model using DPI-C.
- Synthesized and optimized the design using Design Compiler.
- Analyzed timing paths, resolving setup and hold violations.
- Verified functional equivalence using Formality.
- Executed physical implementation through ASIC flow, culminating in GDS file generation.
- Conducted post-layout verification, accounting for actual delays.
- DFT and formality pot DFT then PnR

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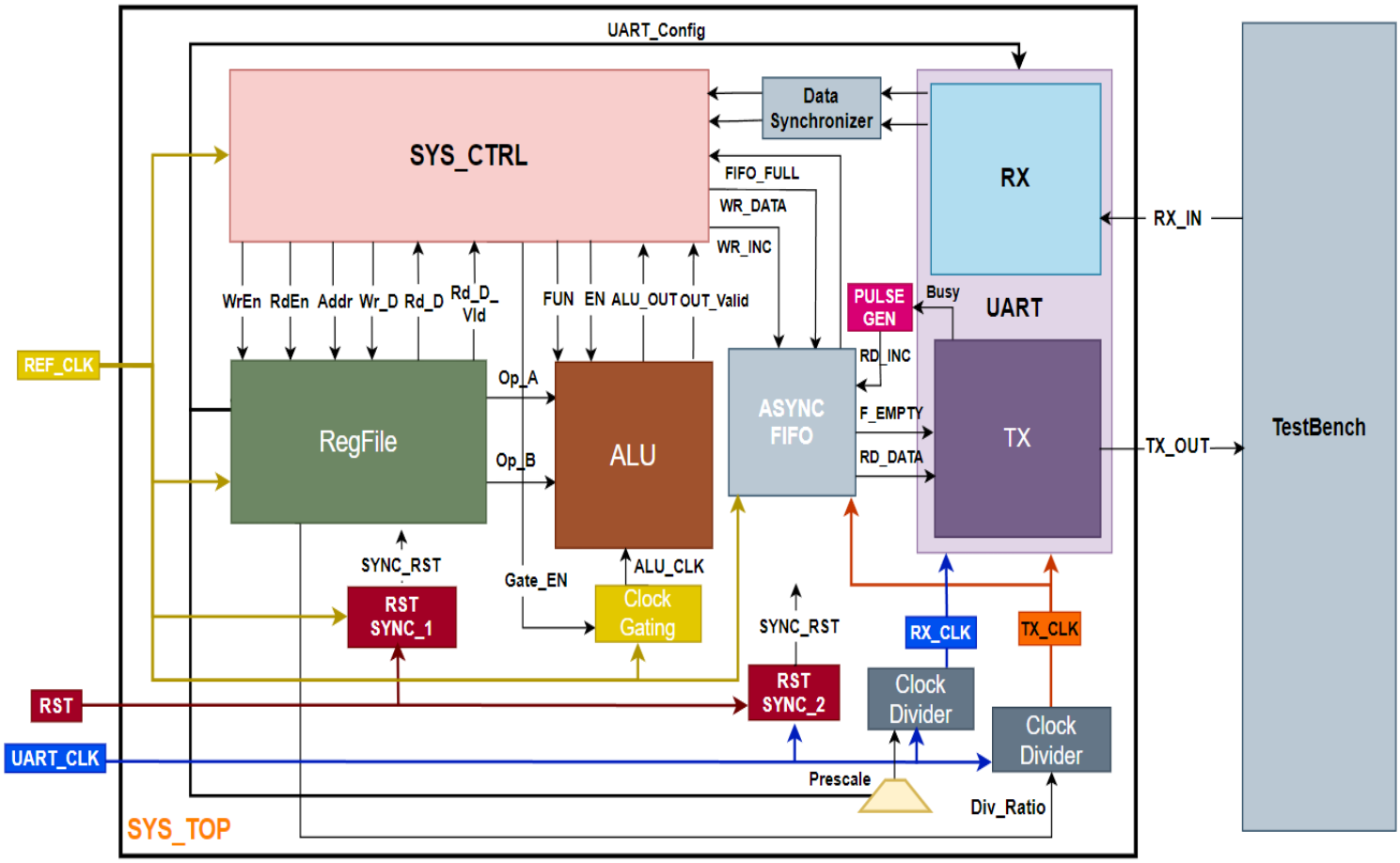
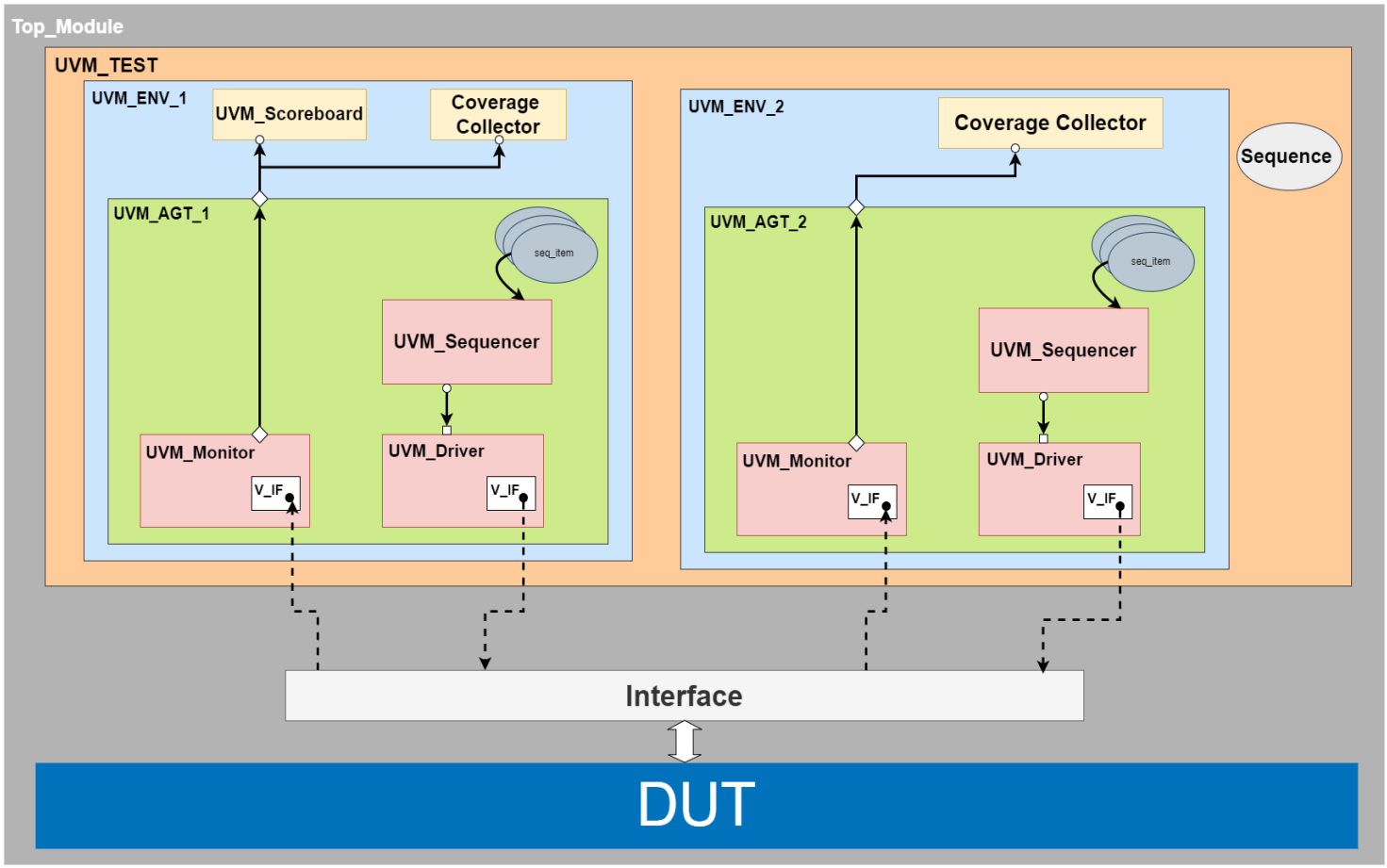
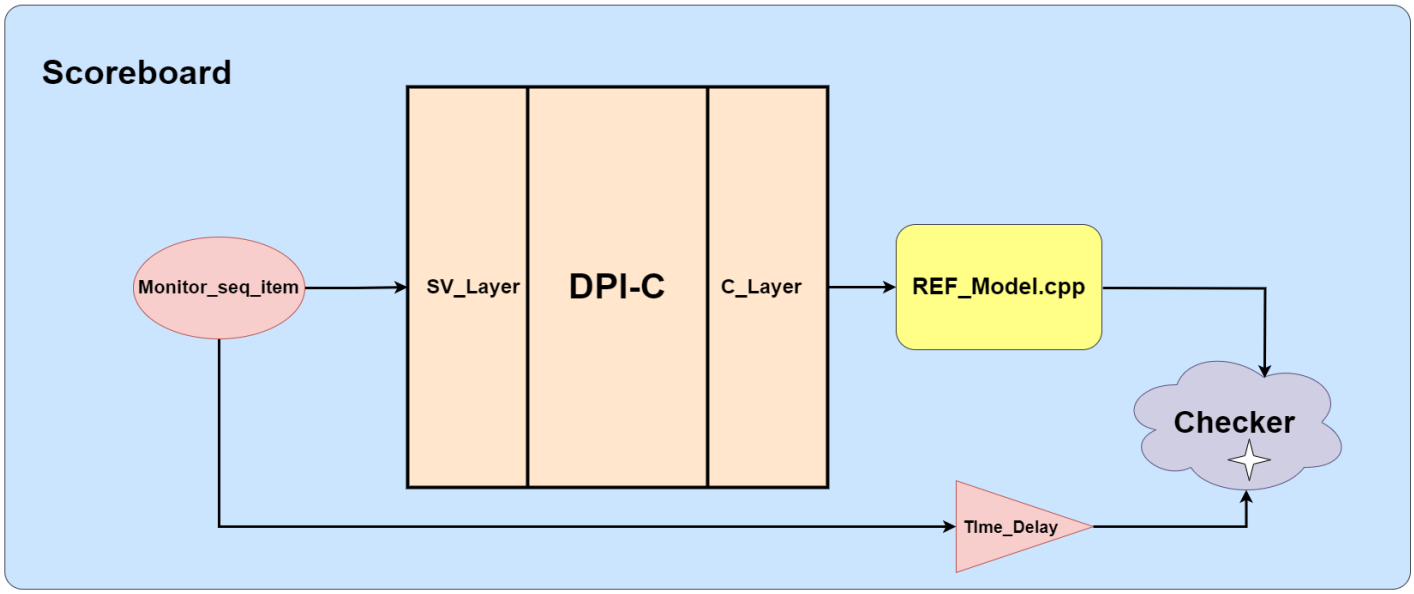
System Flow Diagram

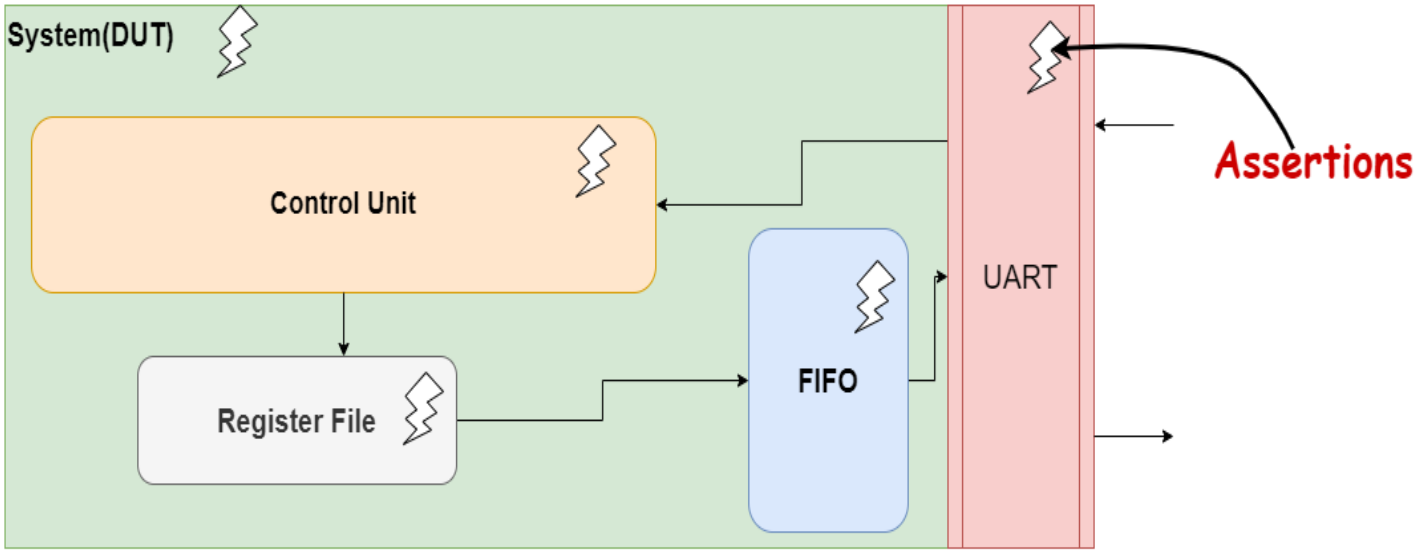


System Verification Environment

SYSTEM VERIFICATION ENVIRONMENT






System(DUT)
Control Unit
Register File
FIFO
UART
Assertions

Verification Results

```
# UVM_INFO @ 0: reporter [RNTST] Running test SYS_TEST_C...
# UVM_INFO SYS_TEST.sv(31) @ 0: uvm_test_top [b] Inside the SYSTEM
# UVM_INFO SYS_TEST.sv(39) @ 0: uvm_test_top [TEST] Inside the SYSTEM
# UVM_INFO SYS_AGENT.sv(44) @ 0: uvm_test_top.SYS_ENV1.MY_AGT [AGT] Inside1
# UVM_INFO SYS_AGENT.sv(46) @ 0: uvm_test_top.SYS_ENV1.MY_AGT [AGT] Inside2
# UVM_INFO SYS_AGENT.sv(48) @ 0: uvm_test_top.SYS_ENV1.MY_AGT [AGT] Inside3
# UVM_INFO SYS_AGENT.sv(50) @ 0: uvm_test_top.SYS_ENV1.MY_AGT [AGT] Inside4
# UVM_INFO SYS_AGENT.sv(44) @ 0: uvm_test_top.SYS_ENV2.MY_AGT [AGT] Inside1
# UVM_INFO SYS_AGENT.sv(46) @ 0: uvm_test_top.SYS_ENV2.MY_AGT [AGT] Inside2
# UVM_INFO SYS_AGENT.sv(48) @ 0: uvm_test_top.SYS_ENV2.MY_AGT [AGT] Inside3
# UVM_INFO SYS_AGENT.sv(50) @ 0: uvm_test_top.SYS_ENV2.MY_AGT [AGT] Inside4
# UVM_INFO SYS_TEST.sv(48) @ 0: uvm_test_top [TEST] Inside the SYSTEM
# UVM_INFO SYS_TEST.sv(51) @ 0: uvm_test_top [TEST] Inside the SYSTEM
# UVM_INFO SYS_TEST.sv(55) @ 0: uvm_test_top [TEST] Inside the SYSTEM1
# UVM_INFO SYS_TEST.sv(62) @ 867208672: uvm_test_top [TEST] Inside the SYSTEM2
# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 1214097344: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
# UVM_INFO SYS_SCOREBOARD.sv(103) @ 1214097344: uvm_test_top.SYS_ENV1.MY_SB [report_phase]
# CORRECT = 985139
# ERROR = 0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :   19
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [AGT]     8
# [Questa UVM]     2
# [RNTST]     1
# [TEST]     5
# [TEST_DONE]     1
# [b]     1
# [report_phase]     1
# ** Note: $finish    : C:/questasim64_2021.1/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 1214097344 ns  Iteration: 60  Instance: /SYS_UVM_TOP
# Saving coverage database on exit...
# End time: 20:08:28 on Sep 24,2024, Elapsed time: 0:27:16
# Errors: 0, Warnings: 0
```

```
# UVM_INFO SYS_SCOREBOARD.sv(73) @ 485660: uvm_test_top.SYS_ENV1.MY_SB [report_phase]  REF = 9  DUT2 = 9
# reg_file read DONE :):):):):):):)  result= 9
```

```
# UVM_INFO SYS_SCOREBOARD.sv(64) @ 201579580: uvm_test_top.SYS_ENV1.MY_SB [report_phase]  REF = d9  DUT1 = d9
# reg_file Write DONE :):):):):):):) 217
```

```
# UVM_INFO SYS_SCOREBOARD.sv(82) @ 458753820: uvm_test_top.SYS_ENV1.MY_SB [report_phase]  REF = 2e  DUT3 = 2e
# ALU_with_OP DONE :):):):):):)  result= 46
```

```
# UVM_INFO SYS_SCOREBOARD.sv(92) @ 187460620: uvm_test_top.SYS_ENV1.MY_SB [report_phase]  REF = 11bf  DUT4 = 11bf
# ALU_NO_OP DONE :):):):):):)  result= 4543
```

Coverage Results

Assertions Coverage

Name	Language	Enabled	Count	AtLeast	Weight	Cmplt %	Cmplt graph	Included	Design Unit
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop1_U	SVA	✓	33506	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop2_U	SVA	✓	33506	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop3_U	SVA	✓	28613	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop4_U	SVA	✓	10084	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop5_U	SVA	✓	10084	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop6_U	SVA	✓	4893	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop7_U	SVA	✓	13360	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop8_U	SVA	✓	13360	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop9_U	SVA	✓	13360	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop10_U	SVA	✓	13360	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop11_U	SVA	✓	13360	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop12_U	SVA	✓	13341	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop13_U	SVA	✓	13324	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop14_U	SVA	✓	13282	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop15_U	SVA	✓	13255	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop16_U	SVA	✓	8688	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop17_U	SVA	✓	1510	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop18_U	SVA	✓	3056	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/cvr_prop19_U	SVA	✓	10198	1	1	100%		✓	UART_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop1_C	SVA	✓	2793	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop2_C	SVA	✓	2769	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop3_C	SVA	✓	2668	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop4_C	SVA	✓	2739	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop5_C	SVA	✓	2788	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop6_C	SVA	✓	2742	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop7_C	SVA	✓	2725	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop8_C	SVA	✓	2725	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop9_C	SVA	✓	2657	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop10_U	SVA	✓	2651	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop11_C	SVA	✓	5357	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop12_C	SVA	✓	5357	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop13_C	SVA	✓	5357	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop14_C	SVA	✓	5357	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop15_C	SVA	✓	5357	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/cvr_prop16_C	SVA	✓	2788	1	1	100%		✓	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U5/RF_Asser/cvr_prop1_R	SVA	✓	8050	1	1	100%		✓	REG_FILE_Asser
/SYS_UVM_TOP/DUT_M/U5/RF_Asser/cvr_prop2_R	SVA	✓	2725	1	1	100%		✓	REG_FILE_Asser
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/cvr_prop1_F	SVA	✓	13439	1	1	100%		✓	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/cvr_prop2_F	SVA	✓	13439	1	1	100%		✓	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/cvr_prop3_F	SVA	✓	13360	1	1	100%		✓	FIFO_ASSER

Name	Assertion Type	Language	Enable	Failure Count	Pass Count	Design Unit
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop3_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/assert_prop2_F	Concurrent	SVA	on	0	1	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/assert_prop1_F	Concurrent	SVA	on	0	1	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop1_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop2_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop3_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop4_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop5_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop6_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop7_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop8_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop9_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop10_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop11_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop12_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop13_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop14_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop15_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop16_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop17_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop18_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/assert_prop19_U	Concurrent	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U5/RF_Asser/assert_prop2_R	Concurrent	SVA	on	0	1	REG_FILE_Asser
/SYS_UVM_TOP/DUT_M/U5/RF_Asser/assert_prop1_R	Concurrent	SVA	on	0	1	REG_FILE_Asser
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop1_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop2_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop16_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop4_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop5_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop6_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop7_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop8_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop9_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop10_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop11_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop12_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop13_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop14_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/assert_prop15_C	Concurrent	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/assert_prop3_F	Concurrent	SVA	on	0	1	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser/proc_reset_RX/immed__25	Immediate	SVA	on	0	1	CTRL_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/proc_reset_TX/immed__52	Immediate	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTIONS/proc_reset_RX/immed__6	Immediate	SVA	on	0	1	UART_Assertions
/SYS_UVM_TOP/DUT_M/U5/RF_Asser/proc_reset/immed__4	Immediate	SVA	on	0	1	REG_FILE_Asser
/SYS_UVM_TOP/DUT_M/U5/RF_Asser/#ublk#82509986#17/immed__18	Immediate	SVA	on	0	1	REG_FILE_Asser
/SYS_SEQUENCE::SEQ_1::body/#ublk#266802693#40/immed__43	Immediate	SVA	on	0	1	SYS_SEQUENCE
/uvm_pkg::uvm_reg_map::do_read/#ublk#215181159#1771/immed__1775	Immediate	SVA	on	0	0	uvm_pkg
/uvm_pkg::uvm_reg_map::do_write/#ublk#215181159#1731/immed__1735	Immediate	SVA	on	0	0	uvm_pkg
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/proc_reset1/immed__5	Immediate	SVA	on	0	1	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/proc_fifo_read/immed__9	Immediate	SVA	on	0	1	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER/proc_reset2/immed__14	Immediate	SVA	on	0	1	FIFO_ASSER
/SYS_UVM_TOP/DUT_M/ASSERTIONS/#ublk#34179907#2/immed__4	Immediate	SVA	on	0	1	SYS_Assertions

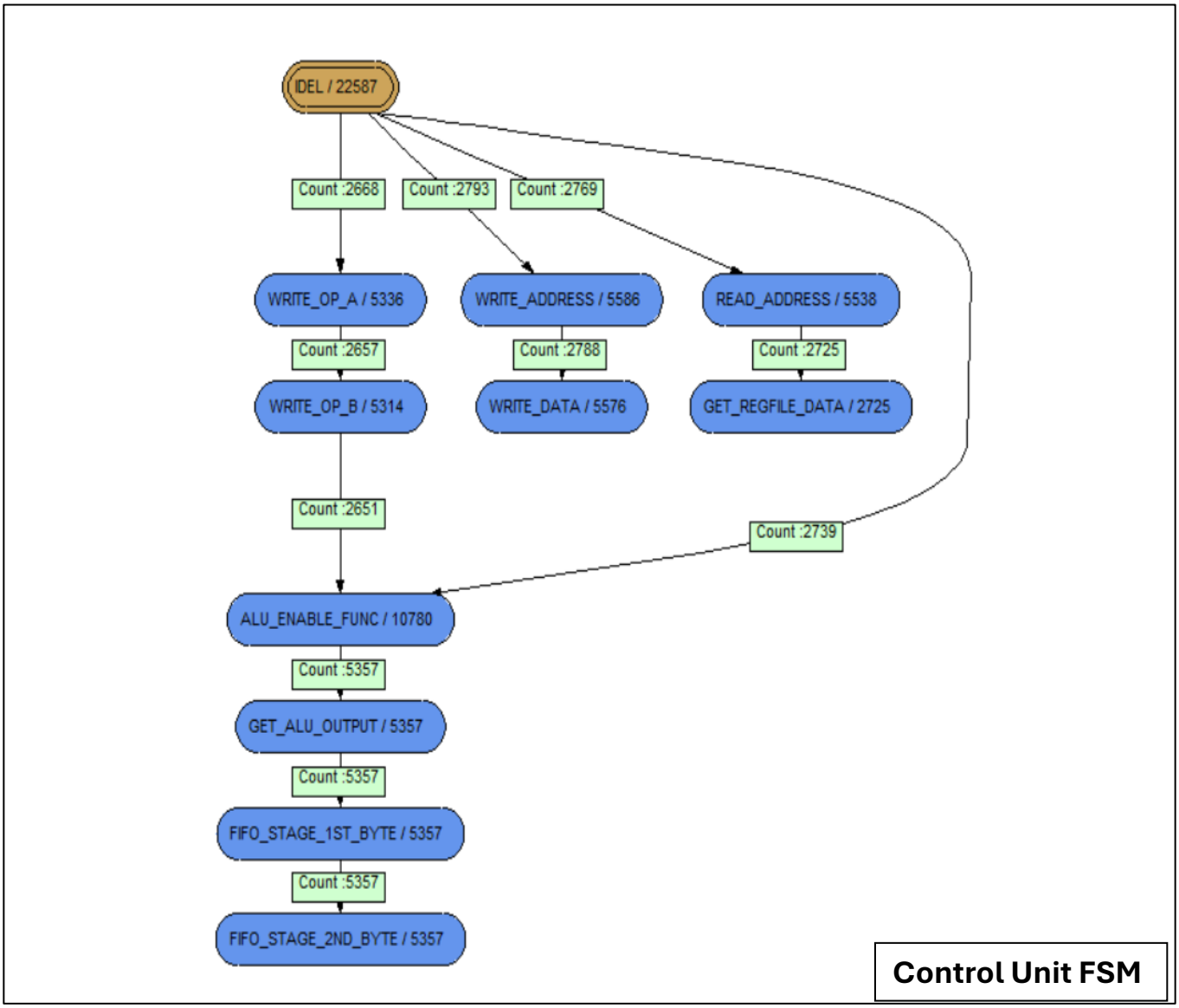
Functional Coverage

Name	Coverage	Goal	% of Goal	Status	% over Goal	Included	BinRHS
/SYS_COV_COLLECTOR/SYS_COV_C...	100.00%						
TYPE COV_GP	100.00%	100	100.00...		100.00%		
CVP COV_GP::CP_1	100.00%	100	100.00...		100.00%		
bin A1[0]	89976305	1	100.00...		...0500.00...		0
bin A1[1]	126824127	1	100.00...		...2700.00...		1
CVP COV_GP::CP_2	100.00%	100	100.00...		100.00%		
bin B1[0]	4359414	1	100.00...		...1400.00...		0
bin B1[1]	212441018	1	100.00...		...1800.00...		1
CVP COV_GP::CP_3	100.00%	100	100.00...		100.00%		
bin C1[4]	23847709	1	100.00...		...0900.00...		4
bin C1[8]	26909768	1	100.00...		...6800.00...		8
bin C1[16]	37205091	1	100.00...		...9100.00...		16
bin C1[32]	128837864	1	100.00...		...6400.00...		32
bin C2	216800432	1	100.00...		...3200.00...		;8;16;32
CVP COV_GP::CP_4	100.00%	100	100.00...		100.00%		
bin D1[0]	216792596	1	100.00...		...9600.00...		0
bin D1[1]	2865	1	100.00...		286500.00...		1
bin D1[2]	468	1	100.00...		46800.00...		2
bin D1[3]	557	1	100.00...		55700.00...		3
bin D1[4]	325	1	100.00...		32500.00...		4
bin D1[5]	340	1	100.00...		34000.00...		5
bin D1[6]	319	1	100.00...		31900.00...		6
bin D1[7]	338	1	100.00...		33800.00...		7
bin D1[8]	330	1	100.00...		33000.00...		8
bin D1[9]	328	1	100.00...		32800.00...		9
bin D1[10]	348	1	100.00...		34800.00...		10
bin D1[11]	296	1	100.00...		29600.00...		11
bin D1[12]	345	1	100.00...		34500.00...		12
bin D1[13]	317	1	100.00...		31700.00...		13
bin D1[14]	343	1	100.00...		34300.00...		14
bin D1[15]	318	1	100.00...		31800.00...		15
CVP COV_GP::CP_5	100.00%	100	100.00...		100.00%		
bin E1[170]	13912908	1	100.00...		...0800.00...		170
bin E1[187]	13822333	1	100.00...		...3300.00...		187
bin E1[204]	13321517	1	100.00...		...1700.00...		204
bin E2	41056758	1	100.00...		...5800.00...		...87;204
CVP COV_GP::CP_6	100.00%	100	100.00...		100.00%		
bin F1[0]	216795420	1	100.00...		...2000.00...		0
bin F1[1]	361	1	100.00...		36100.00...		1
bin F1[2]	317	1	100.00...		31700.00...		2
bin F1[3]	312	1	100.00...		31200.00...		3
bin F1[4]	337	1	100.00...		33700.00...		4
bin F1[5]	339	1	100.00...		33900.00...		5
bin F1[6]	353	1	100.00...		35300.00...		6
bin F1[7]	334	1	100.00...		33400.00...		7
bin F1[8]	359	1	100.00...		35900.00...		8
bin F1[9]	338	1	100.00...		33800.00...		9
bin F1[10]	318	1	100.00...		31800.00...		10
bin F1[11]	310	1	100.00...		31000.00...		11
bin F1[12]	341	1	100.00...		34100.00...		12
bin F1[13]	340	1	100.00...		34000.00...		13
bin F1[14]	348	1	100.00...		34800.00...		14
bin F1[15]	306	1	100.00...		30600.00...		15
bin F2	216800433	1	100.00...		...3300.00...		0:15
CROSS COV_GP::cross1	100.00%	100	100.00...		100.00%		
bin CRO_1	41056758	1	100.00...		...5800.00...		...2>;...
CROSS COV_GP::cross2	100.00%	100	100.00...		100.00%		
bin CRO_1	216800432	1	100.00...		...3200.00...		...2>;...

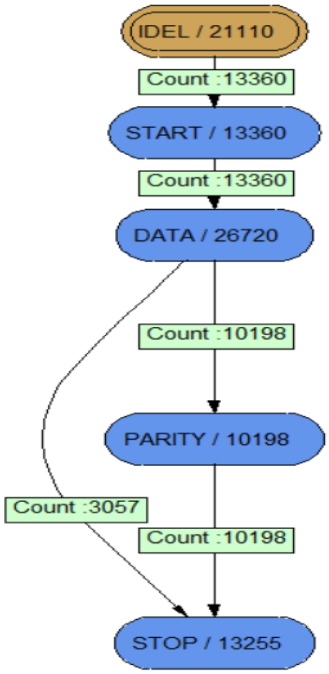
Code Coverage

Instance	Design unit	Design unit type	Total coverage	Cover %	Cover graph	Assertion %	Assertion graph	Stmt graph	Stmt %	Branch graph	Branch %	Toggle nodes	Toggle graph	Toggle %	State graph	State
/SYS_UVM_TOP/DUT_M/U11/Fifo_ASSER	FIFO_ASSER	Module	100.00%	100.00%		100.00%										
/SYS_UVM_TOP/DUT_M/U5/RF_Asser	REG_FILE_...	Module	100.00%	100.00%		100.00%										
/SYS_UVM_TOP/DUT_M/U4/CTRL_Asser	CTRL_Asse...	Module	100.00%	100.00%		100.00%										
/SYS_UVM_TOP/DUT_M/U0/UART_ASSERTION...	UART_Ass...	Module	100.00%	100.00%		100.00%										
/SYS_UVM_TOP/DUT_M/U11/M2_W	SYNC	Module	100.00%						100.00%		100.00%	36		100.00%		
/SYS_UVM_TOP/DUT_M/U11/M1_R	SYNC	Module	100.00%						100.00%		100.00%	36		100.00%		
/SYS_UVM_TOP/DUT_M/U11/M0	FIFO_RD	Module	100.00%						100.00%		100.00%	38		100.00%		
/SYS_UVM_TOP/DUT_M/U10	PULSE_GEN	Module	100.00%						100.00%		100.00%	10		100.00%		
/SYS_UVM_TOP/DUT_M/U8	CLK_GATE	Module	100.00%						100.00%		100.00%	8		100.00%		
/SYS_UVM_TOP/DUT_M/U7	ALU	Module	100.00%						100.00%		100.00%	114		100.00%		
/SYS_UVM_TOP/DUT_M/U3/U3	DFF	Module	100.00%						100.00%		100.00%	36		100.00%		
/SYS_UVM_TOP/DUT_M/U0/TX/V3	TX_PARITY	Module	100.00%						100.00%		100.00%	24		100.00%		
/SYS_UVM_TOP/DUT_M/U0/TX/V4	TX_Serializer	Module	100.00%						100.00%		100.00%	32		100.00%		
/SYS_UVM_TOP/DUT_M/U3/U1	PULSE_GEN	Module	100.00%						100.00%		100.00%	10		100.00%		
/SYS_UVM_TOP/DUT_M/U9/genblk1[1]/genblk1...	DFF	Module	100.00%						100.00%		100.00%	8		100.00%		
/SYS_UVM_TOP/DUT_M/U6/genblk1[1]/genblk1...	DFF	Module	100.00%						100.00%		100.00%	8		100.00%		
/SYS_UVM_TOP/DUT_M/U3/U2	DFF	Module	100.00%						100.00%		100.00%	8		100.00%		
/SYS_UVM_TOP/DUT_M/U3/genblk1[1]/genblk1...	DFF	Module	100.00%						100.00%		100.00%	8		100.00%		
/SYS_UVM_TOP/DUT_M/U3/genblk1[0]/genblk1...	DFF	Module	100.00%						100.00%		100.00%	8		100.00%		
/SYS_UVM_TOP/DUT_M/U3	DATA_SYNC	Module	100.00%						100.00%		100.00%	62		100.00%		
/SYS_UVM_TOP/DUT_M/U0/TX	TX_TOP	Module	98.53%						100.00%		100.00%	68		94.12%		
/SYS_UVM_TOP/DUT_M/U11/M3	FIFO_WR	Module	93.68%						100.00%		100.00%	38		94.74%		
/SYS_UVM_TOP/DUT_M/U0/RX/M1	RX_deseria...	Module	93.48%						100.00%		100.00%	46		73.91%		
/SYS_UVM_TOP/DUT_M/U0/RX/M2	RX_edge_c...	Module	92.11%						100.00%		100.00%	38		68.42%		
/SYS_UVM_TOP/DUT_M/U6/genblk1[0]/genblk1...	DFF	Module	91.67%						100.00%		100.00%	8		75.00%		
/SYS_UVM_TOP/DUT_M/U11/M4	FIFO_RAM	Module	91.92%						100.00%		100.00%	66		75.76%		
/SYS_UVM_TOP/DUT_M/U9/genblk1[0]/genblk1...	DFF	Module	91.67%						100.00%		100.00%	8		75.00%		
/SYS_UVM_TOP/DUT_M/U0/TX/V2	TX_mux	Module	90.48%						100.00%		100.00%	14		71.43%		
/SYS_UVM_TOP/DUT_M/U0/RX/M5	RX_stop_chk	Module	89.06%						100.00%		100.00%	32		56.25%		
/SYS_UVM_TOP/DUT_M/U0/RX/M6	RX_start_chk	Module	89.06%						100.00%		100.00%	32		56.25%		
/SYS_UVM_TOP/DUT_M/U5	REG_FILE	Module	87.28%						100.00%		100.00%	114		82.46%		
/SYS_UVM_TOP/DUT_M/U0/RX/M0	RX_data_s...	Module	87.03%						100.00%		100.00%	74		35.14%		
/SYS_UVM_TOP	SYS_UVM_...	Module	82.14%						100.00%			56		64.29%		
/SYS_UVM_TOP/DUT_M/U0/RX/M3	RX_FSM	Module	82.45%						97.14%		95.24%	72		77.78%		100.0
/SYS_UVM_TOP/DUT_M/U0	UART	Module	81.08%									74		81.08%		
/SYS_UVM_TOP/DUT_M/U0/RX/M4	RX_parity_...	Module	81.04%						83.33%		88.89%	52		76.92%		
/SYS_UVM_TOP/DUT_M/U9	RST_SYNC	Module	80.00%									10		80.00%		
/SYS_UVM_TOP/DUT_M/U0/RX	RX_TOP	Module	80.00%									80		80.00%		
/SYS_UVM_TOP/DUT_M/U6	RST_SYNC	Module	80.00%									10		80.00%		
/SYS_UVM_TOP/DUT_M/U4	SYS_CONT...	Module	77.55%						97.14%		93.06%	234		84.62%		100.0
/SYS_UVM_TOP/DUT_M/U0/TX/V1	TX_FSM	Module	75.33%						85.71%		88.46%	36		100.00%		100.0
/SYS_UVM_TOP/DUT_M/U11	FIFO_TOP	Module	73.91%									92		97.83%		

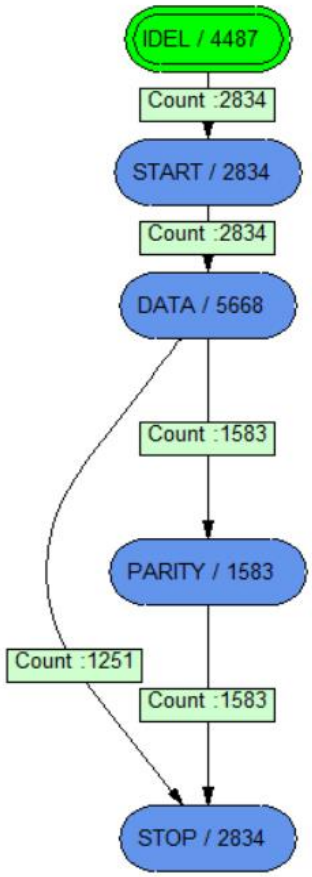
FSM Coverage



RX Unit FSM



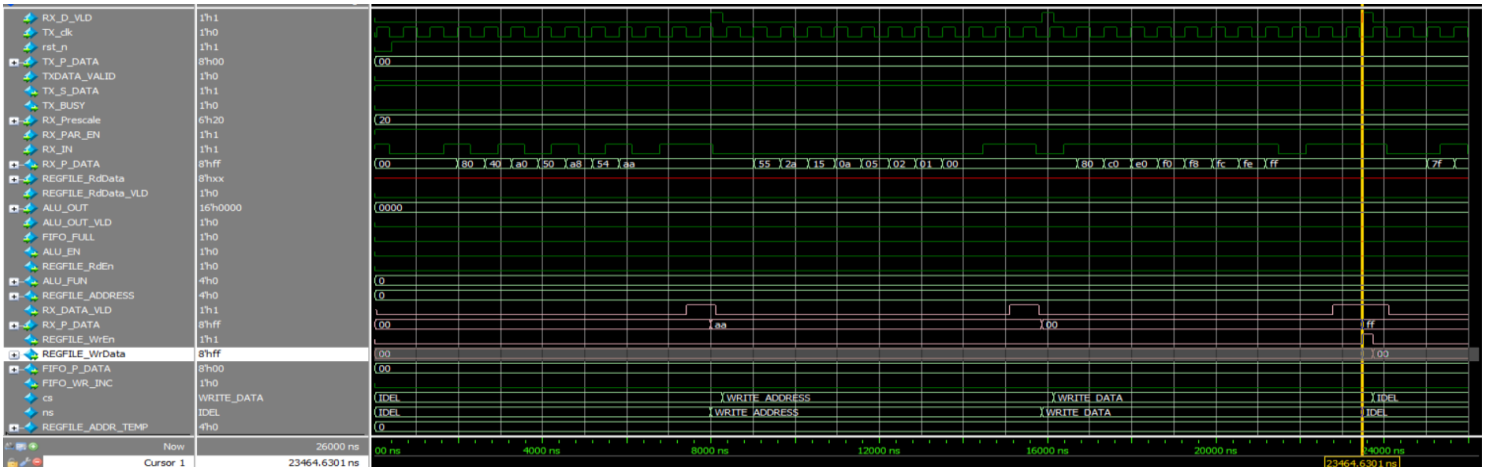
TX Unit FSM



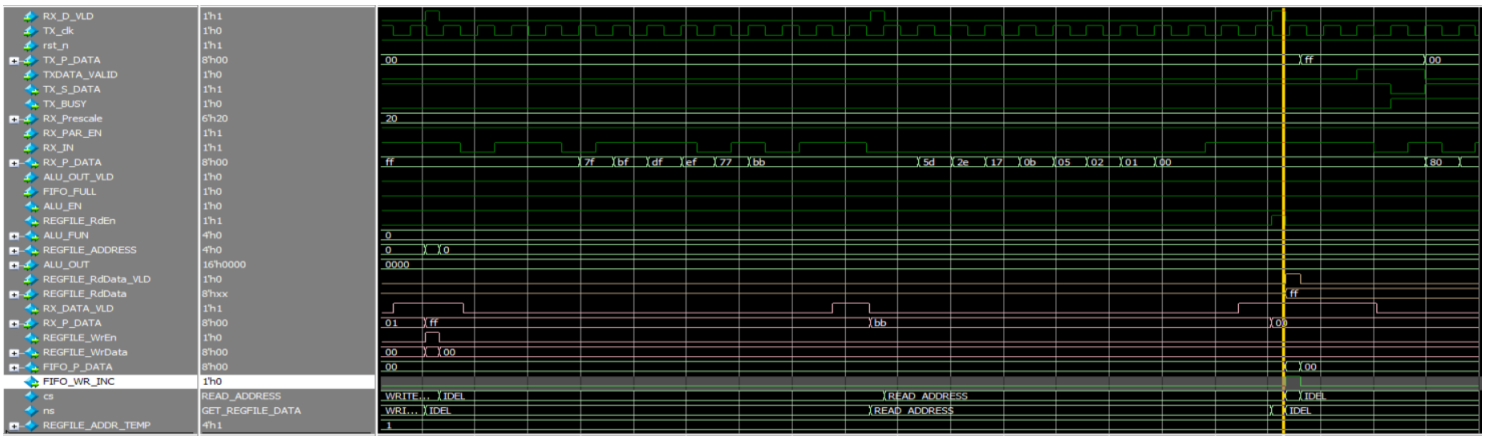
Simulation Results Waveform

Default Configurations

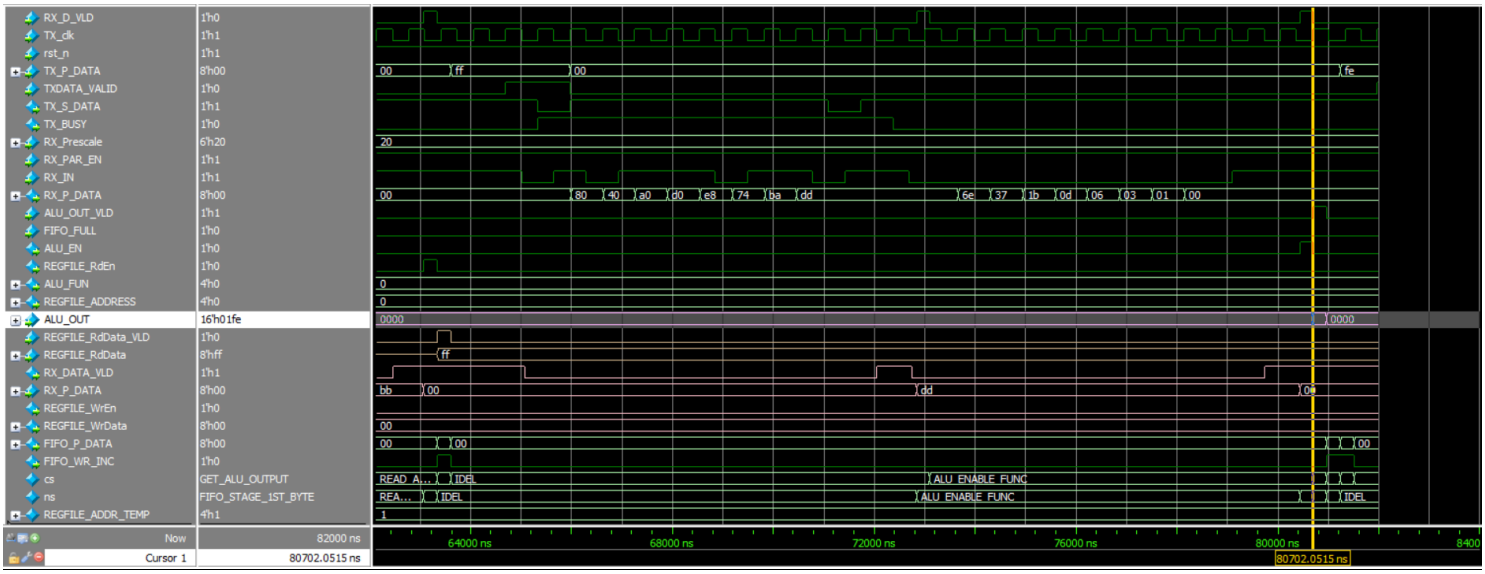
Write Operation



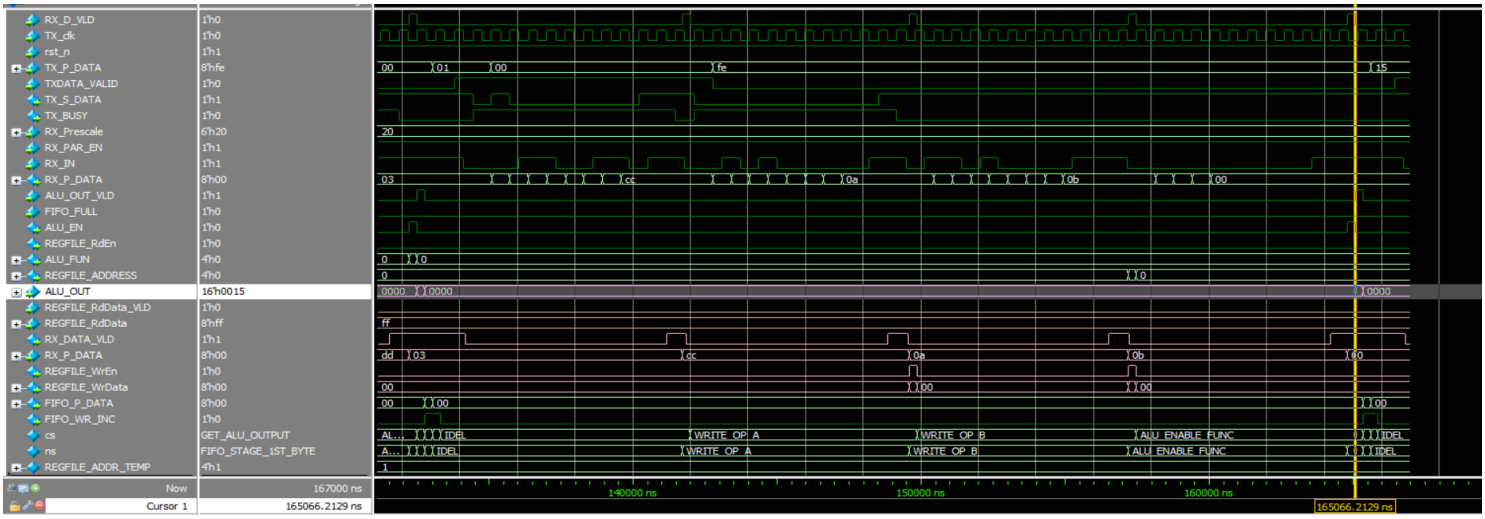
Read Operation



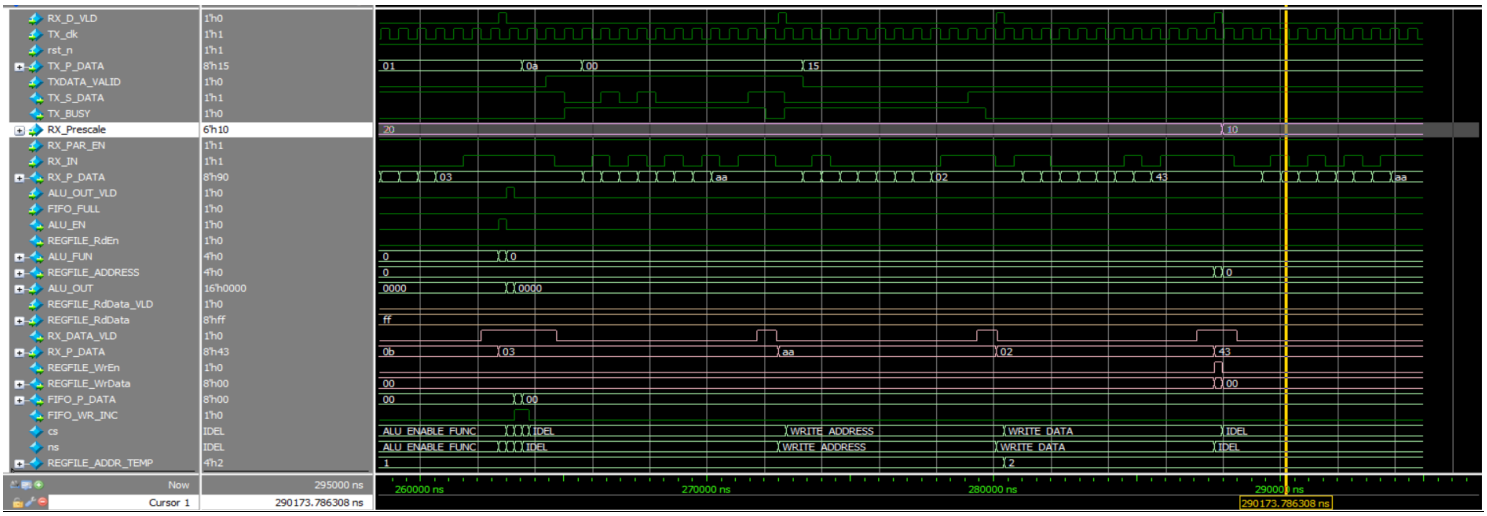
Alu Addition with No Operands



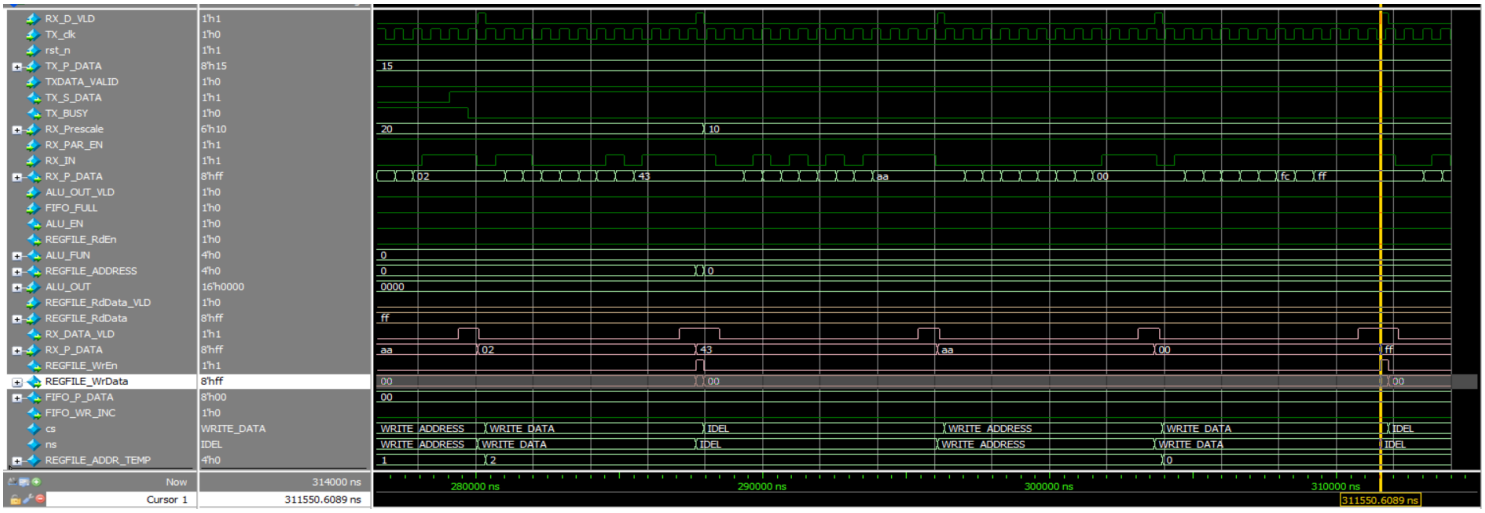
Alu Addition with External Operands



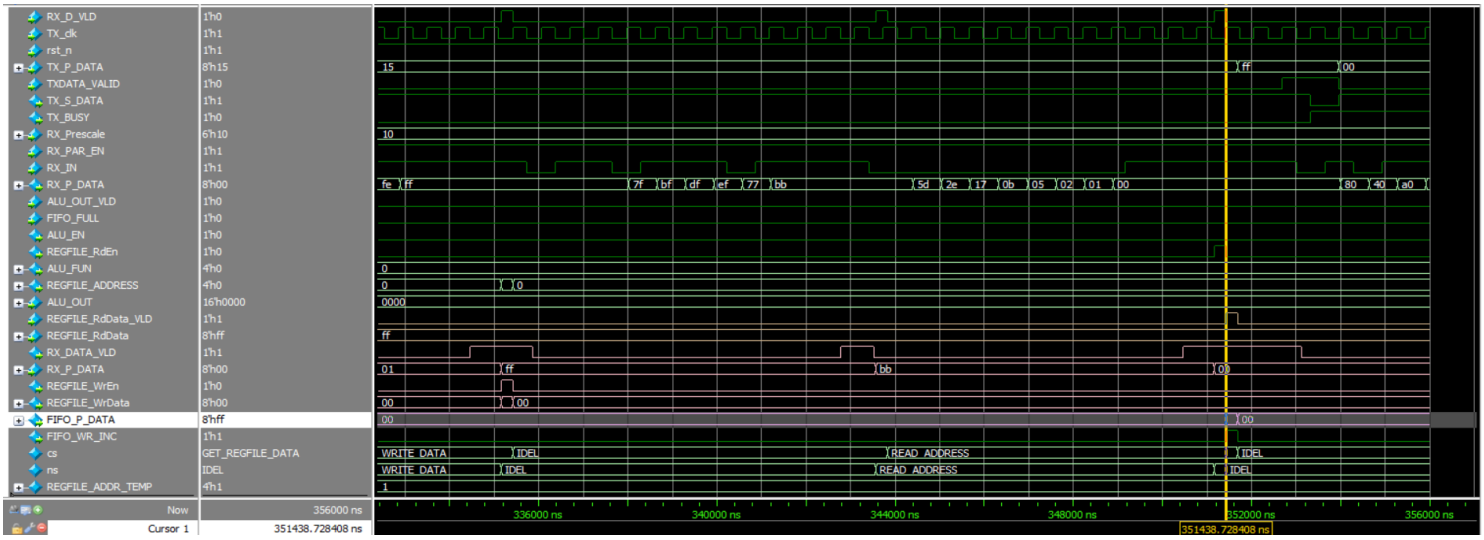
System Reconfiguration



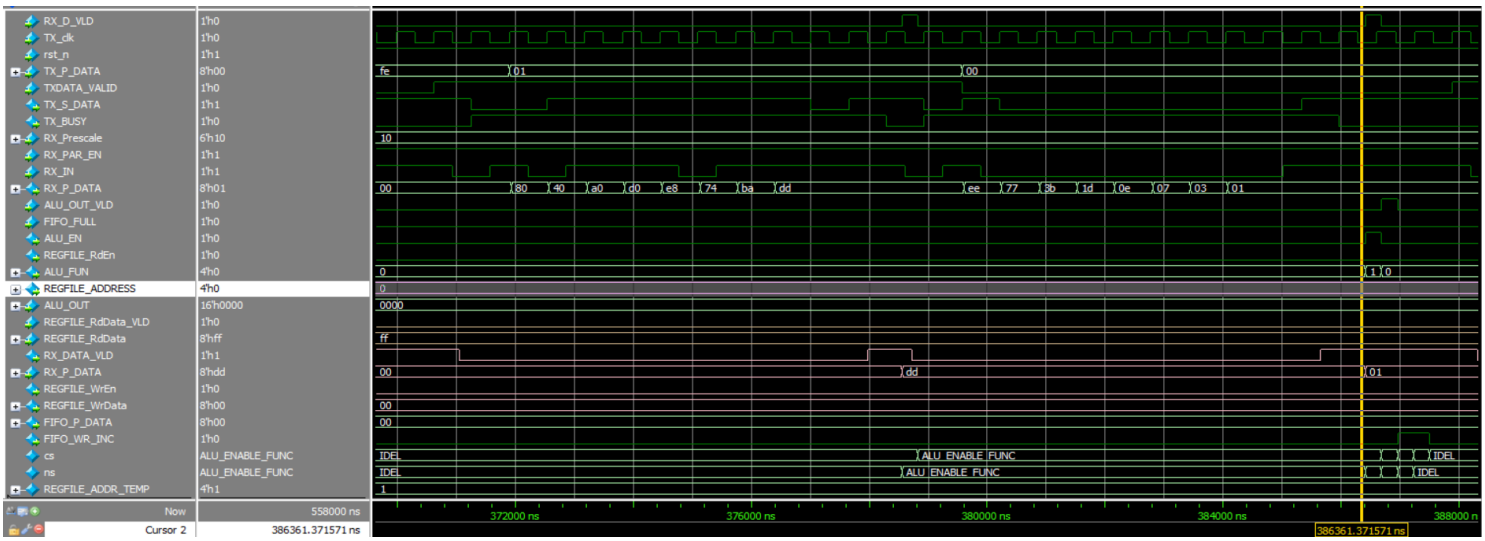
Write Operation After reconfiguration



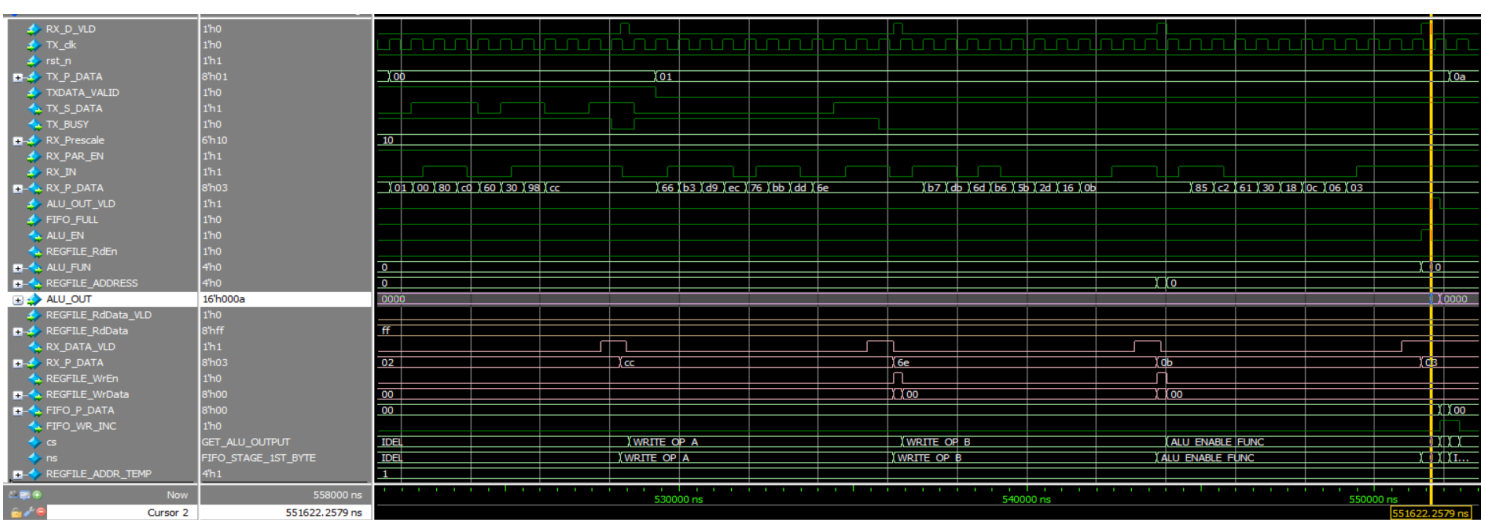
Read Operation After reconfiguration



Alu Subtraction with No Operands After reconfiguration



Alu Addition with External Operands After reconfiguration



Simulation Results in Transcript

```
# ************************ Default Configrations*************************
# ***********************************************************************
# WRITE TEST ---> DONE
# WRITE TEST ---> DONE
# READ TEST ---> DONE
# ADD WITH NO OPERANS---> DONE
# SUB WITH NO OPERANS---> DONE
# MUL WITH NO OPERANS---> DONE
# DIV WITH NO OPERANS---> DONE
# ADD WITH EXTERNAL OPERANDS---> DONE
# SUB WITH EXTERNAL OPERANDS---> DONE
# MUL WITH EXTERNAL OPERANDS---> DONE
# DIV WITH EXTERNAL OPERANDS---> DONE
# ************************ CHANGED Configrations*************************
# ***********************************************************************
# -----RECONFIG TEST ---> DONE
# WRITE TEST ---> DONE
# WRITE TEST ---> DONE
# READ TEST ---> DONE
# ADD WITH NO OPERANS---> DONE
# SUB WITH NO OPERANS---> DONE
# MUL WITH NO OPERANS---> DONE
# DIV WITH NO OPERANS---> DONE
# ADD WITH EXTERNAL OPERANDS---> DONE
# SUB WITH EXTERNAL OPERANDS---> DONE
# MUL WITH EXTERNAL OPERANDS---> DONE
# DIV WITH EXTERNAL OPERANDS---> DONE
# ******************SIMULATION END ---> DONE :) s:)****************************
# ** Note: $stop    : E:/K.O/Crocodile/System/ALL/SYS_TB.sv(370)
#    Time: 553010 ns  Iteration: 4  Instance: /SYS_TB
# Break in Module SYS_TB at E:/K.O/Crocodile/System/ALL/SYS_TB.sv line 370
```

RegFile Content After Simulation	
0000000f	00
0000000e	00
0000000d	00
0000000c	00
0000000b	00
0000000a	00
00000009	00
00000008	00
00000007	00
00000006	00
00000005	00
00000004	00
00000003	20
00000002	43
00000001	0b
00000000	6e

FIFO Content After Simulation	
00000007	00
00000006	6e
00000005	00
00000004	04
00000003	00
00000002	15
00000001	00
00000000	0a

Synthesis Results

Constraints Report

```

****************************************
Report : constraint
         -all_violators
Design : SYS_TOP
Version: K-2015.06
Date   : Wed Aug 21 08:55:33 2024
****************************************

This design has no violated constraints.

1

```

Clocks report

```

***************************************
Report : clocks
Design : SYS_TOP
Version: K-2015.06
Date   : Wed Aug 21 08:55:33 2024
***************************************

Attributes:
    d - dont_touch_network
    f - fix_hold
    p - propagated_clock
    G - generated_clock
    g - lib_generated_clock

Clock          Period   Waveform            Attrs     Sources
--------------------------------------------------------------------------------
ALU_CLK         20.00   {0 10}              G         {U8/GATED_CLK}
REF_CLK         20.00   {0 10}                        {REF_CLK}
SCAN_CLK       100.00   {0 50}                        {scan_clk}
UART_CLK       271.27   {0 135.633}                   {UART_CLK}
UART_RX_CLK    271.27   {0 135.633}          G        {U2_RX/o_div_clk}
UART_TX_CLK   8680.54   {0 4340.27}          G        {U1_TX/o_div_clk}
--------------------------------------------------------------------------------

Generated      Master         Generated      Master         Waveform
Clock          Source         Source         Clock          Modification
--------------------------------------------------------------------------------
ALU_CLK        REF_CLK        {U8/GATED_CLK} REF_CLK        divide_by(1)
UART_RX_CLK    UART_CLK       {U2_RX/o_div_clk}
                                             UART_CLK       divide_by(1)
UART_TX_CLK    UART_CLK       {U1_TX/o_div_clk}
                                             UART_CLK       divide_by(32)
--------------------------------------------------------------------------------
1

```

Area Report

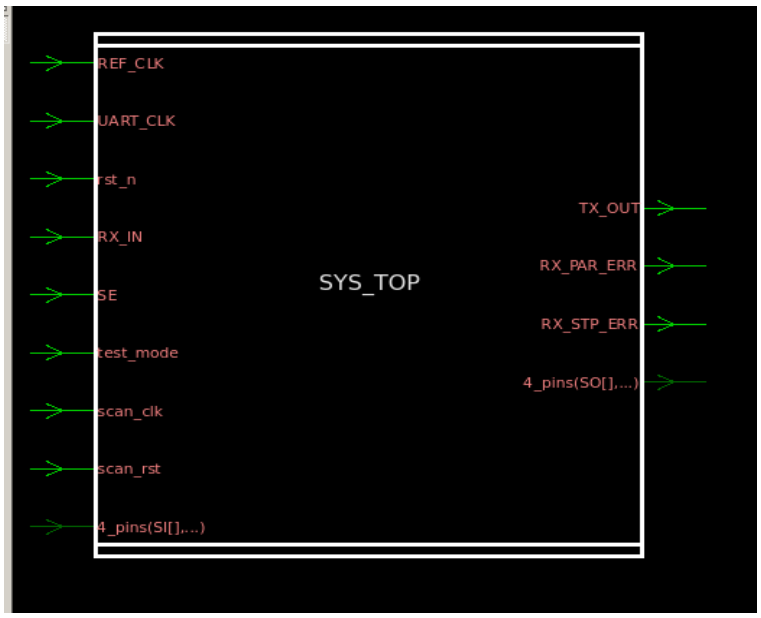
```
****************************************
Report : area
Design : SYS_TOP
Version: K-2015.06
Date   : Wed Aug 21 08:55:33 2024
****************************************

Library(s) Used:

    scmetro_tsmc_cl013g_rvt_ss_1p08v_125c (File: /home/IC/SYSTEM/sys_dft/std_cells/scmetro_tsmc_cl013g_rvt_ss_1p08v_125c.db)

Number of ports:                          945
Number of nets:                          2864
Number of cells:                         1899
Number of combinational cells:           1495
Number of sequential cells:               355
Number of macros/black boxes:               0
Number of buf/inv:                        285
Number of references:                      32

Combinational area:              13927.421438
Buf/Inv area:                     1139.045622
Noncombinational area:           11352.801991
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 25280.223428
Total area:                 undefined
```

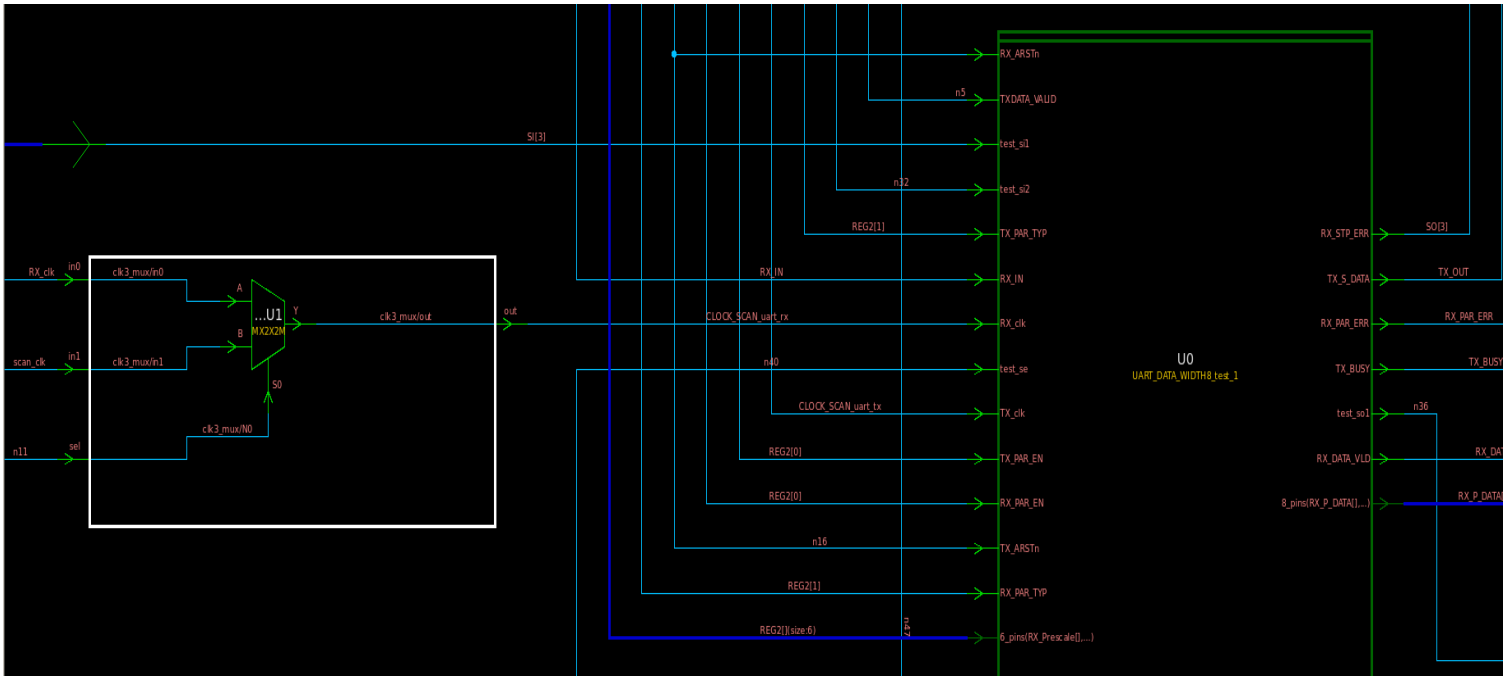
```
--------------------------------
Hierarchical cell                 Absolute    Percent  Combi-      Noncombi-   Black-
--------------------------------  ----------  -------  ----------  ----------  ------  ------------------------------------
SYS_TOP                           25280.2234    100.0    172.9749      0.0000  0.0000  SYS_TOP
U0                                 3797.2110     15.0      9.4136      0.0000  0.0000  UART_DATA_WIDTH8_test_1
U0/RX                              2893.5054     11.4     14.1204      0.0000  0.0000  RX_TOP_test_1
U0/RX/M0                            610.7073      2.4    511.8645     98.8428  0.0000  RX_data_sampling_test_1
U0/RX/M1                            433.0256      1.7    169.4448    263.5808  0.0000  RX_deserializer_test_1
U0/RX/M2                            650.7151      2.6    354.1867    296.5284  0.0000  RX_edge_counter_test_1
U0/RX/M3                            508.3344      2.0    376.5440    131.7904  0.0000  RX_FSM_test_1
U0/RX/M4                            290.6449      1.1    248.2837     42.3612  0.0000  RX_parity_check_test_1
U0/RX/M5                            209.4526      0.8    167.0914     42.3612  0.0000  RX_stop_chk_test_1
U0/RX/M6                            176.5050      0.7    143.5574     32.9476  0.0000  RX_start_chk_test_1
U0/TX                               894.2920      3.5    102.3729    263.5808  0.0000  TX_TOP_DATA_WIDTH8_test_1
U0/TX/V1                            181.2118      0.7     82.3690     98.8428  0.0000  TX_FSM_test_1
U0/TX/V2                             42.3612      0.2     42.3612      0.0000  0.0000  TX_mux
U0/TX/V3                             92.9593      0.4     92.9593      0.0000  0.0000  TX_PARITY
U0/TX/V4                            211.8060      0.8    116.4933     95.3127  0.0000  TX_Serializer_test_1
U10                                  38.8311      0.2      5.8835     32.9476  0.0000  PULSE_GEN_test_1
U11                                4524.4117     17.9     12.9437      0.0000  0.0000  FIFO_TOP_DATA_WIDTH8_MEM_DEPTH8_test_1
U11/M0                              310.6488      1.2    177.6817    132.9671  0.0000  FIFO_RD_test_1
U11/M1_R                            263.5808      1.0      0.0000    263.5808  0.0000  SYNC_test_0
U11/M2_W                            263.5808      1.0      0.0000    263.5808  0.0000  SYNC_test_1
U11/M3                              292.9983      1.2    160.0312    132.9671  0.0000  FIFO_WR_test_1
U11/M4                             3380.6592     13.4   1262.5991   2118.0601  0.0000  FIFO_RAM_test_1
U1_TX                               823.6900      3.3    436.5557    295.3517  0.0000  CLK_DIV_test_0
U1_TX/add_48                         91.7826      0.4     91.7826      0.0000  0.0000  CLK_DIV_0_DW01_inc_0
U2_RX                               823.6900      3.3    436.5557    295.3517  0.0000  CLK_DIV_test_1
U2_RX/add_48                         91.7826      0.4     91.7826      0.0000  0.0000  CLK_DIV_1_DW01_inc_0
U3                                  480.0936      1.9     78.8389      0.0000  0.0000  DATA_SYNC_NUM_STAGES2_BUS_WIDTH8_test_1
U3/U1                                38.8311      0.2      5.8835     32.9476  0.0000  PULSE_GEN_test_0
U3/U2                                32.9476      0.1      0.0000     32.9476  0.0000  DFF_test_0
U3/U3                               263.5808      1.0      0.0000    263.5808  0.0000  DFF_BUS_WIDTH8_test_1
U3/genblk1[0].genblk1.U0             32.9476      0.1      0.0000     32.9476  0.0000  DFF_test_1
U3/genblk1[1].genblk1.U0             32.9476      0.1      0.0000     32.9476  0.0000  DFF_test_2
U4                                 1556.7741      6.2    751.9113    804.8628  0.0000  SYS_CONTROL_test_1
U5                                 7133.1557     28.2   2613.4508   4519.7049  0.0000  REG_FILE_test_1
U6                                   65.8952      0.3      0.0000     65.8952  0.0000  RST_SYNC_NUM_STAGES2_test_0
U7                                 5671.6941     22.4   1023.7290    560.1092  0.0000  ALU_test_1
U7/add_26                           231.8099      0.9    231.8099      0.0000  0.0000  ALU_DW01_add_0
U7/div_29                          1434.3973      5.7   1434.3973      0.0000  0.0000  ALU_DW_div_uns_0
U7/mult_28                         2155.7144      8.5   1914.4909      0.0000  0.0000  ALU_DW02_mult_0
U7/mult_28/FS_1                     241.2235      1.0    241.2235      0.0000  0.0000  ALU_DW01_add_1
U7/sub_27                           265.9342      1.1    265.9342      0.0000  0.0000  ALU_DW01_sub_0
U8                                   40.0078      0.2      0.0000     40.0078  0.0000  CLK_GATE
U9                                   65.8952      0.3      0.0000     65.8952  0.0000  RST_SYNC_NUM_STAGES2_test_1
clk1_mux                             15.2971      0.1     15.2971      0.0000  0.0000  mux_0
clk2_mux                             11.7670      0.0     11.7670      0.0000  0.0000  mux_6
clk3_mux                             11.7670      0.0     11.7670      0.0000  0.0000  mux_5
clk4_mux                             11.7670      0.0     11.7670      0.0000  0.0000  mux_4
rst1_mux                             11.7670      0.0     11.7670      0.0000  0.0000  mux_3
rst2_mux                             11.7670      0.0     11.7670      0.0000  0.0000  mux_2
rst3_mux                             11.7670      0.0     11.7670      0.0000  0.0000  mux_1
--------------------------------  ----------  -------  ----------  ----------  ------  ------------------------------------
Total                                                   13927.4214  11352.8020  0.0000

1
```

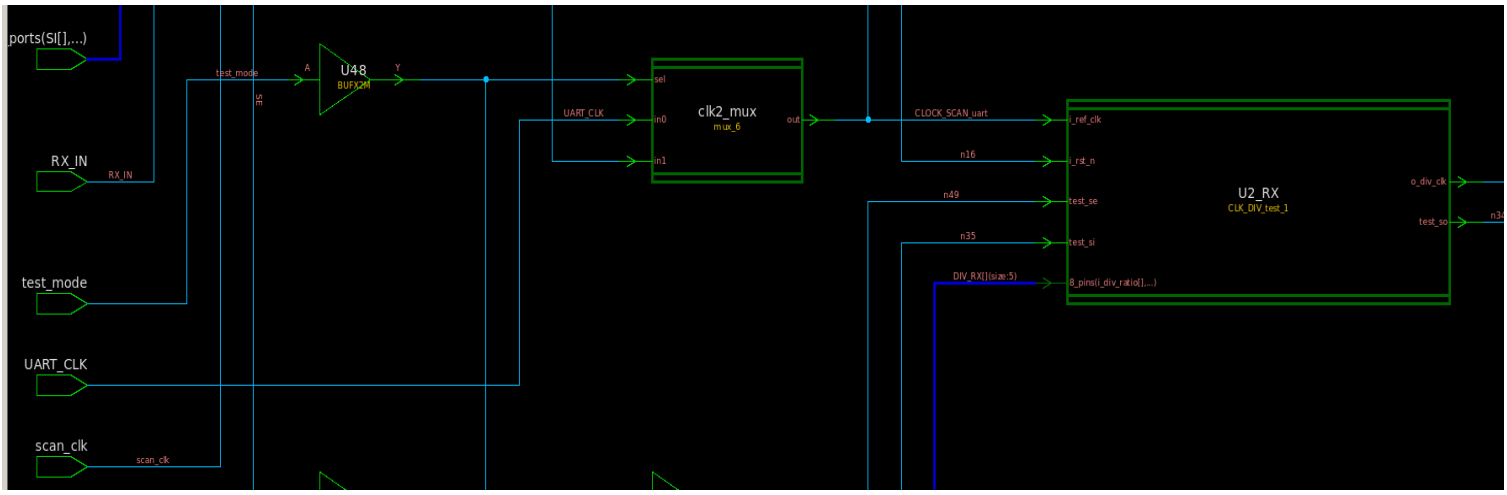
Power Report

```
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -hier
        -analysis_effort low
Design : SYS_TOP
Version: K-2015.06
Date   : Wed Aug 21 08:55:33 2024
****************************************


Library(s) Used:

    scmetro_tsmc_cl013g_rvt_ss_1p08v_125c (File: /home/IC/SYSTEM/sys_dft/std_cells/scmetro_tsmc_cl013g_rvt_ss_1p08v_125c.db)


Operating Conditions: scmetro_tsmc_cl013g_rvt_ss_1p08v_125c   Library: scmetro_tsmc_cl013g_rvt_ss_1p08v_125c
Wire Load Model Mode: top


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW

```

DFT Results


REF_CLK
UART_CLK
rst_n
RX_IN
SE
test_mode
scan_clk
scan_rst
4_pins(SI[],...)
SYS_TOP
TX_OUT
RX_PAR_ERR
RX_STP_ERR
4_pins(SO[],...)

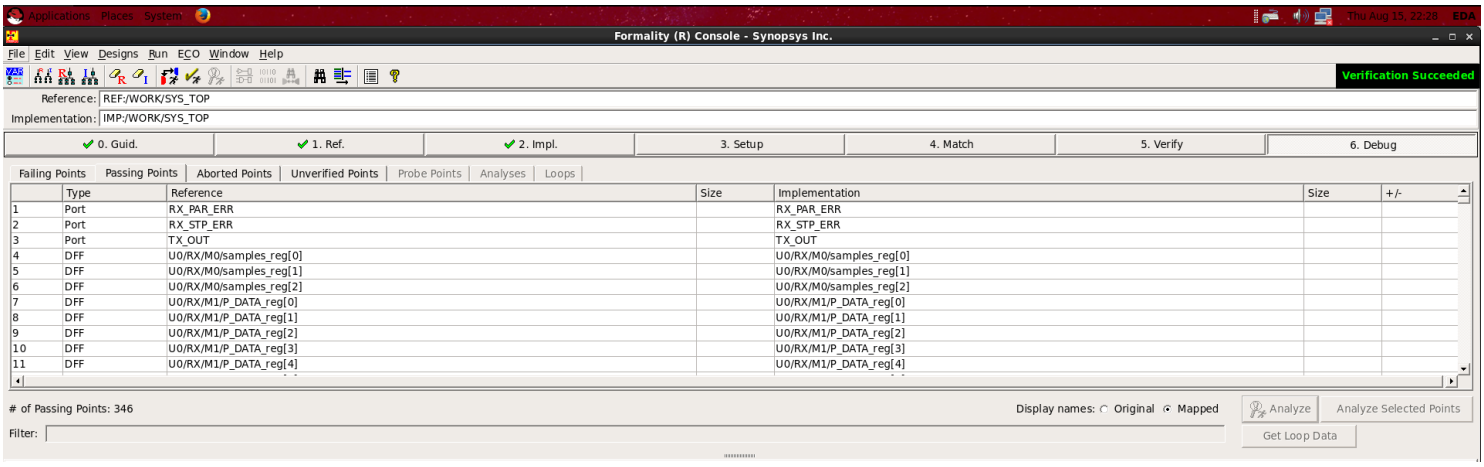

RX_clk
scan_clk
n11
clk3_mux/in0
clk3_mux/in1
clk3_mux/N0
...U1
MX2X2M
clk3_mux/out
SI[3]
RX_IN
CLOCK_SCAN_uart_rx
CLOCK_SCAN_uart_tx
REG2[0]
REG2[1]
n40
n16
n32
n5
RX_ARSTn
TXDATA_VALID
test_si1
test_si2
TX_PAR_TYP
RX_IN
RX_clk
test_se
TX_clk
TX_PAR_EN
RX_PAR_EN
TX_ARSTn
RX_PAR_TYP
6_pins(RX_Prescale[],...)
U0
UART_DATA_WIDTH8_test_1
RX_STP_ERR
TX_S_DATA
RX_PAR_ERR
TX_BUSY
test_so1
RX_DATA_VLD
8_pins(RX_P_DATA[],...)
SO[3]
TX_OUT
RX_PAR_ERR
TX_BUSY
n36


ports(SI[],...)
RX_IN
test_mode
UART_CLK
scan_clk
U48
BUFX2M
clk2_mux
mux_6
CLOCK_SCAN_uart
n16
n49
n35
DIV_RX[](size:5)
U2_RX
CLK_DIV_test_1
i_ref_clk
i_rst_n
test_se
test_si
8_pins(i_div_ratio[],...)
o_div_clk
test_so

```
    Uncollapsed Stuck Fault Summary Report
 -----------------------------------------------
 fault class                      code   #faults
 ------------------------------   ----  ---------
 Detected                          DT      15333
 Possibly detected                 PT          0
 Undetectable                      UD        192
 ATPG untestable                   AU         60
 Not detected                      ND         19
 -----------------------------------------------
 total faults                                15604
 test coverage                               99.49%
 -----------------------------------------------
  Information: The test coverage above may be inferior
               than the real test coverage with customized
               protocol and test simulation library.
1
```

Formality Post DFT Results

Comparison Results



	Type	Reference	Size	Implementation	Size	+/-
1	Port	RX_PAR_ERR		RX_PAR_ERR		
2	Port	RX_STP_ERR		RX_STP_ERR		
3	Port	TX_OUT		TX_OUT		
4	DFF	U0/RX/M0/samples_reg[0]		U0/RX/M0/samples_reg[0]		
5	DFF	U0/RX/M0/samples_reg[1]		U0/RX/M0/samples_reg[1]		
6	DFF	U0/RX/M0/samples_reg[2]		U0/RX/M0/samples_reg[2]		
7	DFF	U0/RX/M1/P_DATA_reg[0]		U0/RX/M1/P_DATA_reg[0]		
8	DFF	U0/RX/M1/P_DATA_reg[1]		U0/RX/M1/P_DATA_reg[1]		
9	DFF	U0/RX/M1/P_DATA_reg[2]		U0/RX/M1/P_DATA_reg[2]		
10	DFF	U0/RX/M1/P_DATA_reg[3]		U0/RX/M1/P_DATA_reg[3]		
11	DFF	U0/RX/M1/P_DATA_reg[4]		U0/RX/M1/P_DATA_reg[4]		

```
********************************* Verification Results *********************************
Verification SUCCEEDED
   ATTENTION: synopsys_auto_setup mode was enabled.
              See Synopsys Auto Setup Summary for details.
---------------------------------------------------------
 Reference design: REF:/WORK/SYS_TOP
 Implementation design: IMP:/WORK/SYS_TOP
 346 Passing compare points
-----------------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop    BBNet     Cut     Port     DFF     LAT   TOTAL
-----------------------------------------------------------------------------------------
Passing (equivalent)           0       0       0       0        3     342       1     346
Failing (not equivalent)       0       0       0       0        0       0       0       0
*****************************************************************************************
1
```

Unverified Report

```
1   ***************************************************
2   Report          : unverified_points
3
4   Reference       : REF:/WORK/SYS_TOP
5   Implementation  : IMP:/WORK/SYS_TOP
6   Version         : L-2016.03-SP1
7   Date            : Thu Aug 15 22:09:22 2024
8   ***************************************************
9
10  No unverified compare points.
11
12  1
```

Fail Report

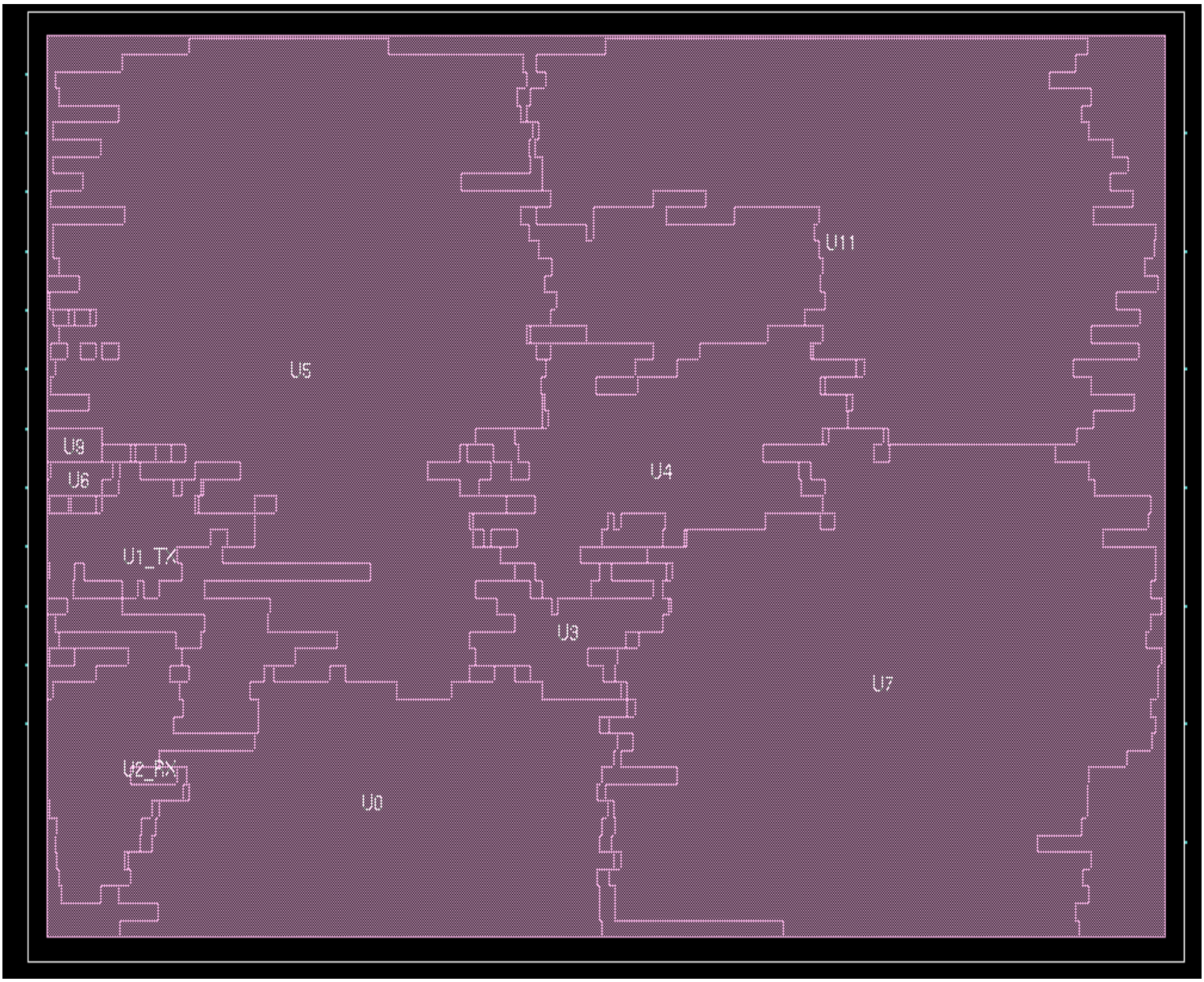
```
**************************************************
Report         : failing_points

Reference      : REF:/WORK/SYS_TOP
Implementation : IMP:/WORK/SYS_TOP
Version        : L-2016.03-SP1
Date           : Thu Aug 15 22:09:22 2024
**************************************************

No failing compare points.

1
```

Aborted Report

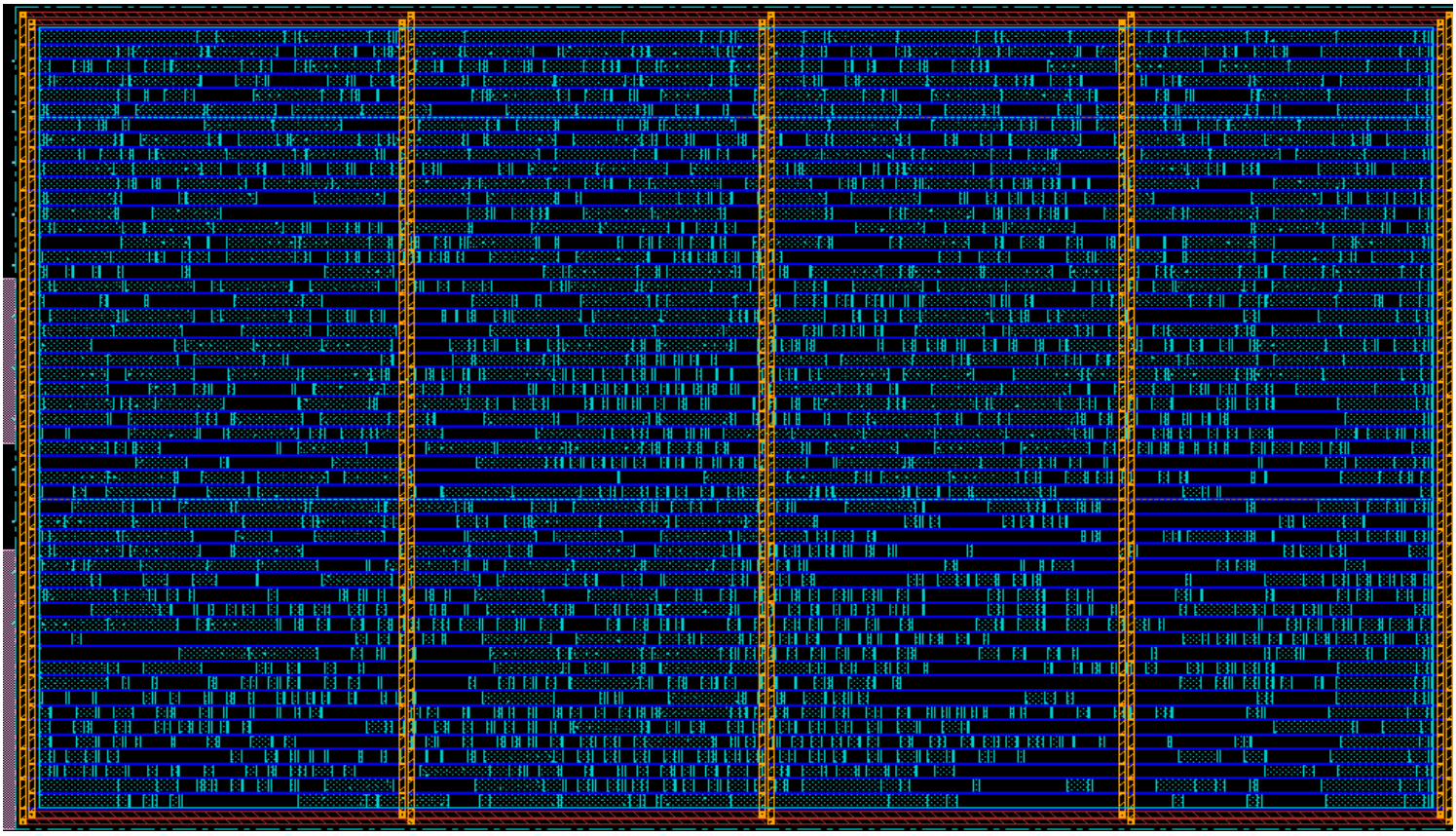
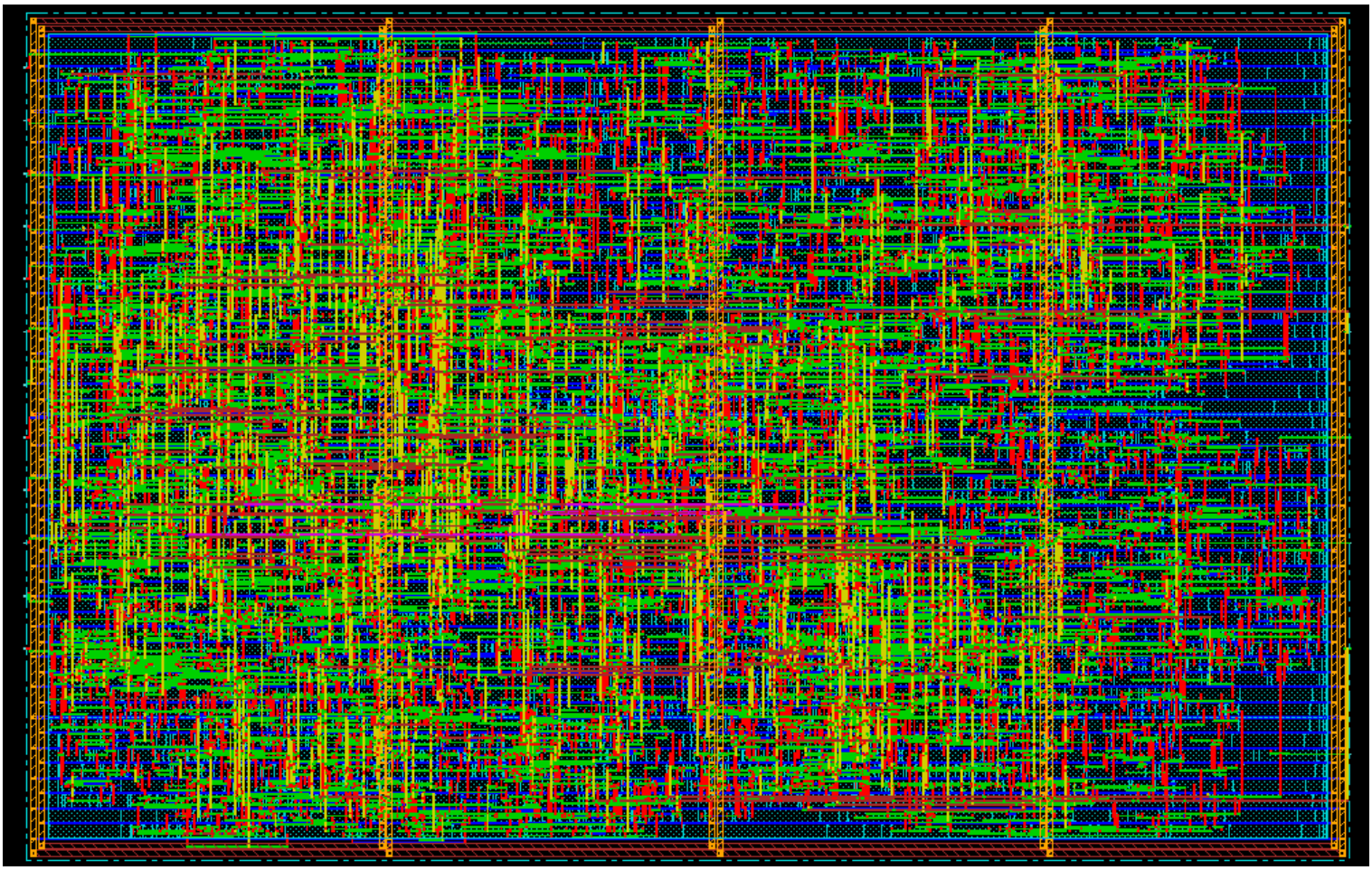
```
**************************************************
Report         : aborted_points

Reference      : REF:/WORK/SYS_TOP
Implementation : IMP:/WORK/SYS_TOP
Version        : L-2016.03-SP1
Date           : Thu Aug 15 22:09:22 2024
**************************************************

No aborted compare points.

1
```

PnR Results

Floor planning



Placing



Routing & Finishing