

Term Project - SIC/XE Assembler Phase (2)

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Requirements specification:

- The term project is to implement a (cross) assembler for (a subset of) SIC/XE assembler , written in C/C++ , producing code for the absolute loader used in the SIC/XE programming assignments.

The output of the assembler should include (at least):

The assembler is to execute by entering assemble <source-file-name>

The source file for the main program for this phase is to be named assemble.cpp

Object-code file whose format is the same as the one described in the text book in section 2.1.1 and 2.3.5.

EOU and ORG statements.

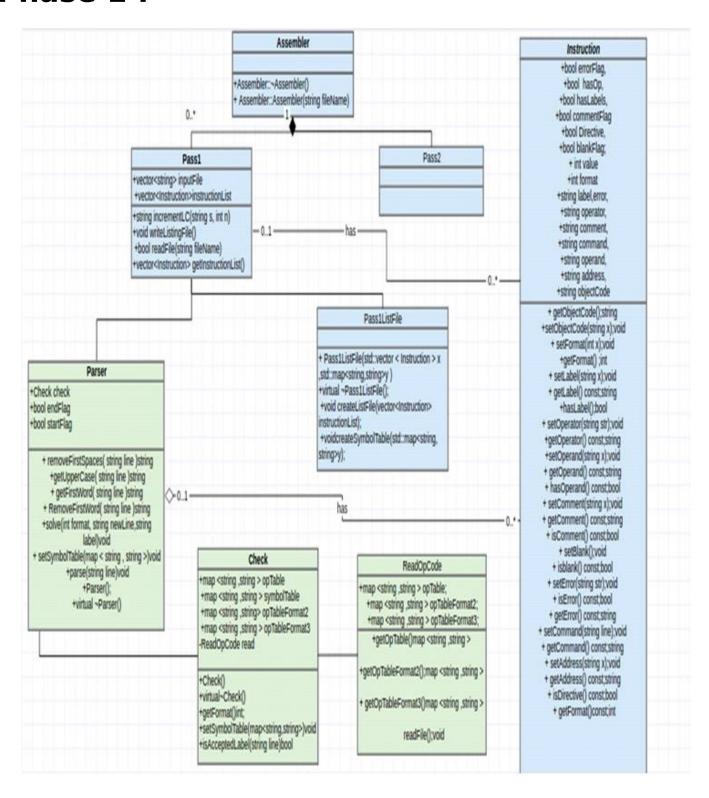
Simple expression evaluation. A simple expression includes simple (A<op>B) operand arithmetic, where <op> is one of +,-,*,/ and no spaces surround the operation, eg. A+B.

General expression evaluation.

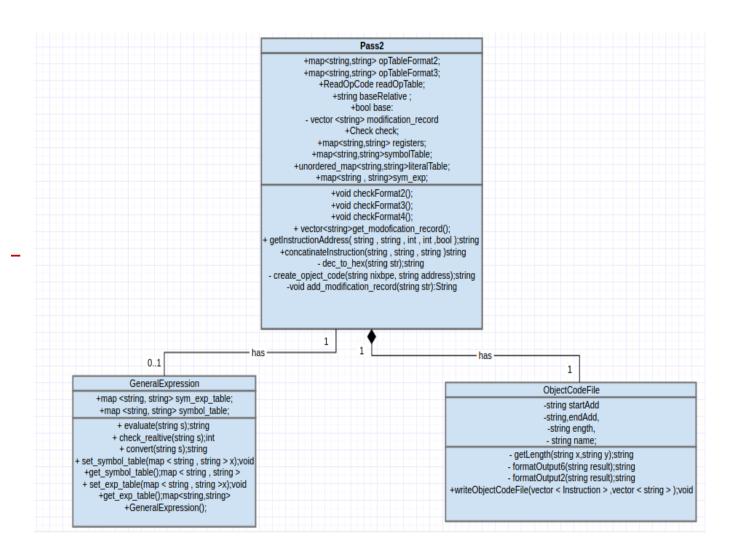
Literals (Including LTORG) =C'<ASCII-TEXT>', =X'HEX-TEXT', =<DECIMAL-TEXT> forms.

Design:

Phase 1:



Phase 2:



Main data structures:

map:

- map is a sorted associative container that contains key-value pairs with unique keys. Keys are sorted by using the comparison function Compare. Search, removal, and insertion operations have logarithmic complexity. Maps are usually implemented as red-black tree.
- we use it to store the op-Table , get the operator foramt , get operator op-code ,to store type of expression .

vector:

- vector is a sequence container that encapsulates dynamic size arrays.
- why we use it?
 - ➤ Random access constant *O(1)*
 - \triangleright Insertion or removal of elements at the end amortized constant O(1).
 - \triangleright Insertion or removal of elements linear in distance to the end of the vector O(n).
- we use it to store each instruction in it , to store modification record ,Store object code for each instruction .

Unordered Map:

- -get the value to corresponding key in order (1).
- -Using in literal table.

Algorithms description:

-validateInstruction(vector < Instruction > instructionList):

To check validation of all Instructions and separate them to corresponding validate format (format 2,3,4, directive).

-CheckFormat2():

To check validation of instructions of format 2 and generate its corresponding object code .

-checkFormat3():

To check validation of instructions of format 3 and generate its corresponding object code .

-checkFormat4():

To check validation of instructions of format 4 and generate its corresponding object code .

-dec to hex(string str):

To convert from decimal value to it's corresponding hex value .use it to calculate the displacement to generate object code .

<u>-add_modification_record(string_str):</u>

add modification record to vector of modification records .

-create object code(string nixbpe, string address):

To create object code to instructions of format 4.

-getInstructionAddress(string pc , string add , int flag, int format, bool isHex):

To get the displacement of instruction (last 3 bit in object code).

-get_modofication_record():

Return modification record vector, use it to print in object code file.

-concatinateInstruction(string opCode , string nixbpe , string address):

Concatenate between first 3 bits and last 3 bits in object code to generate the object code .

- GetInstructionList():

Return Instructions list after adding its object code to print object code file .

writeObjectCodeFile(std::vector < Instruction > x, std::vect or < string > modificationRecords):

Write object code file after validate its format.

- getLength(string x,string y):

Get the length of the code.

- formatOutput6(string result):

To update the format of 6 digits to print it in object code file.

- formatOutput2(string result):

To update the format of 2 digits to print it in object code file.

-void insertIntoLiteralTable(string operands) :

To insert into literal table.

- unordered_map < string , string > getLiteralTable()
return literal table .

void setLiteralTable(unordered_map<string , string > literal):

To set literal table.

void insertAddressIntoLiteralTable()

to set address for each literal after LTORG or END.

-string evaluate(string s) :

calculate the expression using postfix algorithm.

-int check_realtive(string s) :

check type of expression return 0 in case of absolute, 1 in case of relative, otherwise return -1.

-string convert(string s)

Check validation of expression usnig symbol table and get the address for each variable .

Assumptions:

- default start address equal zero in case not mentioned in the code.
- free format is handled.
- no comment is supported on the same line of code.
- code is case insensitive.
- line which has an error has won't be saved in memory.
- The operand for End instruction must be the same for Start Instruction .
- Base relative is handled .
- Literals are handled .
- General Expression is handled.
- Expressions don't have braces .
- No object code is case of corrupted code.
- The location for instructions which contain * have location for same instruction .
- Any number in operand field considered decimal.
- literals is defined with a name of it's value .
- in case of =* it's names with the *+address of instruction
- C'EOF' is different from x'454f46'

For format 4 can use immediate, indexing and direct addressing

Sample Runs:

```
1 copy start 0
 2 first stl retadr
 3 ldb #length
 4 base length
 5 cloop +jsub rdrec
 6 lda length
 7 comp
         #0
8 jeg endfil
 9 + jsub wrrec
10 j cloop
11 endfil lda EOF
12 sta buffer
13 lda #3
14 sta length
15 + j sub wrrec
16 j @retadr
17 eof byte c'EOF'
18 retadr resw 1
19 length resw 1
20 buffer resb 4096
21 rdrec clear x
22 clear a
23 clear s
24 +ldt #4096
```

```
27 rloop td input
28 jeg rloop
29 rd input
30 compr a,s
31 jeg exit
32 stch buffer,x
33 tixr t
34 jlt rloop
35 exit stx length
36 rsub
37 input byte x'F1'
38 wrrec clear x
39 ldt length
40 wloop td output
41 jeg wloop
42 ldch buffer,x
43 wd output
44 tixr t
45 jlt wloop
46 rsub
47 output byte x'05'
48 end copy
```

Sample Run 2:

```
7 PROB1
            START
                    Θ
            LDS
                    #0
            LDT
                    #10
10 TESTDEV
            TD
                    INDEV
            JEQ
                    TESTDEV
            LDA
                    #0
13
            RD
                    INDEV
            COMP
                    EOF
            JEQ
                    EXIT
            SUB
                     #48
18 .Test lower bound
19 LCHECK
            COMP
            JEQ
                    UCHECK
            JGT
                    UCHECK
            J
                    EXIT
24 .Test upper bound
25 UCHECK
            COMP
                    #10
            JLT
                    VNUMBER
            J
29 .valid number
30 VNUMBER MULR
                    T,S
            ADDR
                    A,S
            J
                    TESTDEV
33 EXIT
            RM0
                    S,A
34
            J
   .*****Assembler Directives****
36 INDEV
            BYTE
                    X'F3'
37 E0F
            WORD
                    4
38
            END
```

Sample run 3:

1	.2345678	90123456	7890123	
2	PROB3	START	0	
3		LDA	#0	HVAROR :
4	. READ T	ARGET CH	ARCACTER I	FROM DEVICE F2 .
5	TESTDEV2	TD	READCHAR	
6		JEQ	TESTDEV2	
7		RD		READCHAR
8		STA		TARGET
9	. READ S	TRING FR	OM DEVICE	F3 .
10		LDX	#0	
11	TESTDEV3	TD	READSTR	
12		JEQ	TESTDEV3)
13			LDA #0	9
14		RD		READSTR
15		STA	STRING,X	
16			COMP	TARGET
17		JEQ	FOUND	
18		COMP	E0T	
19		JEQ		
20		TIX	#256	
21			J	TESTDEV3
22	FOUND			
23			X,T	
24	EXIT	RM0	T,A	
25		J		8
			E X'F2	1
27	READSTR	BYTE	X'F3'	
28		1000	TARGET	RESW 1
1333	STRING		100	
100	EOT	WORD	4	
31		END		