CS 311 Computer Architecture

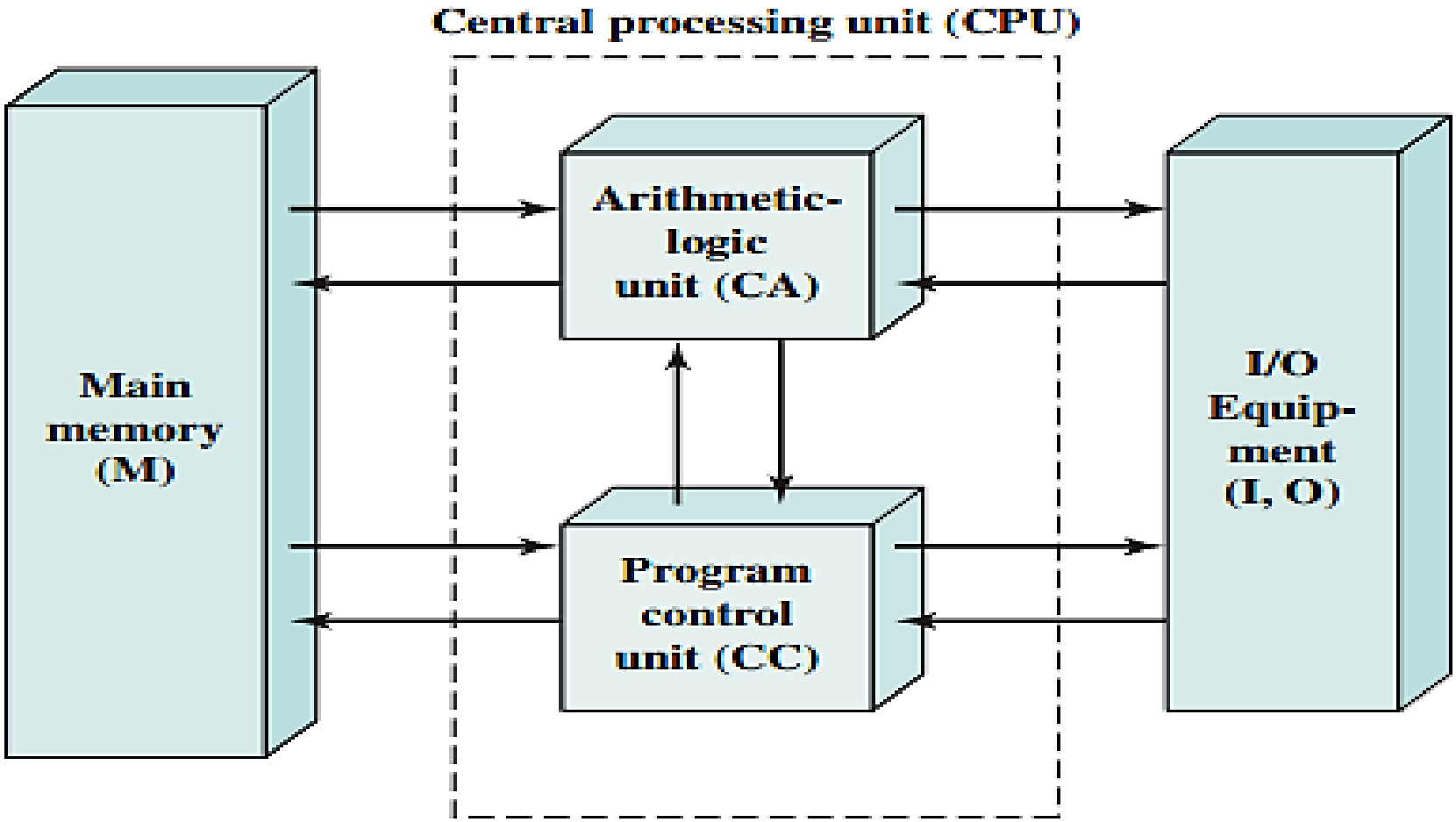
2025/2026

Lecture 2

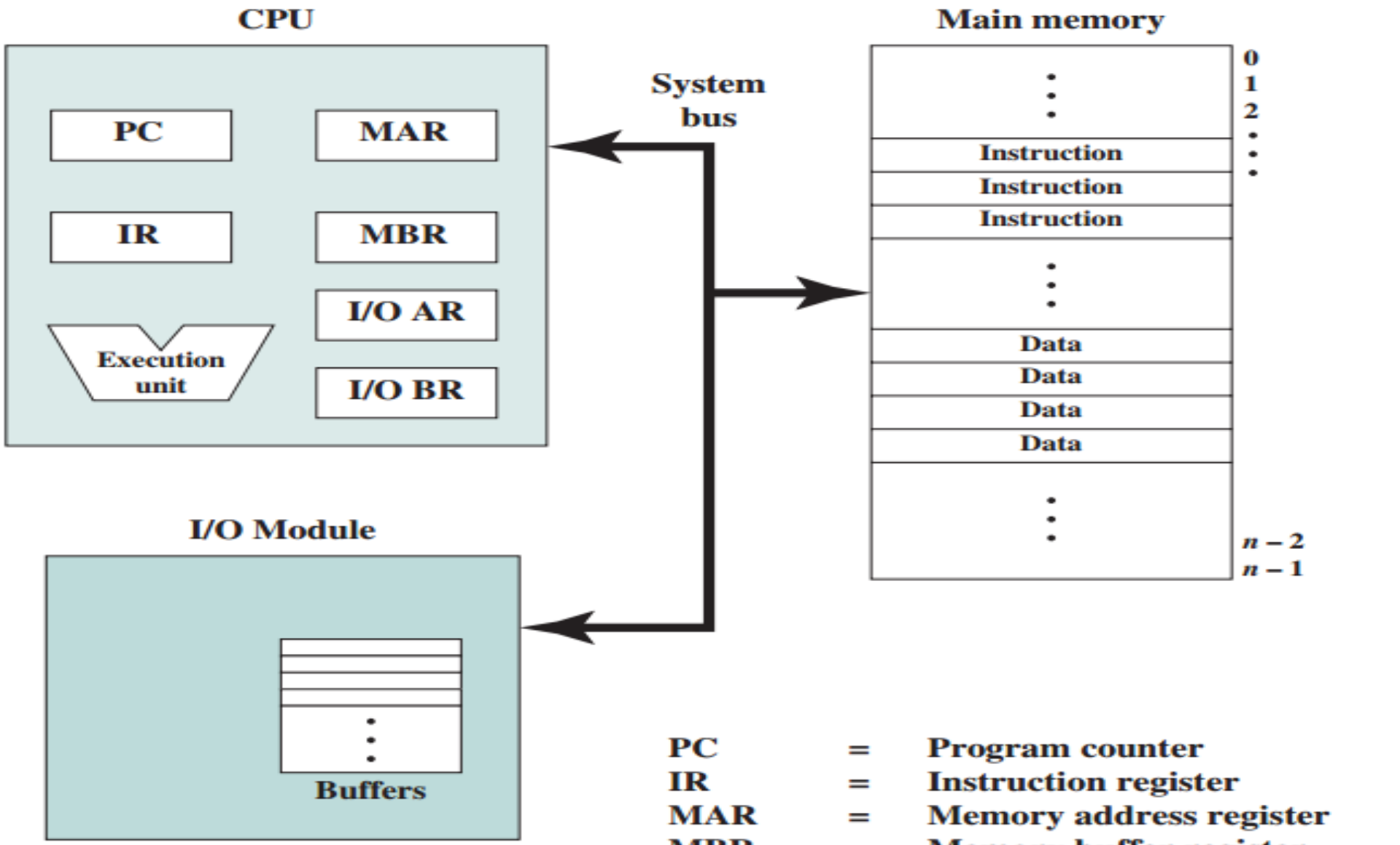
Assis. Prof. Dr. Elmahdy Maree

A Top-Level View of Computer Function and Interconnection

A Top-Level View of Computer Interconnection



Computer Components: Top-Level View



PC = Program counter
IR = Instruction register
MAR = Memory address register
MBR = Memory buffer register
I/O AR = Input/output address register
I/O BR = Input/output buffer register

IAS stands for Princeton Institute for Advanced Studies. (Von Neumann)

Digital Building Blocks

1. Registers
2. BUS System
3. COUNTERS
4. RAMS

COUNTERS

A. SYNCHRONOUS COUNTERS

B. ASYNCHRONOUS (RIPPLE) COUNTERS

SYNCHRONOUS COUNTERS

Design of Sequential Circuit

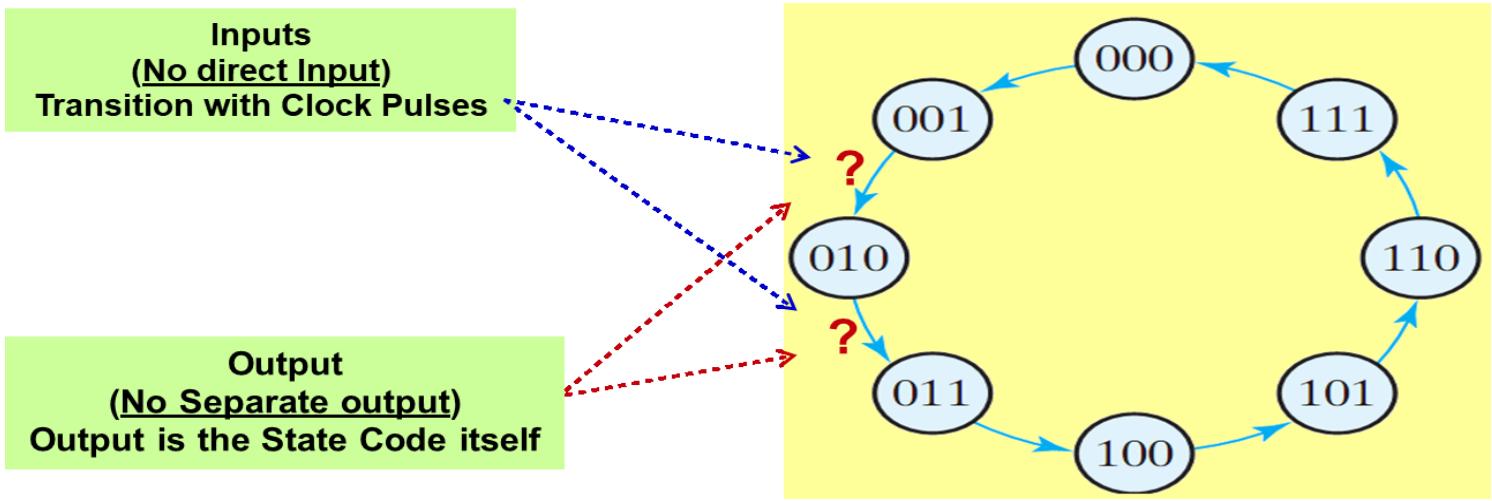
Example 1:

Design a 3 bit Counter (Using "T" FF) which counts in binary form as follows;

000, 001, 010, … 111, 000, 001, …

Solution

2- State diagram:



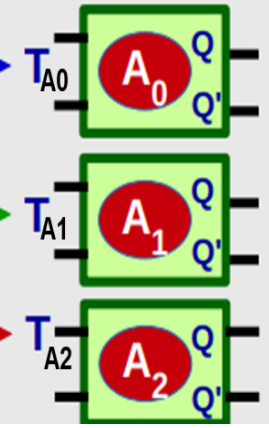
4- State Table:

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2^+	A_1^+	A_0^+	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

INPUTS

Excitation Table of "T" flip flop

T	Q(t+1)	
0	Q(t)	No change
1	Q'(t)	Toggle



5- K-Map for FFs inputs and circuit Outputs

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2^+	A_1^+	A_0^+	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

INPUTS

T_{A0}

A_2 \ A_1A_0	00	01	11	10
0	1	1	1	1
1	1	1	1	1

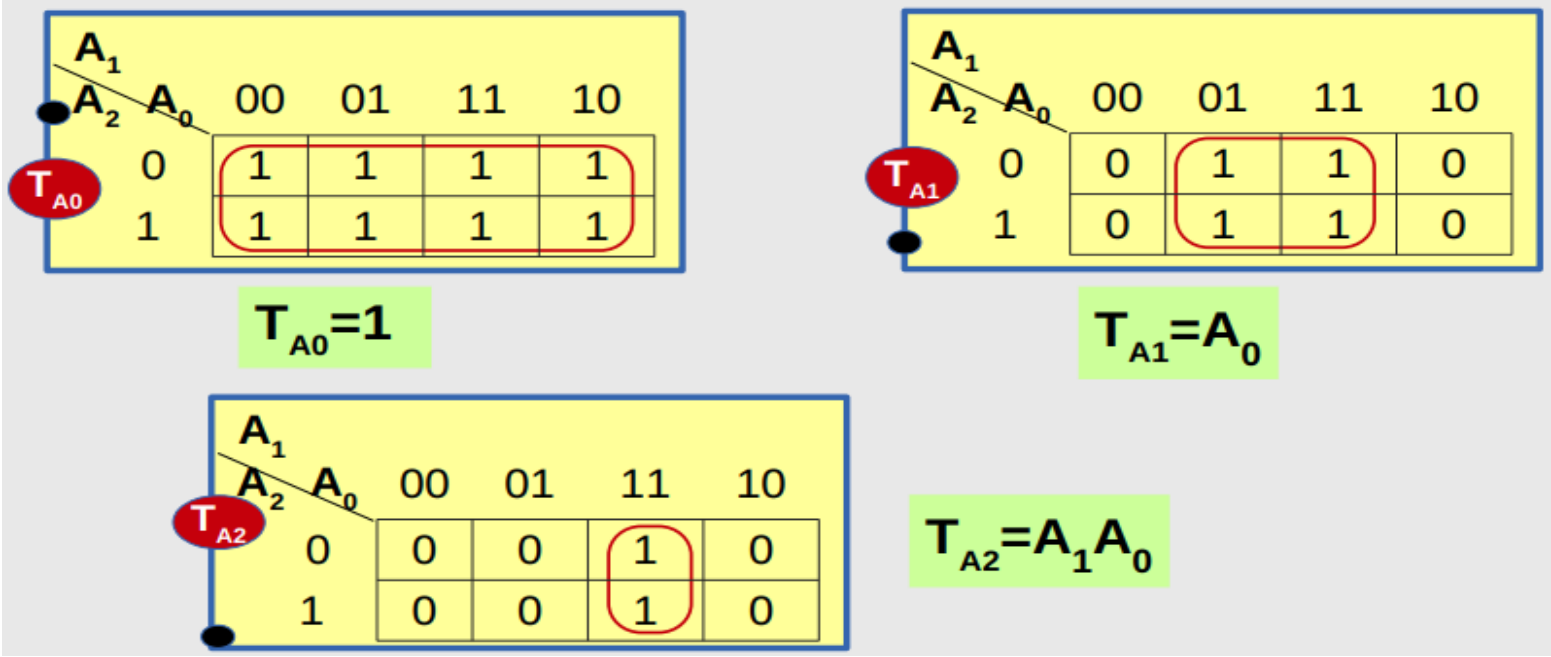
T_{A1}

A_2 \ A_1A_0	00	01	11	10
0	0	1	1	0
1	0	1	1	0

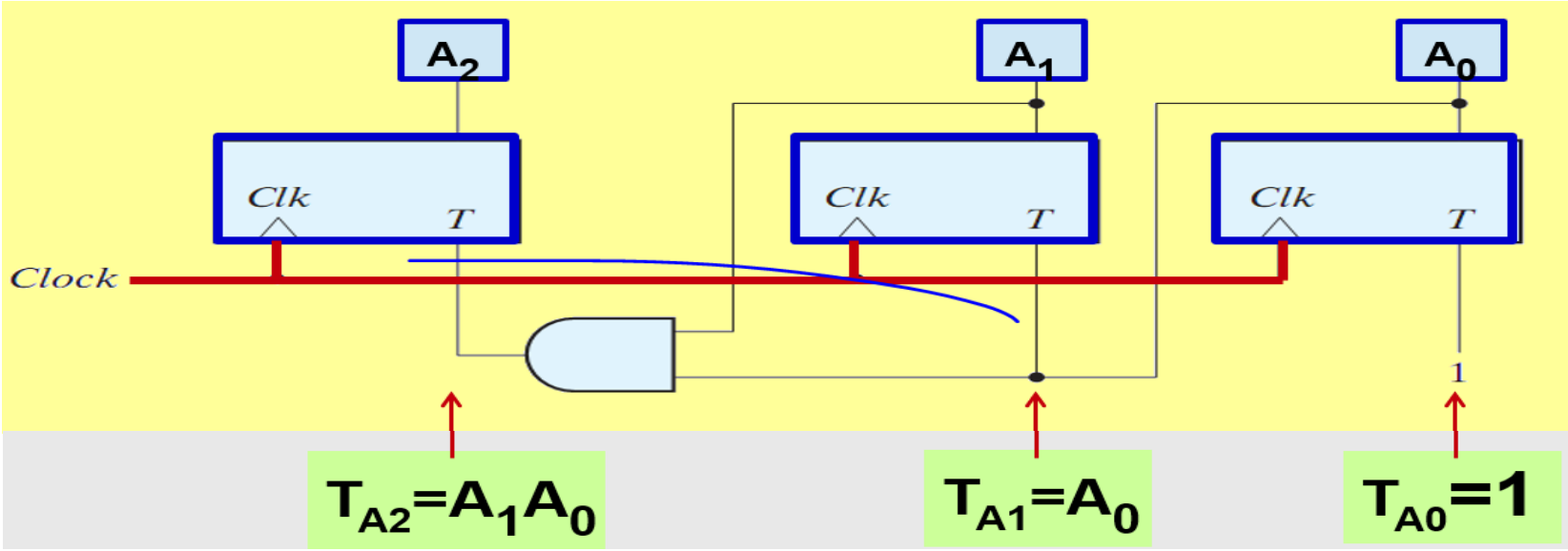
T_{A2}

A_2 \ A_1A_0	00	01	11	10
0	0	0	1	0
1	0	0	1	0

5- K-Map for FFs inputs and circuit Outputs



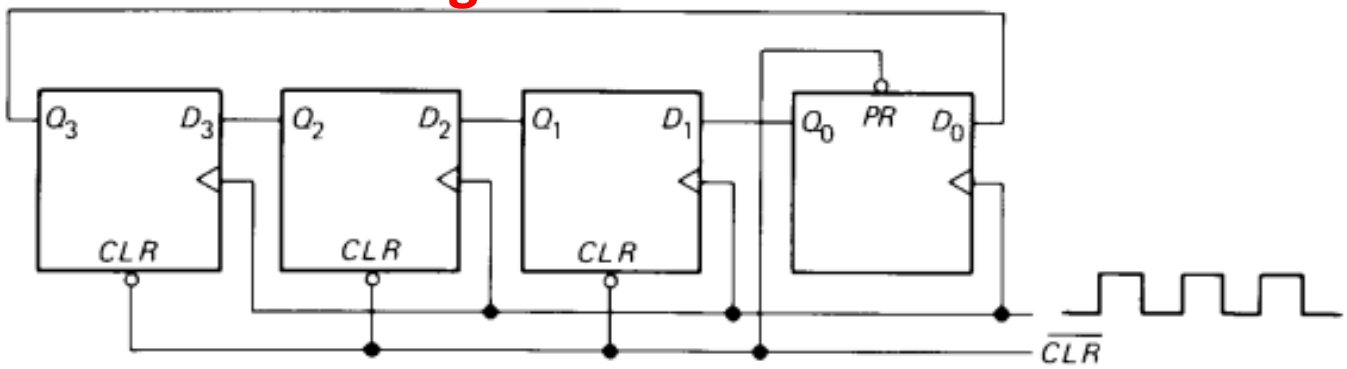
6- Circuit diagram:



Symbol :

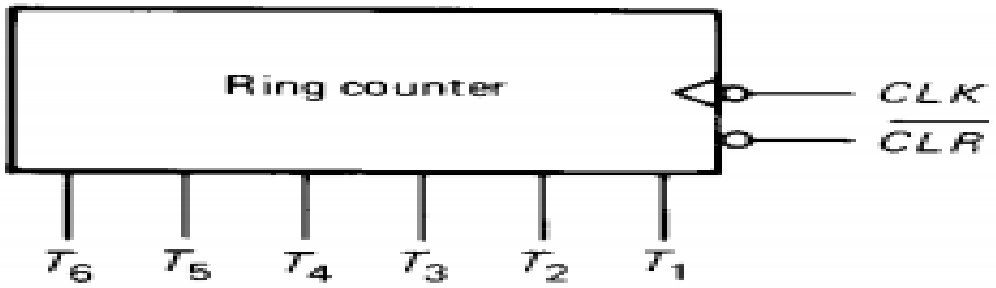
SYNCHRONOUS COUNTERS

Ring Counters



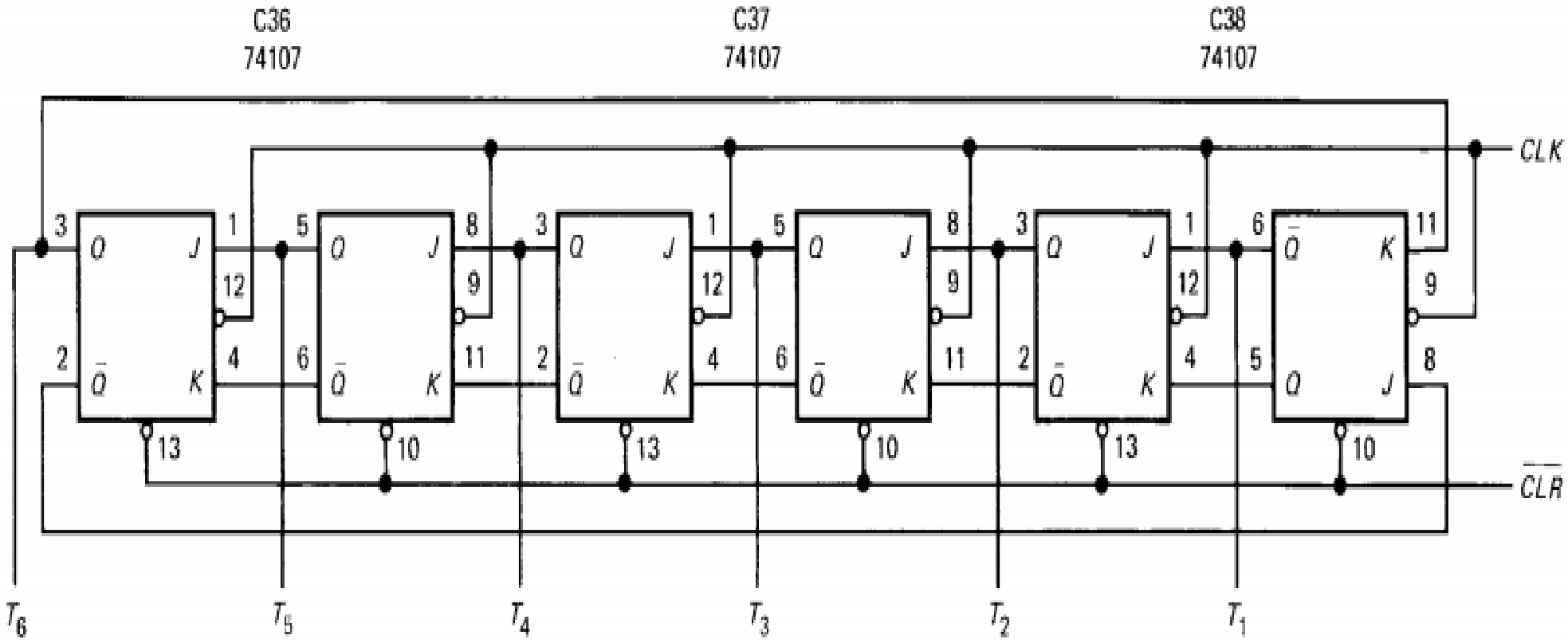
Many digital circuits participate during a computer run to fetch and execute instructions

Symbol :



Controlling a sequence of operations

SAP-1 ring counter Hardware Implementation



Note: Pin 14 is connected to +5 V, and pin 7 is grounded.

ASYNCHRONOUS (RIPPLE) COUNTERS

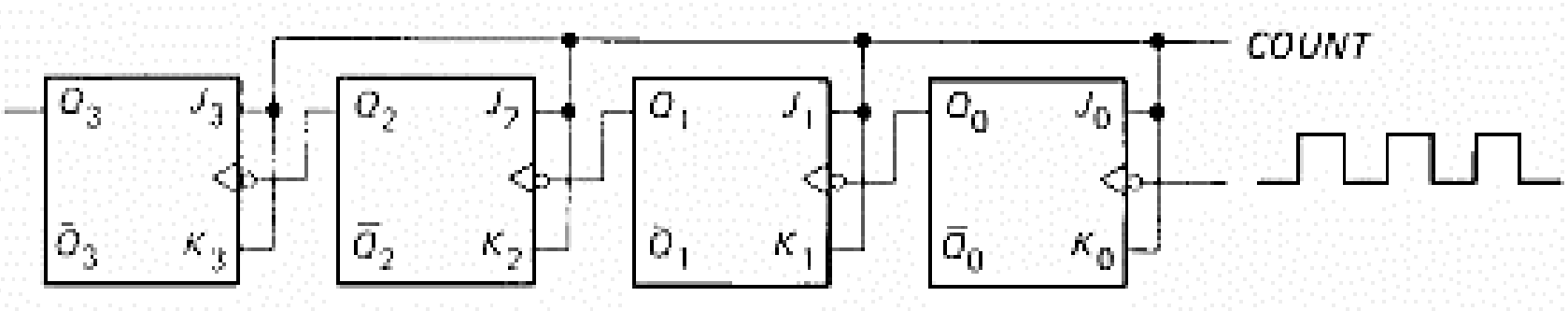
ASYNCHRONOUS (RIPPLE) COUNTERS

-ve edge up counter (Asyn)

Count	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

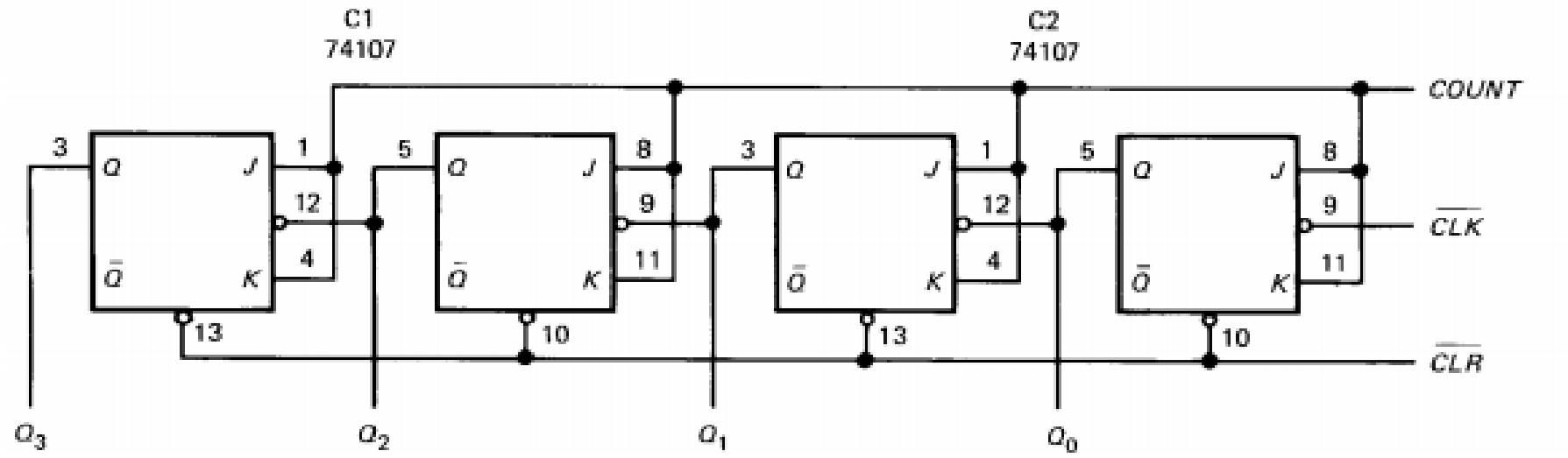
ASYNCHRONOUS (RIPPLE) COUNTERS

Controlled ripple counter(up counter –ve edge)

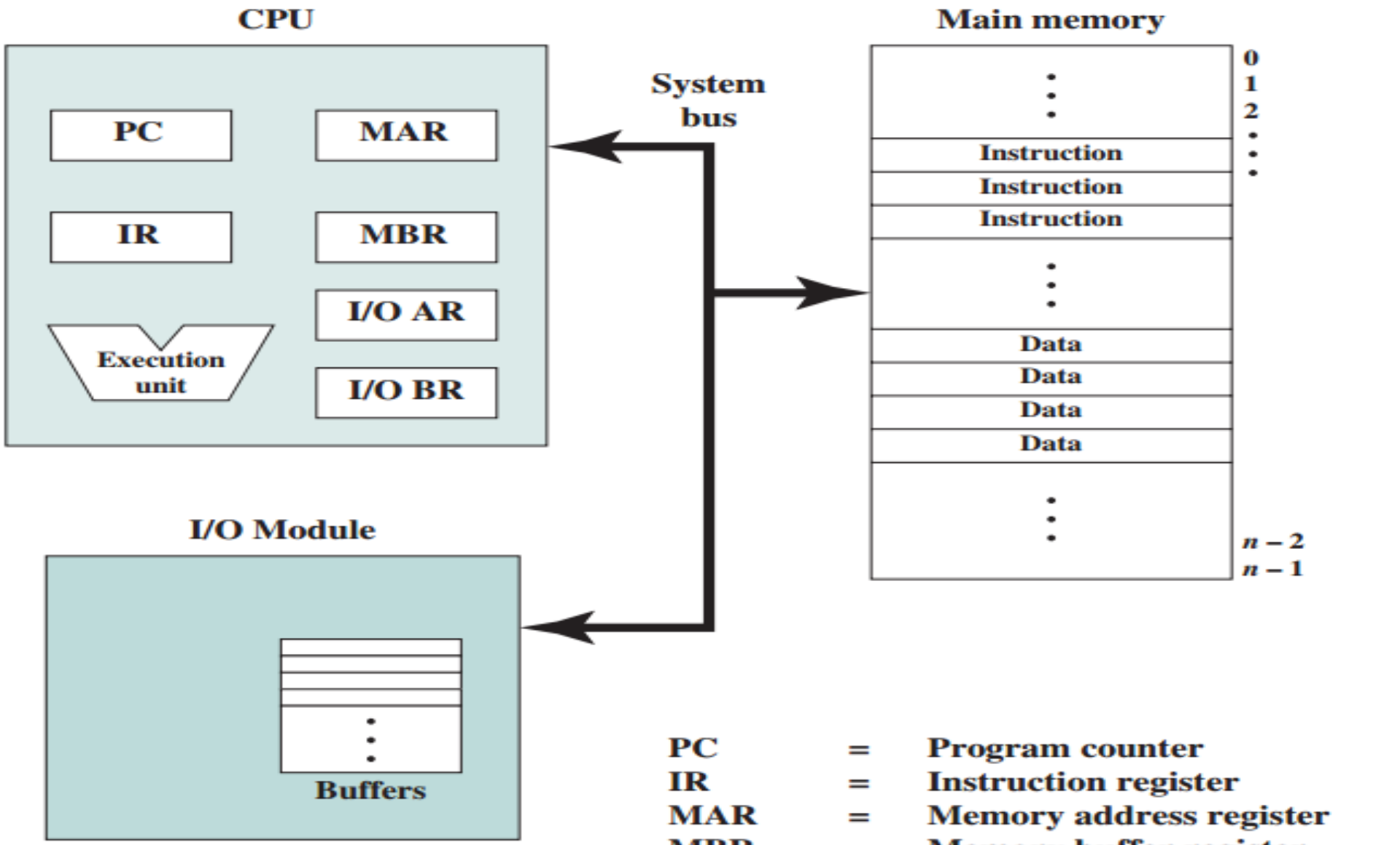


Symbol :

SAP-1 program counter



Computer Components: Top-Level View



PC = Program counter
IR = Instruction register
MAR = Memory address register
MBR = Memory buffer register
I/O AR = Input/output address register
I/O BR = Input/output buffer register

IAS stands for Princeton Institute for Advanced Studies. (Von Neumann)

Memory System

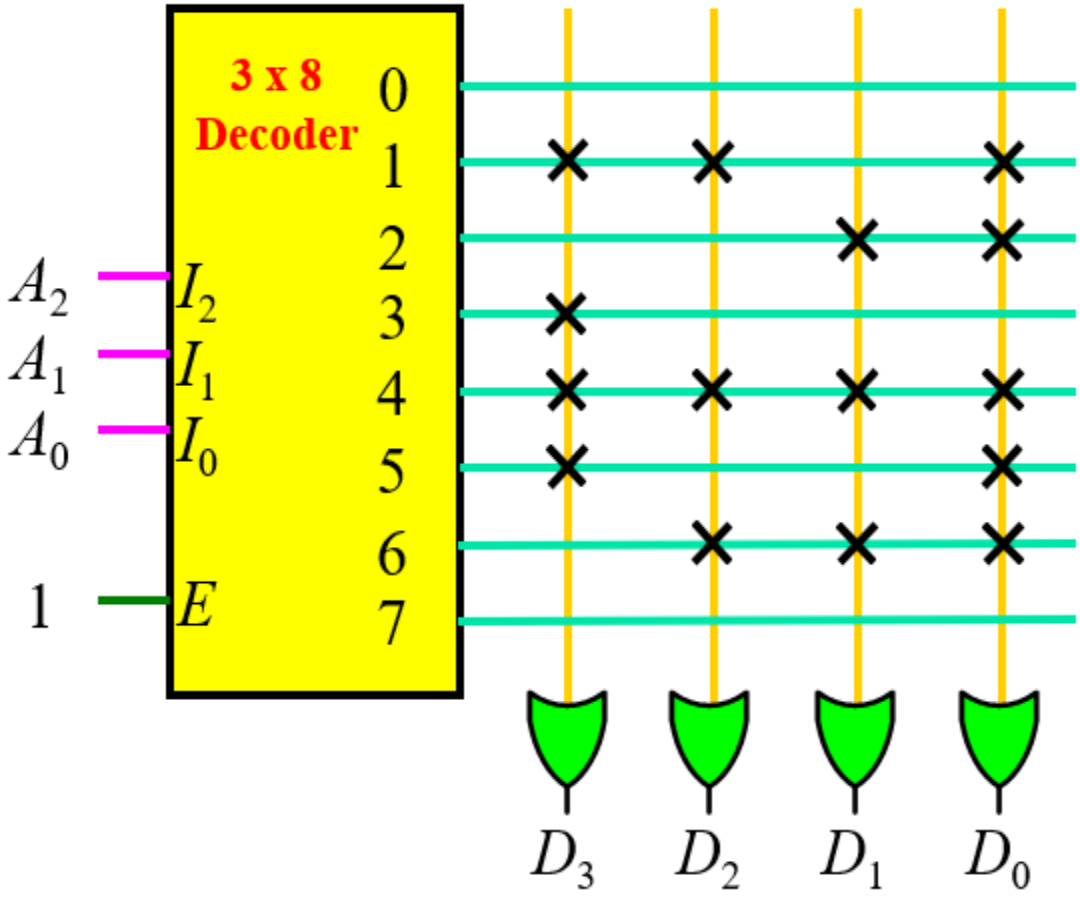
- ROM
- RAM

ROM Design

ROM Design

Design 8 x 4 ROM.

Address	Data
0 0 0	0 0 0 0
0 0 1	1 1 0 1
0 1 0	0 0 1 1
0 1 1	1 0 0 0
1 0 0	1 1 1 1
1 0 1	1 0 0 1
1 1 0	0 1 1 1
1 1 1	0 0 0 0



Types of ROMs

Mask Programmed ROM

Programmed during manufacturing

Programmable Read-Only Memory (PROM)

Blow out fuses to produce '0'

Erasable Programmable ROM (EPROM)

Erase all data by *Ultra Violet* exposure

Electrically Erasable PROM (EEPROM)

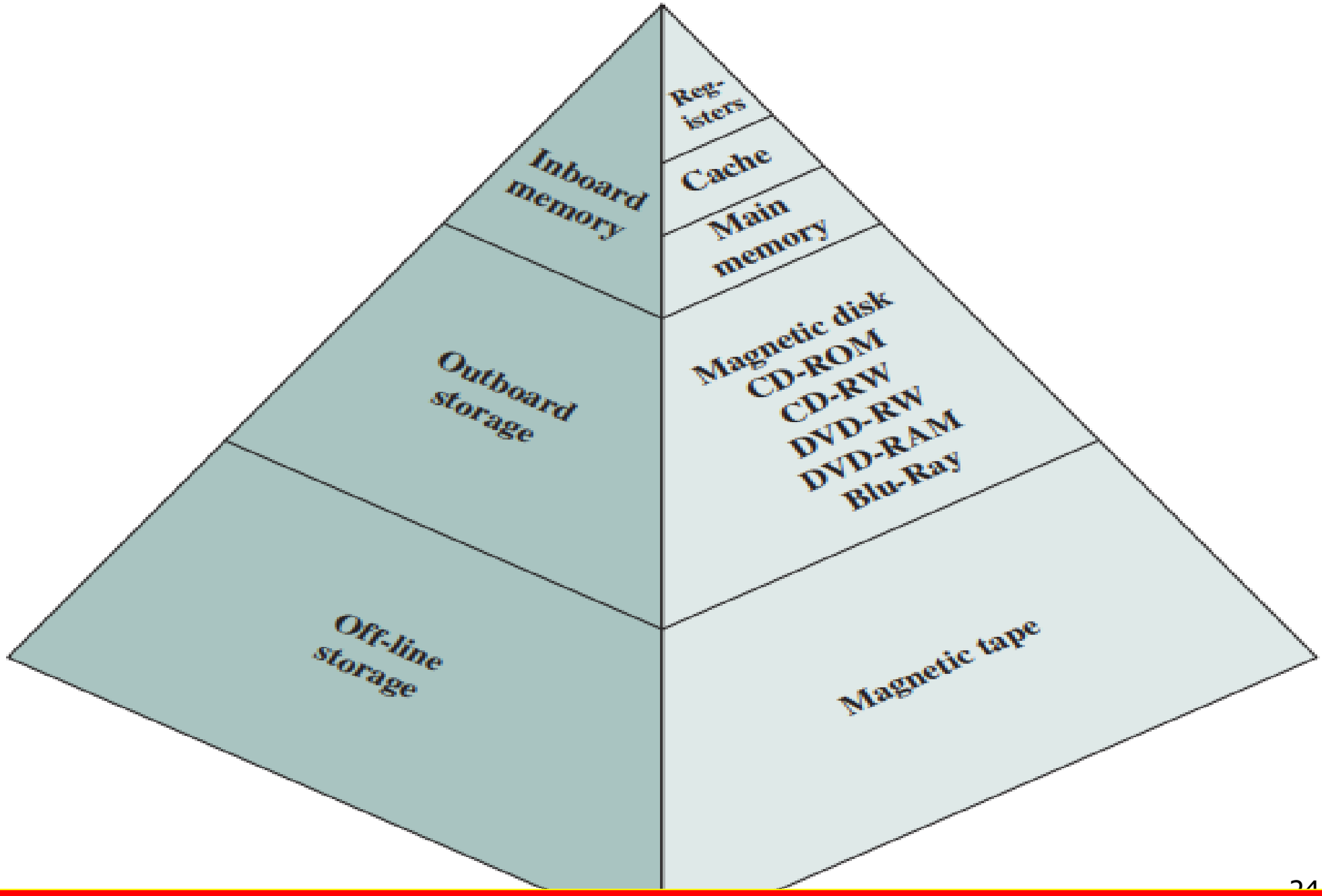
Erase the required data using an electrical signal

CH 5

Memory System

Cache Memory

The Memory Hierarchy



Questions

THANK YOU