question 1

Fetch stage

memory

300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
:	
940	0 0 0 3
941	0 0 0 2

CPU Register

3 0 0	PC
	AC
1 9 4 0	IR

step 1

exute stage

memory

300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
:	
940	0 0 0 3
941	0 0 0 2

CPU Register

3 0 1	PC
0 0 0 3	AC
1 9 4 0	IR

step 2

memory

300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
:	
940	0 0 0 3
941	0 0 0 2

CPU Register

3 0 1	PC
0 0 0 3	AC
5 9 4 1	IR

step 3

memory

300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
:	
940	0 0 0 3
941	0 0 0 2

CPU Register

3 0 2	PC
0 0 0 5	AC
5 9 4 1	IR

3+2=5

step 4

memory

300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
940	0 0 0 3
941	0 0 0 2

CPU Register

3 0 2	PC
0 0 0 5	AC
2 9 4 1	IR

step 5

memory

300	1 9 4 0
301	5 9 4 1
302	2 9 4 1
940	0 0 0 3
941	0 0 0 5

CPU Register

3 0 3	PC
0 0 0 5	AC
2 9 4 1	IR

step 6

question 2

Fetch

memory

300	1550
301	5551
302	2600

CPU

300	PC
	AC
1550	IR

550	0003
551	0004

step 1

execute

memory

300	1550
301	5551
302	2600

CPU

301	PC
0003	AC
1550	IR

550	0003
551	0004

step 2

memory

300	1550
301	5551
302	2600

CPU

302	PC
0003	AC
5551	IR

550	0003
551	0004

step 3

memory

300	1550
301	5551
302	2600

CPU

302	PC
0007	AC
5551	IR

4+3=>7

550	0003
551	0004

step 4

memory

300	1550
301	5551
302	2600

CPU

303	PC
0007	AC
2600	IR

550	0003
551	0004

step 5

memory

300	1550
301	5551
302	2600

550	0003
551	0004
560	0007

step 6

Question 3

memory

300	3005
301	5940
302	7006

CPU

301	PC
0005	AC
5940	IR

940 : 0002

memory

3005
5940
7006

CPU

302	PC
	AC
7006	IR

940 : 0002