

Write 2 on Pit 16 on ODR register by use structure and Rinter for AU registers in GPIO PrePheral: * Pragma Pack () struct SGPIO volatle cintact MODER; volatile vintart oDR; Volable vintset ASCR; Base - Address volatile vintsex IDP; * define GBioA ((struct SGPio *) 0x 4800 0000) void main () 3 GBioA->ODR=(1ul << 16); 11 GBIOA-INIT (GBIOA); 11 GBioB-init (GBIOB); Mcu Bus interface: · "init" Je master port II apartil * anoster interface .: BH. * @ slave interface :: الد استطاع انه يعت من لفسه . No. (add, Data, size) > init transactions # slave restand to master. 1 master issue transaction to slave. MI MI. An Dra: Direct memory access Controller. EL Ly have 2 Register " SAT" & " DAT " have master +slave.

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system bus can handle time Policy and Arbitration if there are 2 master Port from 2 CPu issue transaction read or write at the Address simultaneously.

Junderstanding Amba Bus Architecture and Proto 61:

-> two main characteristics of bus interface Performance are bandwidth and latency.

> traditional Amba:

* AHB. " Advanced High Performance "

* ASB. " II system

* APB. " " Peri Pheral Bus

= Axi Channel: "issue "
write"

ceissue ~ Gread or

O write Address Channel

@ write data channel

@ write response channel

o read address channel

@ read data channel

Note: every channel is a signal.

Note: every signal is a group of wires.

[info]

* Byte: 8 bits

* Halfword: - 16 bits - 2 Byte

* word: - 32 bits - 4 Byte

= * Double-word: - 64 bits - 8 Byte.

= * nibbles: 4 bits - 1/2 Byte.

Big indian & Little indian:





