what is the embedded system ?!

① embededd system is a special purpose computer system designed to perform one or few function.

② embedd system has constraints : " power - size - time "
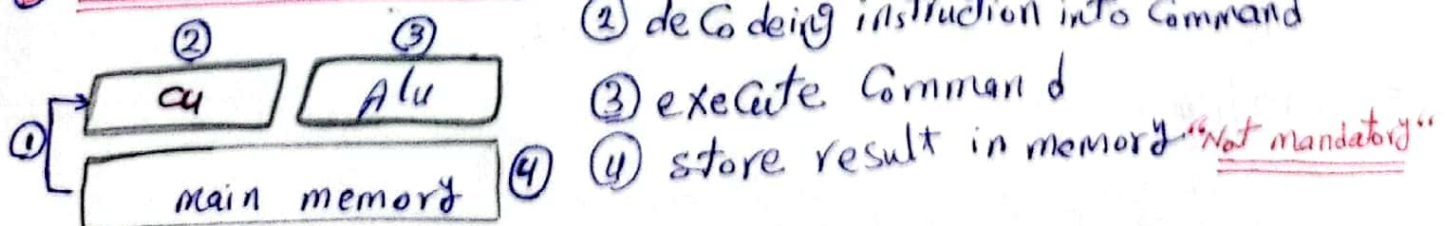
difference between IC, mPu, mCu, SoC, ECu :-

① **IC** :- the integrated circuit is a single chip which has a set of electronic circuit . " timer 555 "

② **VLSI** :- very large scale integrated circuits

③ **moor's law** :- the density كثافة of transistors in an IC will double every years .

[Note] microprocessors, micro-controller- system on chips every processing devices is made of us are made of IC's .

④ **micro processor** : is an integrated circuit which can perform Arithmatic and logic operations .
   it only consists of cpu .
   used for general computing like our personal computers, servers , etc .

⑤ **Central Processor unit "cpu"** :- contain Alu - Cu - Registers

⑥ **instruction life cycle** :- ① fetch instruction from memory.
   ② decodeing instruction into command
   ③ execute command
   ④ store result in memory "Not mandatory"

```
      ②              ③
   ┌─────────┐   ┌─────────┐
 →│   Cu    │   │  Alu    │
 │ └─────────┘   └─────────┘
 │ ┌───────────────────────┐
 └─│    main memory        │ ④
   └───────────────────────┘
 ①
```

⑦ **micro Controllers:-** mcu = micro Controller unit.
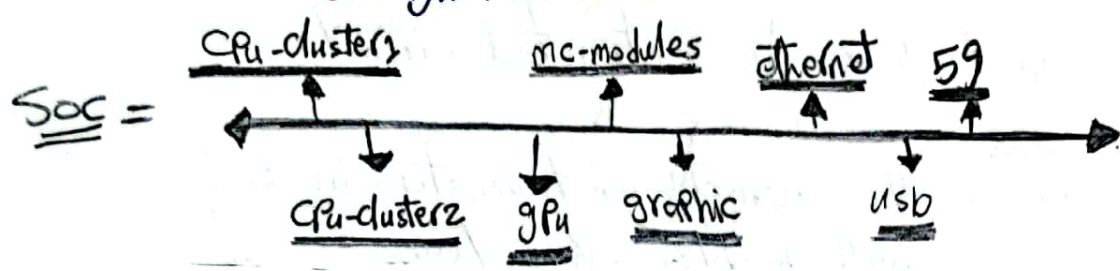
  ↳ is also an IC which Consists of:
     CPu and other Components like Ram, Rom, I/o Ports.

⑧ **System on chip(soc)** :- it is a high Performance micro Controller

  * two main families of embedded system Platform:-
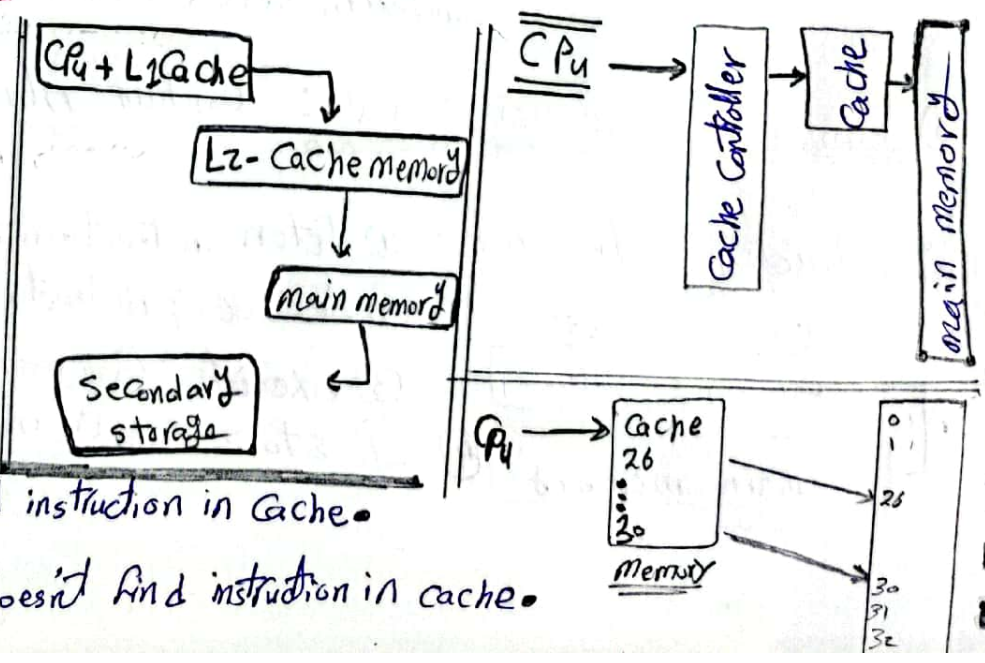   ① micro Controller family.
     ② High Performance " soc "

$Soc =$

CPu -clusters   mc-modules   ethernet   59

CPu-cluster2   gPu   graphic   usb

⑨ **F PGA** :-

⑩ **electrical Control unit** :- " ECu " = soc + sensor + Actuater.

           N number of soc + sensor + Actuators.

⑪ **Cache memory** :-

  CPu   fast
  Register   ①

  Cache memory ②

  main memory ③

  secondary memory ④
                  slow

  CPu + L1 Cache

  L2- Cache memory

  main memory

  Secondary storage

  CPu → Cache Controller → Cache → main memory
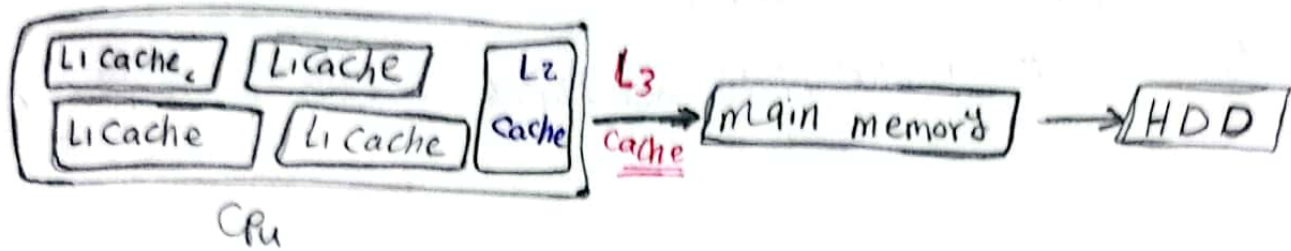
  CPu → Cache 26 ... 30   Memory   0 1 ... 26 30 31 32

* cache hit :- CPu find instruction in Cache.

* Cache miss :- CPu doesn't find instruction in cache.

Type of memory cache :-

L1 cache | L1 cache | L2 cache | L3 cache → main memory → HDD
L1 cache | L1 cache |

CPu

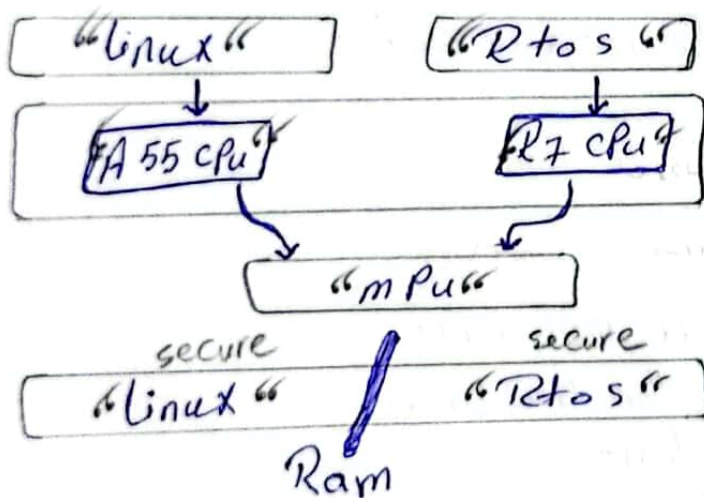☒ **Cach Coherence** :- is the mechanism that ensure that changes in the values of shared oPerands (data).

☒ **Floating - Point unit "FPu"** :- is on Ic that Carry out addition substraction, multiplication, on floating Point value.

---

* **memory Protection and mangement unit [mPu - mmu]** :-

"Linux" → "A 55 cPu"

"Rtos" → "R7 cPu"

"mPu"

secure "Linux"   secure "Rtos"

Ram

☒ **mPu** :- allow software to define regions in the memory and assign access Permissions to those region.

☒ **mmu** :- translate the virtual address in the Programs to Physical address in main memory.

data
CPu ←——→ memory
virtual Address → mmu → Physical Address

* memory Type :-

① Basic memory element " D Flip Flop "
② Register is a group of Flip Flop, each Flip Flop is caple of storing one bits.
③

memory

Ram	Hybrid	Rom
* Dram	* NvRam	* EProm
* Sram	* Flash	* Prom
	*EEProm	* masked rom

Ram "Random access memory ":-

① Data at any time memory Can be read or write.
② volatile memory.
③ faster than Rom. " Based on mosfet transistor ".

Ⓐ S-Ram : static Random access memory :-
　① No refresh time to keep their data.
　② s ram performance is better than Dram.
　③ medium Power Consumption.

Ⓑ disadvantage of sram :-

　① expensive.
　② Complex design.
　③ each Cell require at least 6 transistors.
　④ when the Power is lost, Data will be lost.

Ⓑ D-ram : Dynamic Random access memory :-
　① refresh time each slot.
　② slower than s-ram.
　③ use Capcitor to store data.

"S-Ram"	"D-Ram"
* speed is faster.	* speed is slower Than S-Ram.
* small size.	* large size.
* cach memory.	* Cheap Cost.
* Complex and use Transistors.	* used in main memory.
* 6 Transistor.	* simple and use Capacitors.
* low Power Consumption.	* only one transistor.
* expensive Cost.	* High Power Consumption.

※ Rom :: Read only memory :-

Ⓐ Prom :- ① Can be Programmed only once
② The kind of Rom that the user Can burn information
③ burn only once, So it is Called OTP.

Ⓑ mask Rom :- ① Not user Programmable Rom.
② only Programmed by IC-manufactuer.
③ cheaper than other kinds of Rom.

→ difference between Prom and masked rom :-
① Prom is manufactured as a blank memory
② mask rom is Programmed during the manufactured Process

Ⓒ EProm :- ① it Can be Programmed many time.
② EProm need UV light to erase the data.
③ is Non volatile.

Hybrid memory :-

→ Combination of ram as well as Rom
→ Like ram : the Content to hybrid memory Can be read and written.
→ like rom : the Contents of hybrid memory are Non volatile.

(A) EEProm :- electrical erasable Programmable Rom

① Can be Connected serial through I_2C, SPI.

② Non volatile

(B) Flash :

① Flash is the most recent advancement in memory
② low Cost - High denisty - Non Volatile - fast
③ Flash is Popular than EEProm.

(C) Non-Volatile Ram "Nv Ram" :- it's sram with battery backup
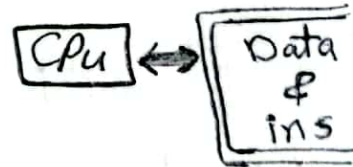So that the Content are not erased

S.Ram | Backup battery.

"Von neumann & Harvard"

A bus is a set of Parallel Conductors that transfer data
between different Components of a Computers.

a bus has three main Part :

→ Data bus.
→ Address bus.
→ Control bus.

CPu ⟷ Data & ins

Von-neumann Architectures :- the same memory & bus are used
to store Data and instructions.

→ CPu is unable to access Program memory and data simultaneously
→ the bus is not used by another operation. "wait state"

Harvard Architectures :- The harvard Architectures store machine instructions and data "sperates memory - different bus"

main advantage :- able to run Program and access data independently, therefore simultaneously.

$CPU \xleftrightarrow{bus} Data$

$\downarrow bus$

ins
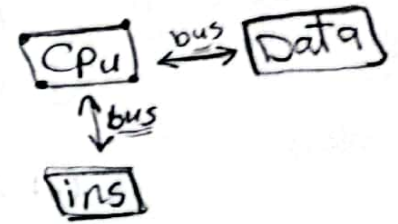
modified Harvard Architectures:-

no Physical seperate between the memory space used by both data and instruction

* Two sperate address space, different bus.

$CPU \rightleftarrows \begin{cases} Data \\ instruction \end{cases}$
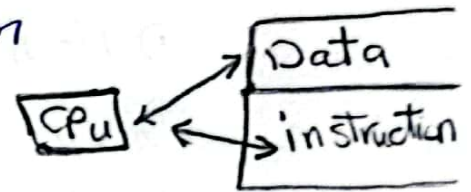
why von neumann is used in Computers and harvard is used in mcu?

- signal length
- the natural of architectures.
- Pc use von neumann beCause expected the boot code
- micro Controller has it's own Program into flash memory so lead to Harvard architectures.

Pipeline :-

Cisc	Risc
* used in laptoP and desktop	* Used in smart Phones and tables
* Has more Complex hardware.	* Has simpler hardware
* multiple machine cycle.	* single machine cycle Per instruction
*greater energy Consumption	* lower energy requirements
* more intensive task will do	*
* better with Cisc	* Run at bwer clock speed
*	* but Can Perform simpler task more
* Can't SuPPort Pipeline	* Quickly than Cisc
	* Can supPort Pipeling.

micro Processor :- It's an IC, General Purpose Processor with no Ram and Rom, Io Ports.

micro Controller:- It's an IC, single specific Purpose Contain CPu, fixed amount of Ram and Rom used to Controll emdedd systems.

Embedded system :- system "electrical or electromechanical devices"

n-bit Processor :-
① Processor work only on n-bit of data at atime
② Data large than n-bit has to be broken into n-bit Pieces to be Processed.

" micro-Processor "	" micro-Controller "
- general Purpose	- specific Purpose
- Contain no Ram no Rom no I/o Ports	- Contain fixed Ram - Rom - I/o Ports
- expensive because Ram add andsoon	- The designer Can't add any external devices
- Flixable to versatile enabling the designer decide amount of Ram	- Ideal for application

Von - neuman	Harvard Architecture
1- single Common memory space where Program instructions and data are store	- seperate memory area for ins. and Data
2- there are single data bus fetch both of instructions and Data	- different bus to access data and instructions.

Why Rom is Read only memory although i can write on it ?!

- Cpu doesn't have the capability to write to it.
- it may be written to by an external devices to access writing on it.

Type	volatile	writeable	erase size	max-size	Cost	speed
S-Ram	Yes	Yes	Byte	unlimited	expensive	Fast
D-Ram	Yes	Yes	Byte	unlimited	moderate	moderate
masked Rom	No	No	N/A	N/A	inexpensive	Fast
P-rom	No	once	N/A	N/A	moderate	Fast
EP-Rom	No	yes many by devices	Entire " Chip "	limited	moderate	Fast
EEProm	No	Yes	Byte	limited	expensive	Fast to read
Flash	No	Yes	sector.	limited	moderate	Fast to read
Nv-Ram.	No	Yes	Byte	unlimited	expensive	Fast

المسوحة ضوئيا بـ CamScanner