Embedded Systems Advanced Nano Degree

Automotive door control system design

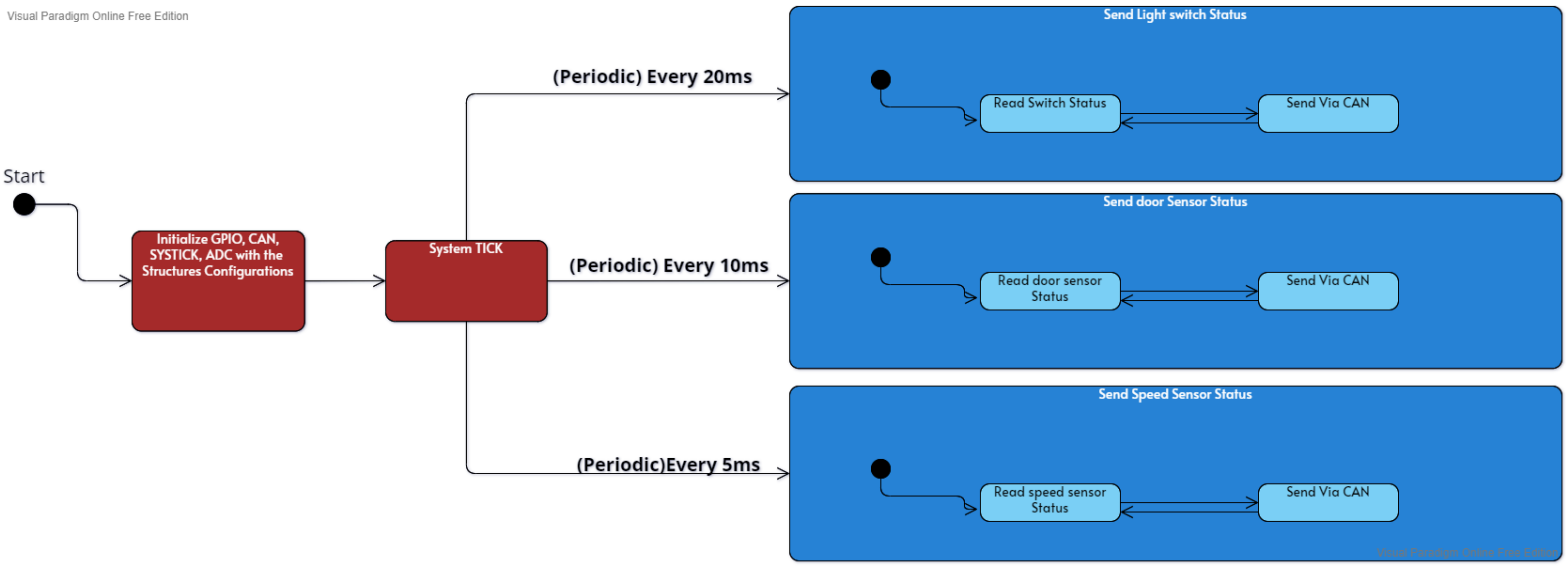
Dynamic Design Analysis

Youssef Hussien Mahmoud

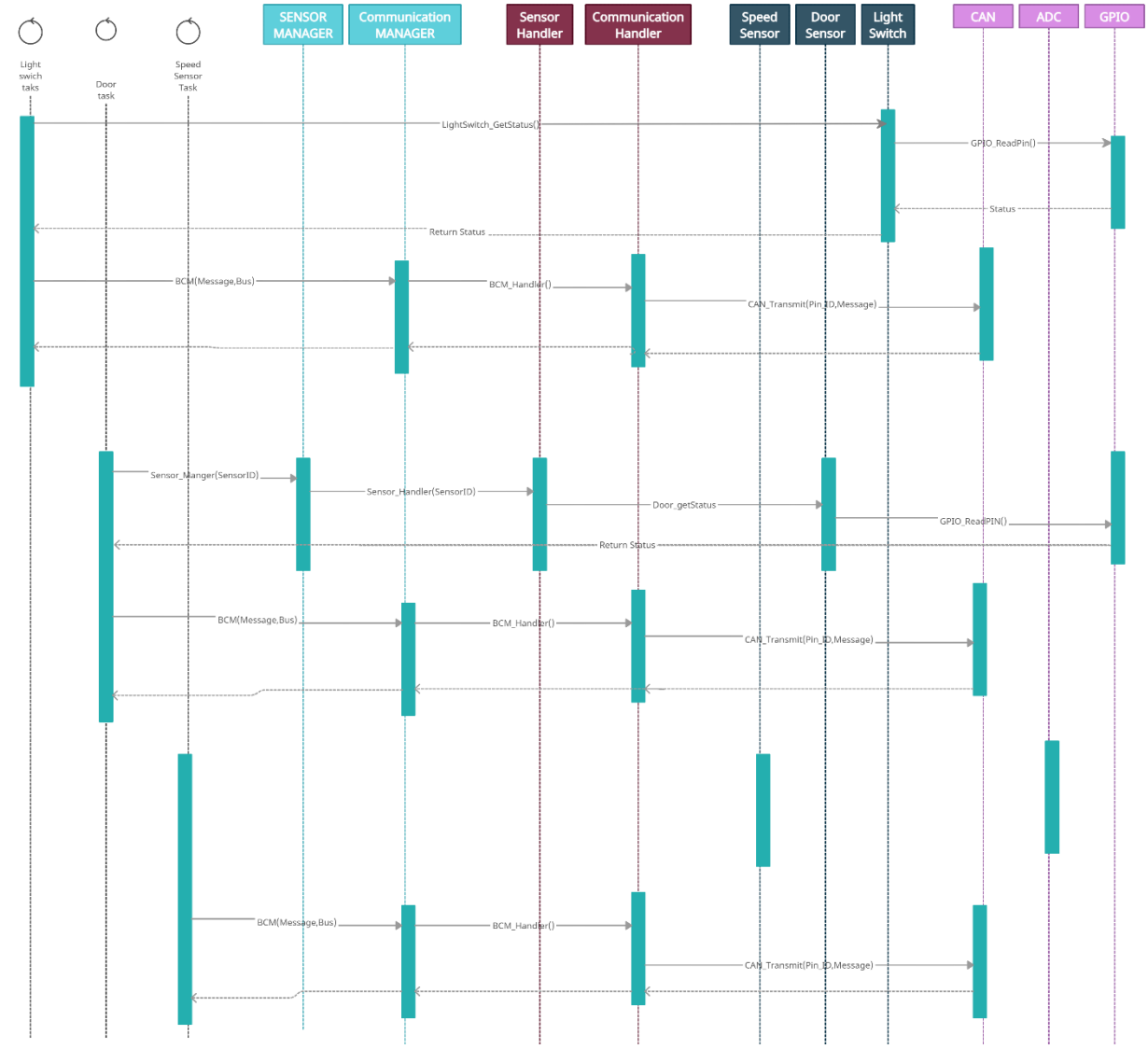
ysfhussien@gmail.com

ECU_1

1- State Machine Diagram



2- Sequence Diagram



3- CPU Load

The system contains three tasks assuming worst case scenario that the execution time of task is 1ms.

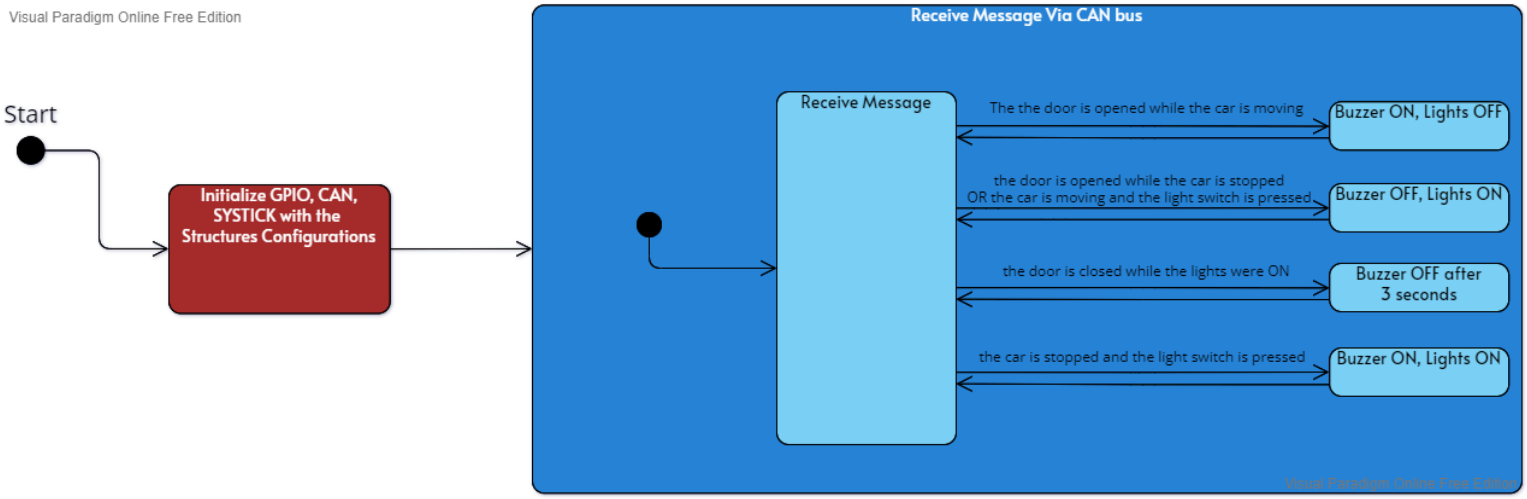
T1 {P:20, E:1} T1 {P:10, E:1} T1 {P:5, E:1}

Hyper period = 20

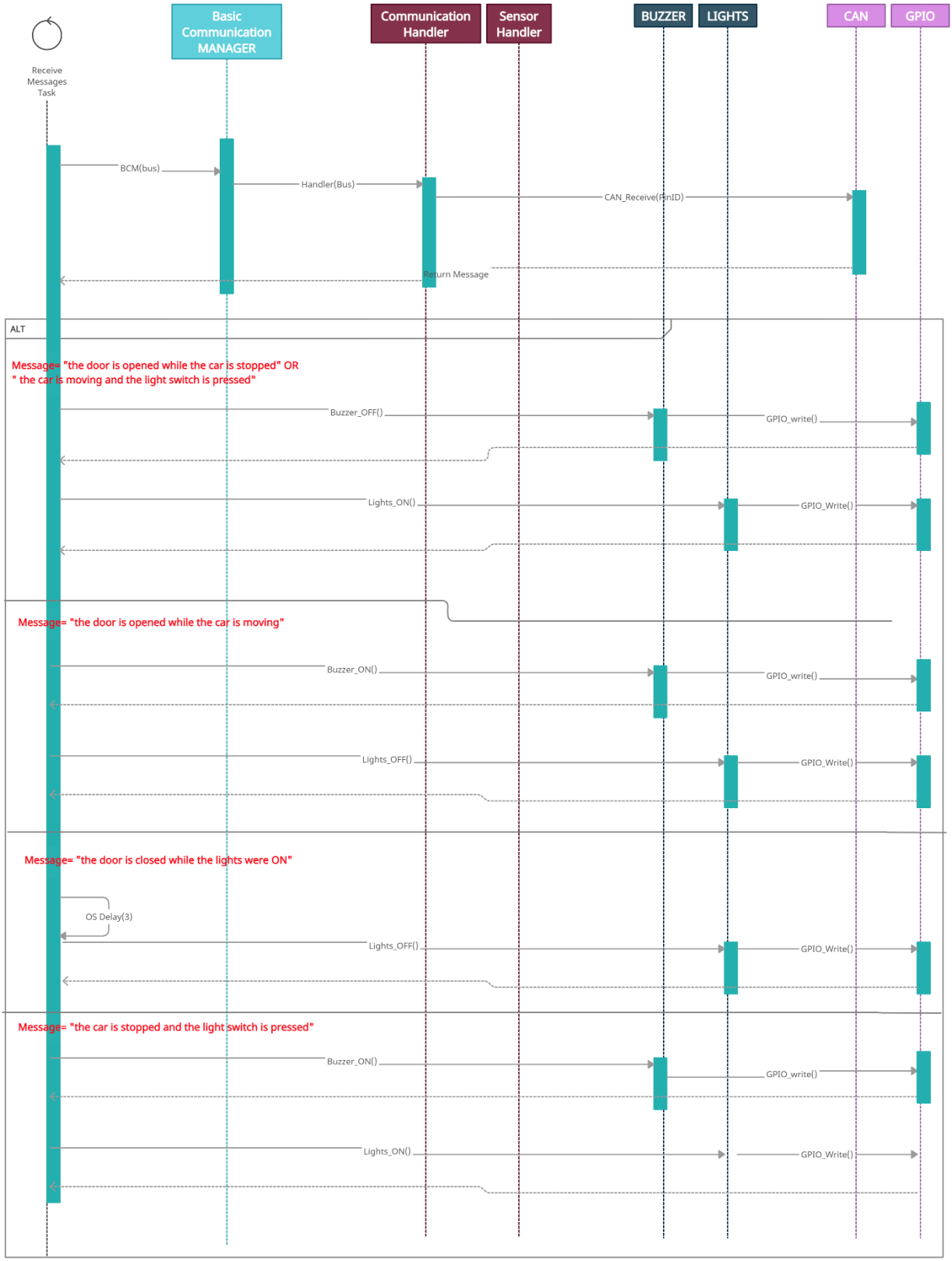
U = (E1 + E2 + E3) / H = ((1*1) + (1*2) + (1*4) / 20) * 100 % = 35%

ECU_2

1- State Machine Diagram



2- Sequence Diagram



3- CPU Load

The system contains only one task assuming execution time 2.5ms And periodicity is 5ms.
T1 {P:5, E:2.5}
Hyper period = 5
U = E1 / H = ((1*2.5) / 5) * 100 % = 50%

BUS LOAD

Assuming CAN frame consists of **125 bit** and using **500 kBit/s**

Bit time = 1 / bit rate = 1 / (500 * 1000) s **= 2 us**

Frame time = number of bits * bit time = 125 bit * 2 us = **250 us**

the bus load for 3 messages every 5, 10 and 20 ms can be calculated by
- 1 frame every 5 ms = 200 frame every 1000 ms
- 1 frame every 10 ms = 100 frame every 1000 ms
- 1 frame every 20 ms = 50 frame every 1000 ms

Total frames in 1 s = **350**
Total time on bus = 350 * 250 us = 87500 us
Bus load in 1 s = (87500 * 1000 ms / (1000)) * 100 % = **8.75 %**