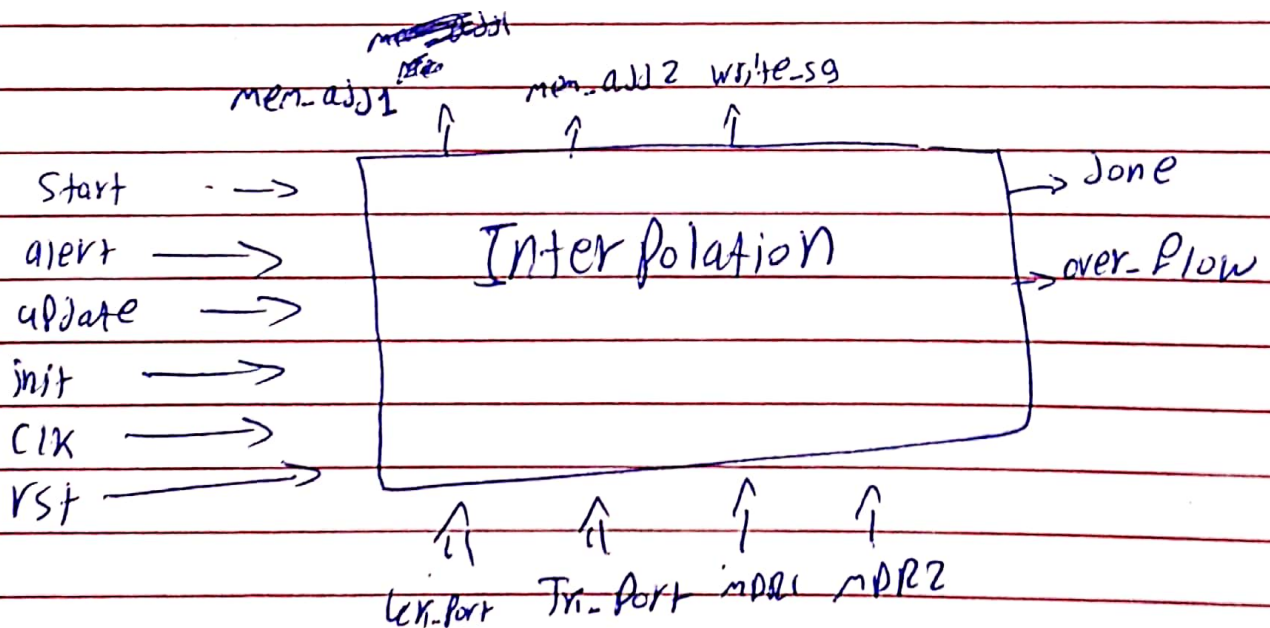
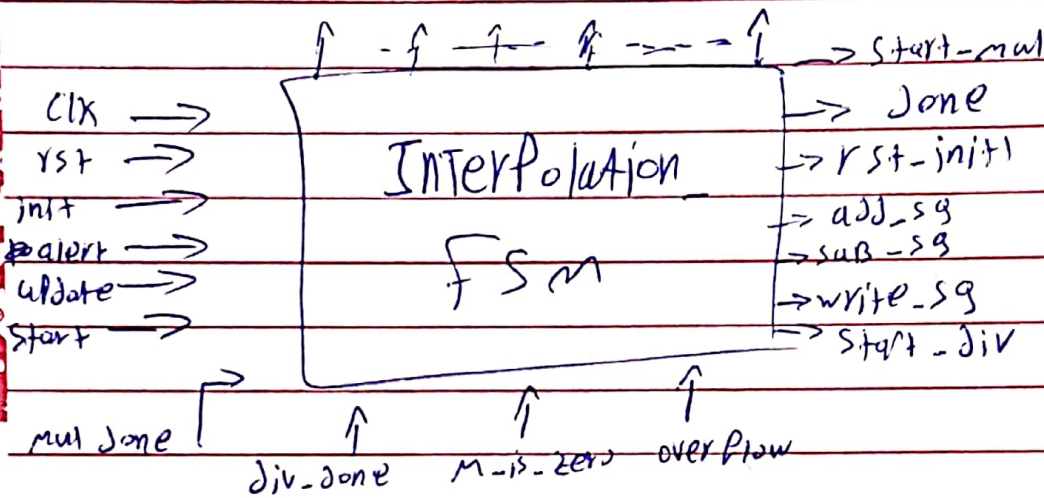


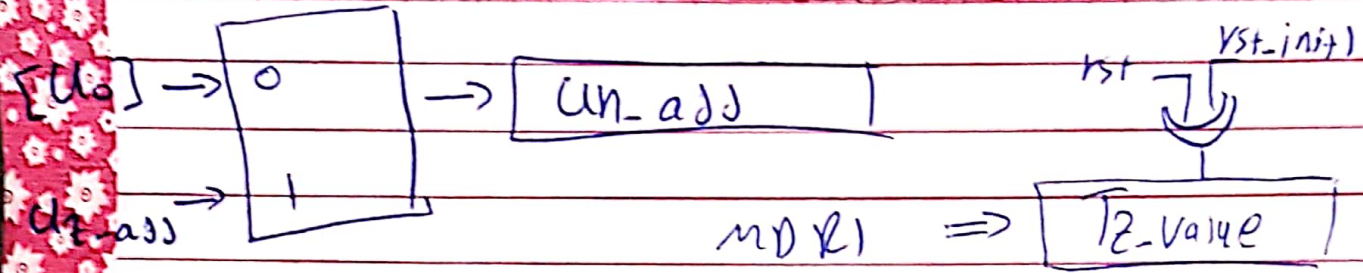
all registers enables and all mux selectors



note mdr2 is actually in/out

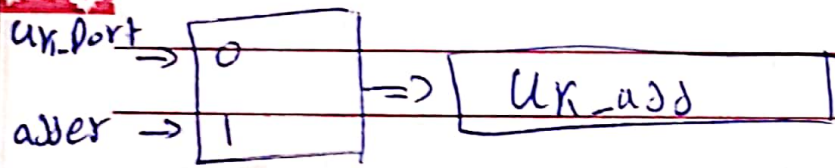
if write = 1 then

Temp2 \Rightarrow mdr2



adder $\rightarrow U_{z_add}$

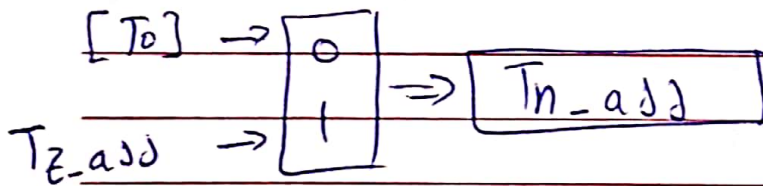
adder $\Rightarrow Temp1$



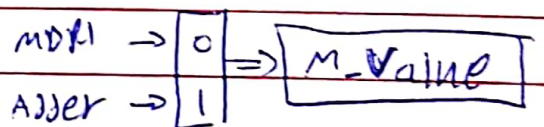
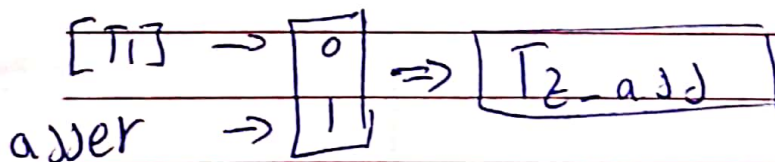
adder $\Rightarrow Temp2$

MDR2 $\rightarrow U_{n_value}$

div-result $\Rightarrow K$



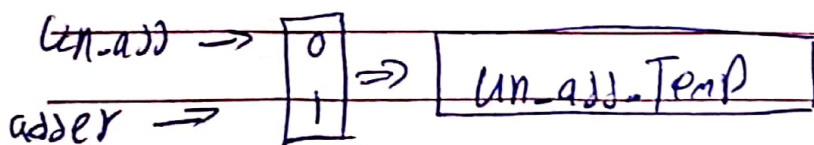
$[M] \Rightarrow M_Add$

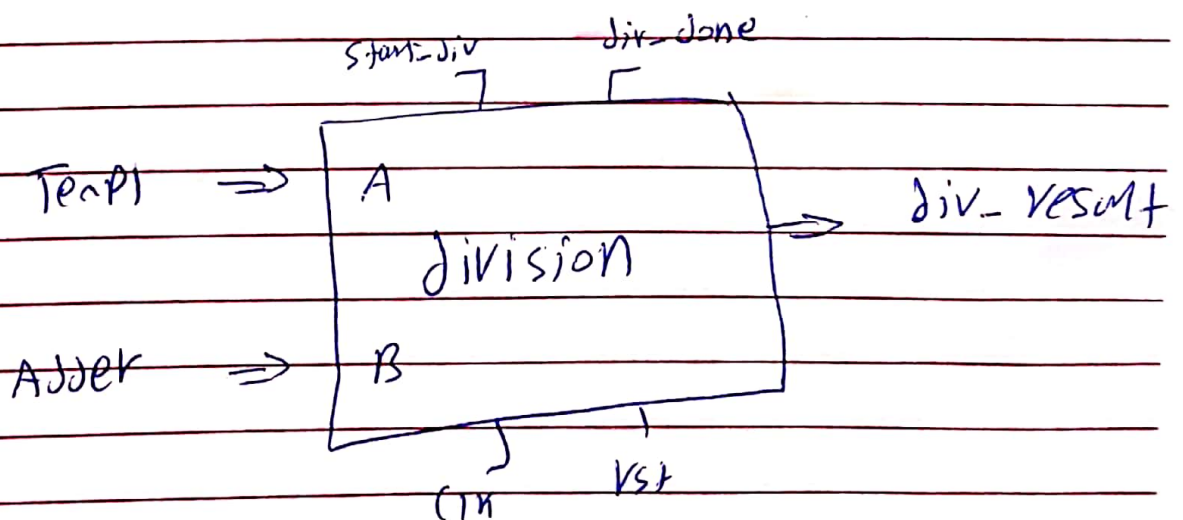
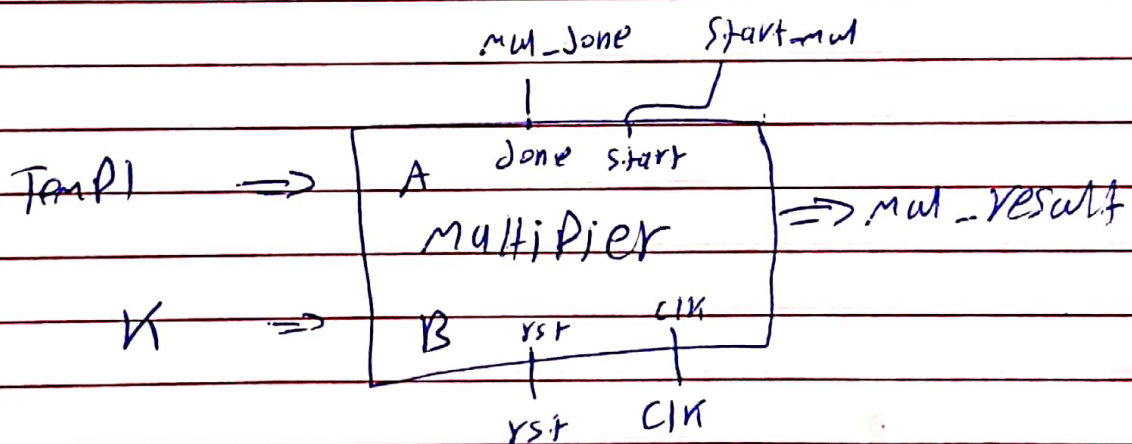
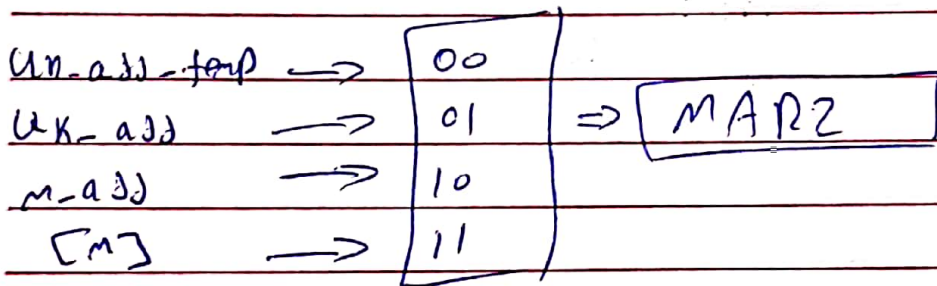
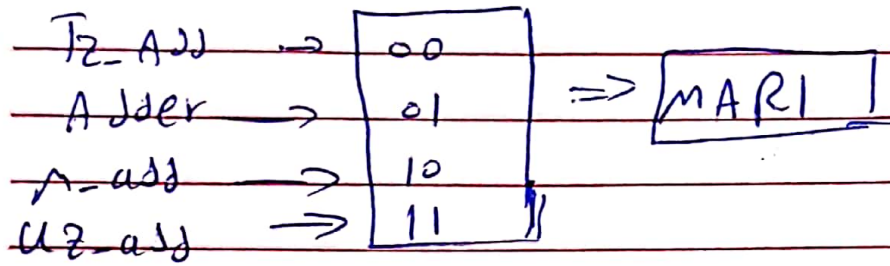


$Tz_value \Rightarrow Tn_value$

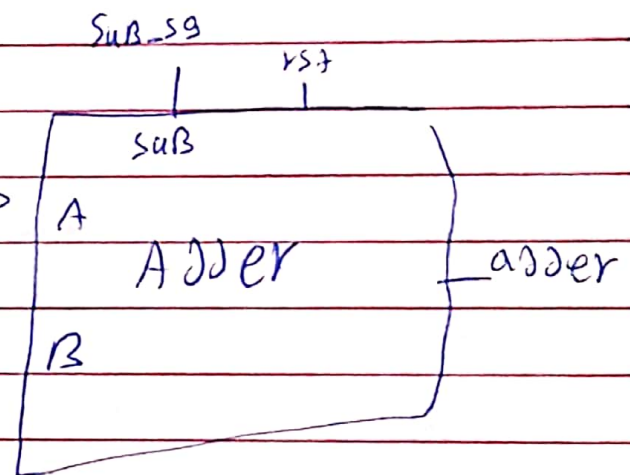
$rst \rightarrow rst_init$

$T_{n_port} \Rightarrow T_{n_value}$





Un-add →	0000
TZ-add →	0001
U2-Add →	0010
Tn →	0011
TZ →	0100
MDR1 →	0101
MAR1 →	0110
Un-add-temp →	0111
M-value →	1000
Un-add →	1001
mul-result →	1010
not used ⇒	;



Tn	
"1" →	000
Un-add-temp →	001
Tn →	010
MDR2 →	011
Un-value →	100
MDR2 →	101
not used ⇒	;