Interpolation

Test bench:
Test bench file is test_bench.tcl which uses InterploationMiniMain.v to test the interpolation module, both can be found in Interpolation Module/Test.

SW equivalent can be found in the same folder and it takes two inputs number of Us and M (size of the U vector).

Note:- M can take any value but the number of Us is related to a local param in the Interpolation_Module.v called uo_add as uo_add = Us num + 2
So to generate 4 Us u0_add needs to be 16'd6 (its current value)
The software generates .txt file which .tcl file uses it to fill the ram.

As for synthesis:
Generated .v output and reports can be found in
Interpolation Module/Synthesis and named:
Interploation_Module_after.syn.v

Used clock period is 2.2
Reports summary

	Default	I2R	I20	R20
Slack time	369	250.9	.7	118.8

	Internal	Switching	Leakage	Total
Power(uw)	1345.088	1789.8	83.4	3218.3

Number of Cells	Cells Area	Chip size	Placeable Are	Moveable Cell area	Utilization
2319	4157	20516	6874	4157	60%