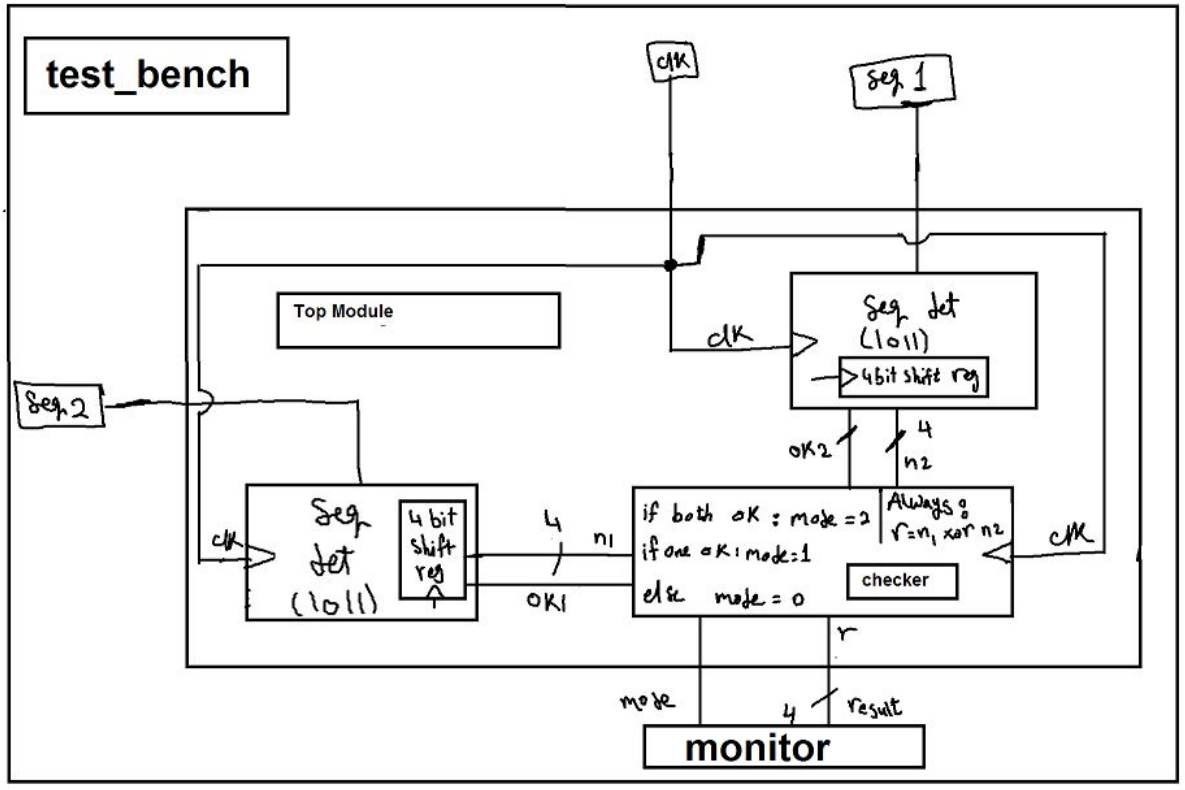
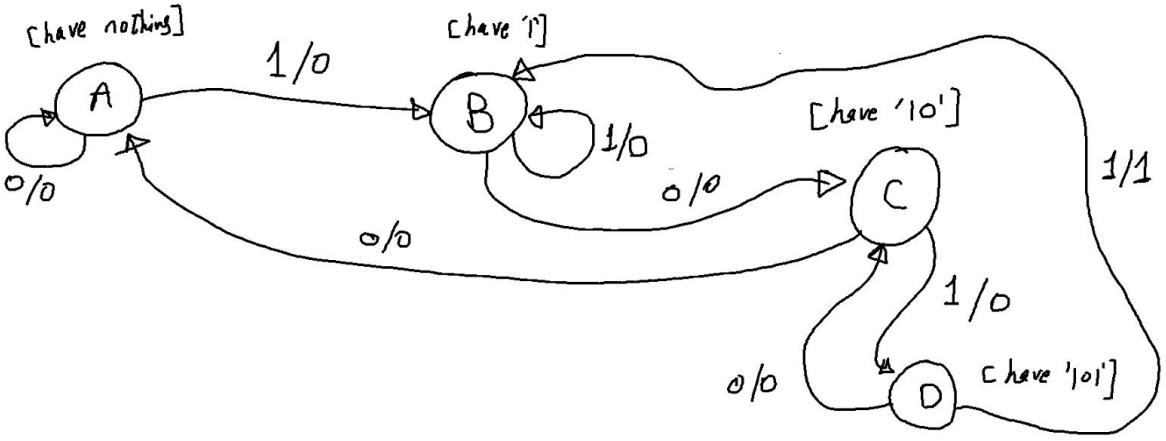
Sec 1 : Verilog problem

Q) Implement the following design in verilog, with an appropriate test bench. You have two sequence detectors, each fire their “ok” signal when they receive a sequence of “1011”. Also, internally, each one of those has a 4-bit serial-in-parallel-out shift register, that receives the sequence bit by bit and outputs the 4-bit parallel output as seen in the figure. The output of the shift registers as propagated as the output of the sequence detector itself. The “checker” module checks both “ok1” and “ok2”. If both are asserted on a certain clock edge, it will output a mode of “2”. If only one is asserted, it will output a mode of “1” , else it will output a mode of “0”. It also outputs “r” which is always “n1” xor “n2” . The two detectors and the checker are all placed in and connected by the Top Module. a test_bench is connected to the top module to check the functionality of the whole system.



Answer :

1- sequence detector state machine :



2- Verilog Code :

See the code file.